Data Sheet

CADEKA
Amplify the Human Experience

COMLINEAR® CLC1603, CLC3603, CLC3613

Single and Triple, 1.1mA, 200MHz Amplifiers

FEATURES

- 0.1dB gain flatness to 30MHz
- 0.01%/0.03° differential gain/phase
- 200MHz -3dB bandwidth at G = 2
- 140MHz large signal bandwidth
- 450V/µs slew rate
- 1.1mA supply current (enabled)
- 0.35mA supply current (disabled)
- 100mA output current
- Fully specified at 5V and ±5V supplies
- CLC1603: Pb-free SOT23-6
- CLC3603: Pb-free SOIC-16
- CLC3613: Pb-free SOIC-14

APPLICATIONS

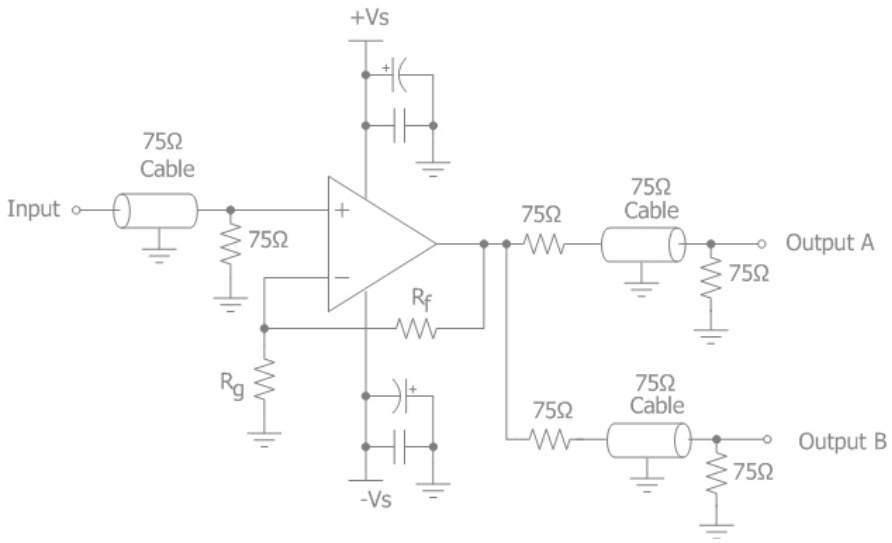
- RGB video line drivers
- Portable Video
- Line drivers
- Set top box
- Active filters
- Cable drivers
- Imaging applications
- Radar/communication receivers

General Description

The COMLINEAR CLC1603 (single with disable), CLC3603 (triple with disable), and CLC3613 (triple) are high-performance, current feedback amplifiers that provide 240MHz unity gain bandwidth, ±0.1dB gain flatness to 30MHz, and 450V/µs slew rate while consuming only 1.1mA of supply current. This high performance exceeds the requirements of NTSC/PAL/HDTV video applications. These COMLINEAR high-performance amplifiers also provide ample output current to drive multiple video loads.

The COMLINEAR CLC1603, CLC3603, and CLC3613 are designed to operate from ±5V or +5V supplies. The CLC1603 and CLC3603 offer a enable/disable feature to save power. While disabled, the outputs are in a high-impedance state to allow for multiplexing applications. The combination of high-speed, low-power, and excellent video performance make these amplifiers well suited for use in many general purpose, high-speed applications including set top boxes, high-definition video, active filters, and cable driving applications.

Typical Application - Driving Dual Video Loads



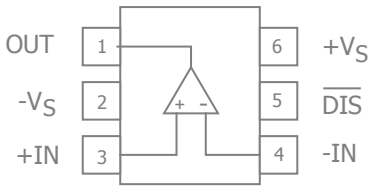
Ordering Information

Part Number	Package	Disable Option	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1603IST6X	SOT23-6	Yes	Yes	Yes	-40°C to +85°C	Reel
CLC3613ISO14X	SOIC-14	No	Yes	Yes	-40°C to +85°C	Reel
CLC3613ISO14	SOIC-14	No	Yes	Yes	-40°C to +85°C	Rail
CLC3603ISO16X	SOIC-16	Yes	Yes	Yes	-40°C to +85°C	Reel
CLC3603ISO16	SOIC-16	Yes	Yes	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

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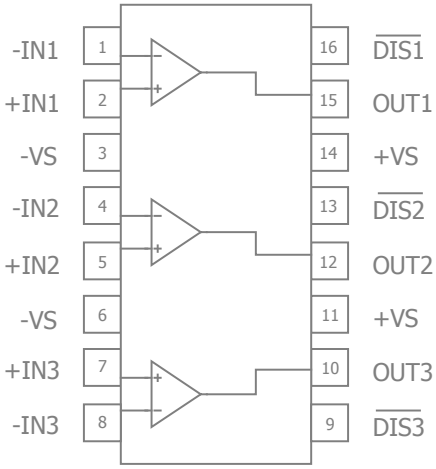
CLC1603 Pin Configuration



CLC1603 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.
6	$+V_S$	Positive supply

CLC3603 Pin Configuration



CLC3603 Pin Assignments

Pin No.	Pin Name	Description
1	-IN1	Negative input, channel 1
2	+IN1	Positive input, channel 1
3	$-V_S$	Negative supply
4	-IN2	Negative input, channel 2
5	+IN2	Positive input, channel 2
6	$-V_S$	Negative supply
7	+IN3	Positive input, channel 3
8	-IN3	Negative input, channel 3
9	$\overline{DIS3}$	Disable pin for channel 3. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.
10	OUT3	Output, channel 3
11	$+V_S$	Positive supply
12	OUT2	Output, channel 2
13	$\overline{DIS2}$	Disable pin for channel 2. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.
14	$+V_S$	Positive supply
15	OUT1	Output, channel 1
16	$\overline{DIS1}$	Disable pin for channel 2. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.

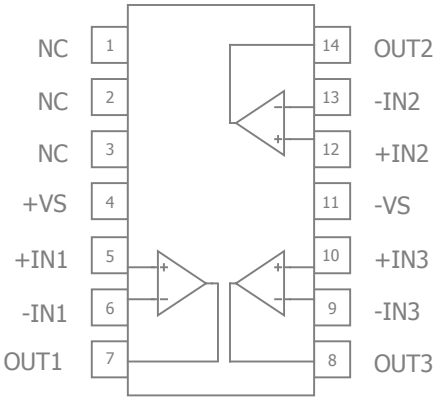
Disable Pin Truth Table

Pin	High* (> ($+V_S$ - 1.5V))	Low (< ($+V_S$ - 3.5V))
$\overline{DIS}$	Enabled	Disabled

*Default Open State

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CLC3613 Pin Configuration



CLC3613 Pin Assignments

Pin No.	Pin Name	Description
1	NC	No Connect
2	NC	No Connect
3	NC	No Connect
4	+V_S	Positive supply
5	+IN1	Positive input, channel 1
6	-IN1	Negative input, channel 1
7	OUT1	Output, channel 1
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	-V_S	Negative supply
12	+IN2	Positive input, channel 2
13	-IN2	Negative input, channel 2
14	OUT2	Output, channel 2

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V
Continuous Output Current		100	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
6-Lead SOT23		177		°C/W
14-Lead SOIC		88		°C/W
16-Lead SOIC		68		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOT23-6	SOIC-14	SOIC-16
Human Body Model (HBM)	2kV	2kV	2kV
Charged Device Model (CDM)	1kV	1kV	1kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	4.5		12	V

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Electrical Characteristics at +5V

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = GND, R_f = R_g =1.2kΩ, R_L = 100Ω to $+V_S/2$, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	Unity Gain Bandwidth	G = +1, V_{OUT} = 0.5V_{pp}, R_f = 2.5kΩ		210		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.5V_{pp}		180		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 1V_{pp}		160		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.5V_{pp}		15		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		3		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		18		ns
	Settling Time to 0.01%	V_{OUT} = 1V step		40		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	1V step		350		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		-60		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		-51		dBc
THD	Total Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		50		dB
D_G	Differential Gain	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.01		%
D_P	Differential Phase	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.04		°
IP3	Third Order Intercept	V_{OUT} = 1V_{pp}, 10MHz		26		dBm
SFDR	Spurious Free Dynamic Range	V_{OUT} = 1V_{pp}, 5MHz		58		dBc
e_n	Input Voltage Noise	> 1MHz		4		nV/√Hz
i_n	Input Current Noise	> 1MHz, Inverting		15		pA/√Hz
		> 1MHz, Non-Inverting		15		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		56		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.5		mV
dV_{IO}	Average Drift			6		µV/°C
I_{bn}	Input Bias Current - Non-Inverting			2		µA
dI_{bn}	Average Drift			40		nA/°C
I_{bi}	Input Bias Current - Inverting			0.4		µA
dI_{bi}	Average Drift			10		nA/°C
PSRR	Power Supply Rejection Ratio	DC		60		dB
I_S	Supply Current	per channel		0.9		mA
Disable Characteristics - CLC1603, CLC3603						
T_{ON}	Turn On Time			100		ns
T_{OFF}	Turn Off Time			2.25		µs
V_{OFF}	Power Down Input Voltage	$\overline{DIS}$ pin, disabled if pin is grounded or pulled below V_{OFF} = $+V_s$ - 3.5V	Disabled if < ($+V_s$ - 3.5V)			V
V_{ON}	Enable Input Voltage	$\overline{DIS}$ pin, enabled if pin is left open or pulled above V_{ON} = $+V_s$ - 1.5V	Enabled if > ($+V_s$ - 1.5V)			V
I_{SD}	Disable Supply Current	$\overline{DIS}$ pin is grounded		0.15		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4		MΩ
		Inverting		350		Ω
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			1.5 to 3.5		V
CMRR	Common Mode Rejection Ratio	DC		55		dB

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Electrical Characteristics at +5V continued

T_A = 25°C, $+V_s$ = 5V, $-V_S$ = GND, R_f = R_g =1.2kΩ, R_L = 100Ω to $+V_S/2$, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.02		Ω
V_{OUT}	Output Voltage Swing	R_L = 100Ω		1.4 to 3.6		V
I_{OUT}	Output Current			±140		mA

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Electrical Characteristics at ±5V

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	Unity Gain Bandwidth	G = +1, V_{OUT} = 0.5V_{pp}, R_f = 2.5kΩ		240		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.5V_{pp}		200		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		120		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.5V_{pp}		30		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 2V step; (10% to 90%)		4		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		18		ns
	Settling Time to 0.01%	V_{OUT} = 2V step		35		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	2V step		450		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		-67		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		-57		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz, R_L = 150Ω		55		dB
D_G	Differential Gain	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.01		%
D_P	Differential Phase	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.03		°
IP3	Third Order Intercept	V_{OUT} = 0.5V_{pp}, 10MHz		35		dBm
SFDR	Spurious Free Dynamic Range	V_{OUT} = 1V_{pp}, 5MHz		58		dBc
e_n	Input Voltage Noise	> 1MHz		4		nV/√Hz
i_n	Input Current Noise	> 1MHz, Inverting		15		pA/√Hz
		> 1MHz, Non-Inverting		15		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		56		dB
DC Performance						
V_{IO}	Input Offset Voltage (1)		-4	0.7	4	mV
dV_{IO}	Average Drift			6		µV/°C
I_{bn}	Input Bias Current - Non-Inverting (1)		-5	2	5	µA
dI_{bn}	Average Drift			40		nA/°C
I_{bi}	Input Bias Current - Inverting (1)		-5	2	5	µA
dI_{bi}	Average Drift			10		nA/°C
PSRR	Power Supply Rejection Ratio (1)	DC	50	75		dB
I_S	Supply Current (1)	CLC1603		1.1	2.5	mA
		CLC3603, CLC3613		3.3	6.5	mA
Disable Characteristics - CLC1603, CLC3603						
T_{ON}	Turn On Time			250		ns
T_{OFF}	Turn Off Time			2.25		µs
V_{OFF}	Power Down Input Voltage	$\overline{DIS}$ pin, disabled if pin is grounded or pulled below V_{OFF} = $+V_s$ - 3.5V	Disabled if < ($+V_s$ - 3.5V)			V
V_{ON}	Enable Input Voltage	$\overline{DIS}$ pin, enabled if pin is left open or pulled above V_{ON} = $+V_s$ - 1.5V	Enabled if > ($+V_s$ - 1.5V)			V
I_{SD}	Disable Supply Current (1)	$\overline{DIS}$ pin is grounded, CLC1603		0.11	0.5	mA
		$\overline{DIS}$ pin is grounded, CLC3603		0.3	0.5	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4		MΩ
		Inverting		350		Ω
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			±4.0		V

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Electrical Characteristics at ±5V continued

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMRR	Common Mode Rejection Ratio (1)	DC	50	60		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.1		Ω
V_{OUT}	Output Voltage Swing	R_L = 100Ω (1)	-3.0	±3.5	+3.0	V
I_{OUT}	Output Current			±270		mA

Notes:

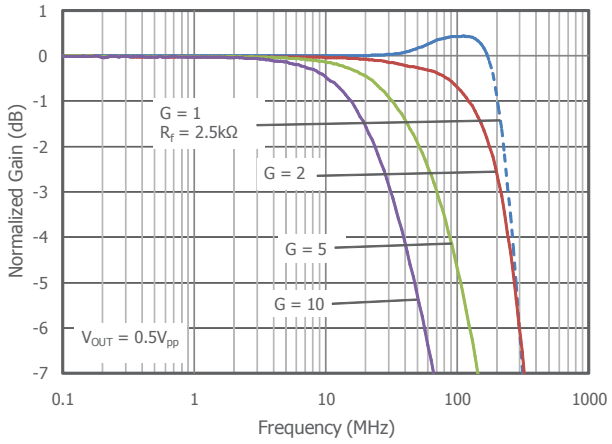
1. 100% tested at 25°C

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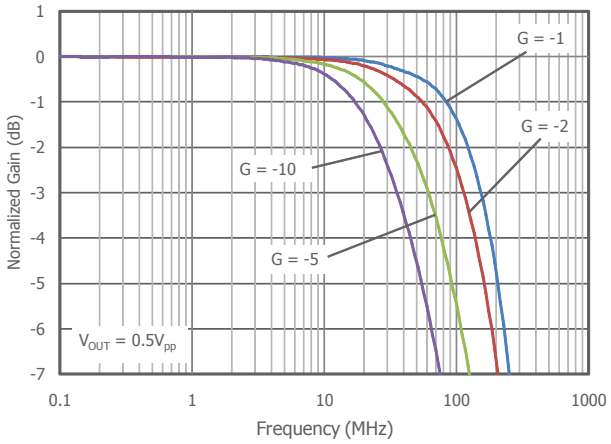
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

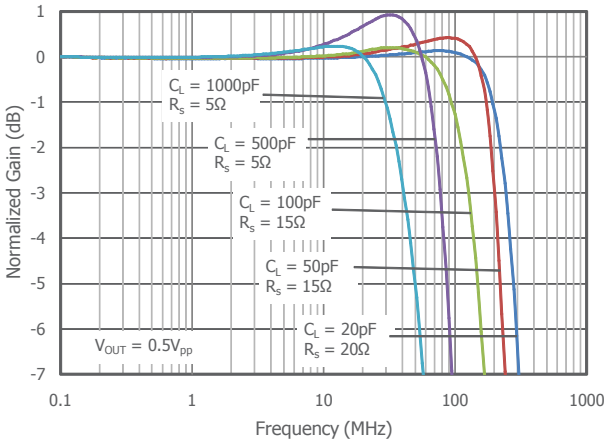
Non-Inverting Frequency Response



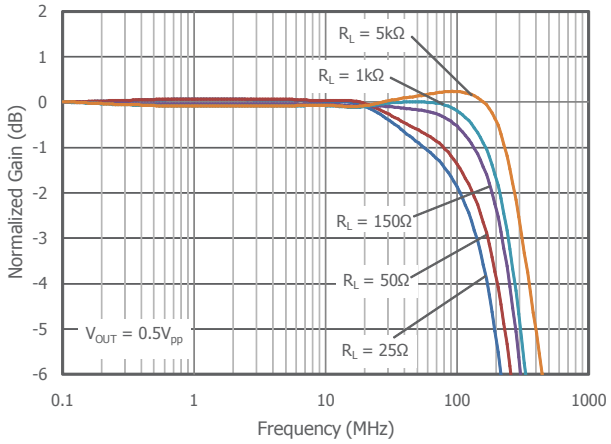
Inverting Frequency Response



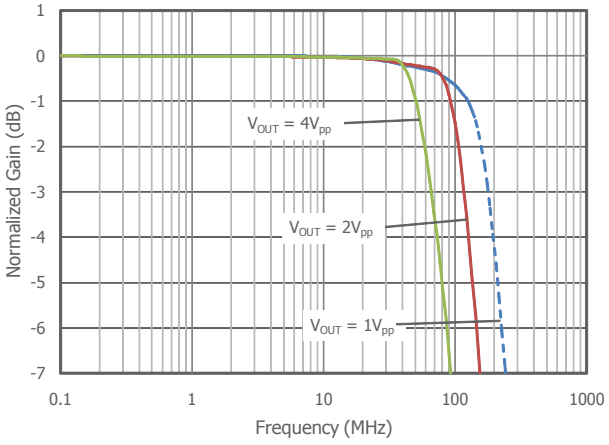
Frequency Response vs. C_L



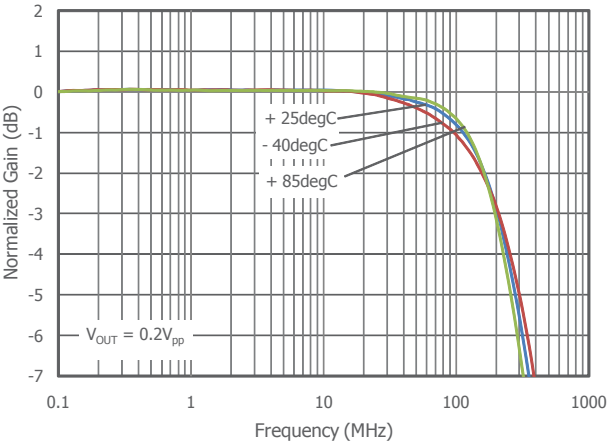
Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



Frequency Response vs. Temperature

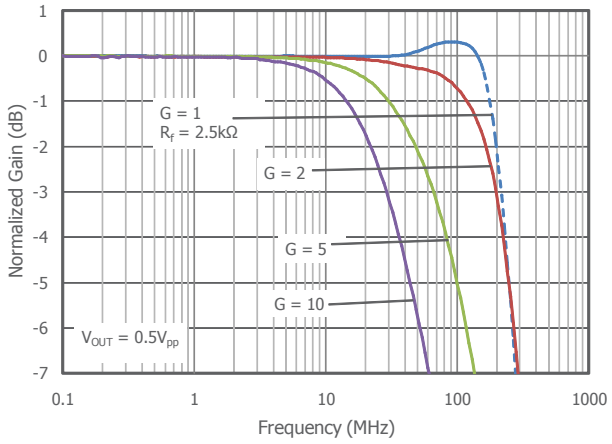


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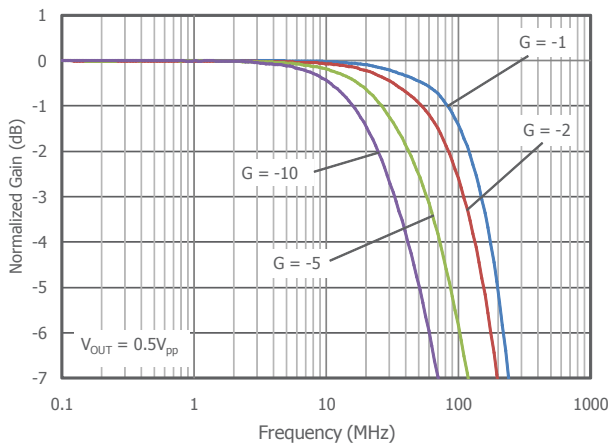
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

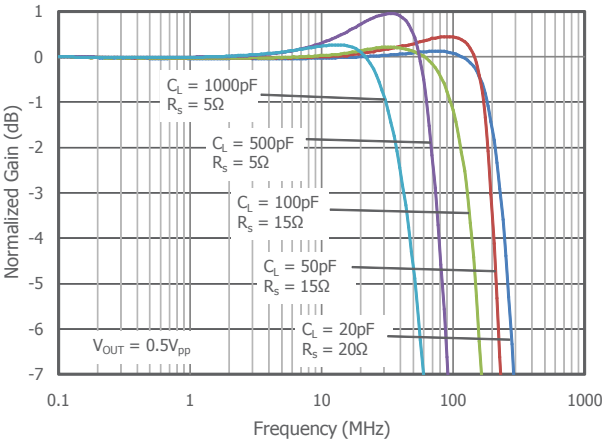
Non-Inverting Frequency Response at $+V_S$ = 5V, $-V_S$=GND



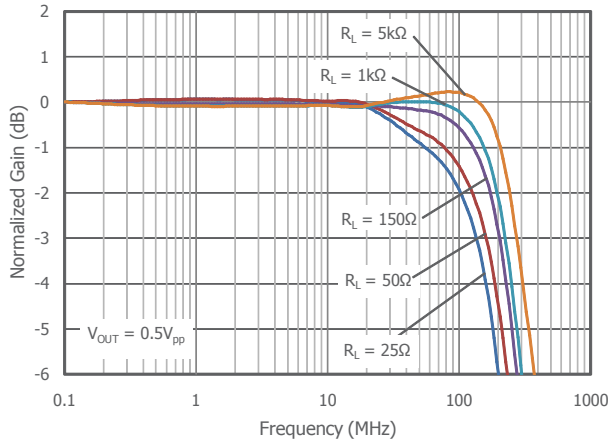
Inverting Frequency Response at $+V_S$ = 5V, $-V_S$ = GND



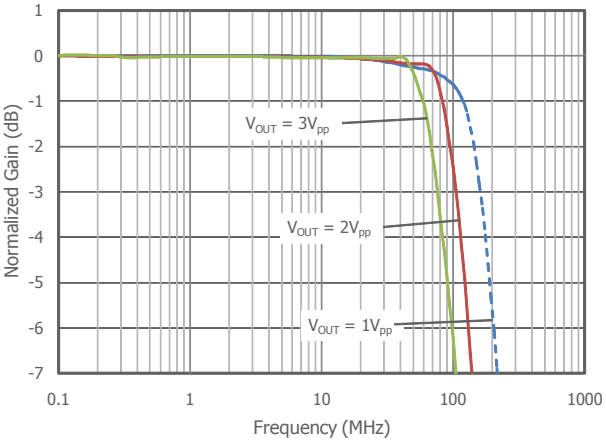
Frequency Response vs. C_L at $+V_S$ = 5V, $-V_S$ = GND



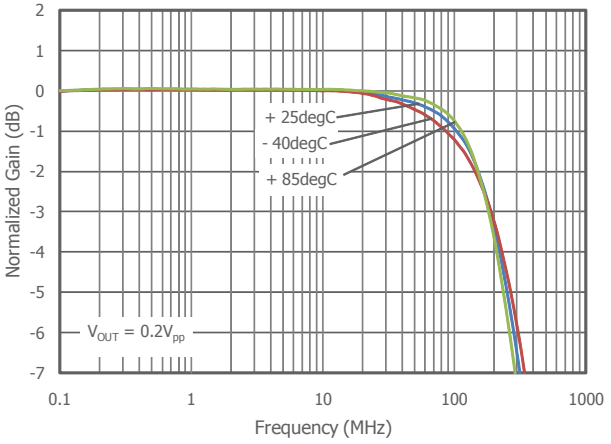
Frequency Response vs. R_L at $+V_S$ = 5V, $-V_S$ = GND



Frequency Response vs. V_{OUT} at $+V_S$ = 5V, $-V_S$ = GND



Frequency Response vs. Temp. at $+V_S$ = 5V, $-V_S$ = GND

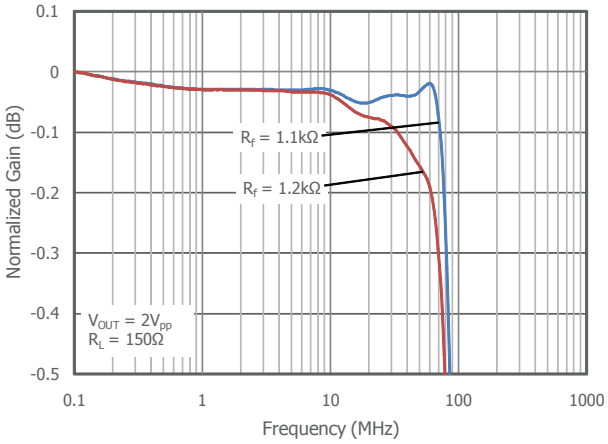


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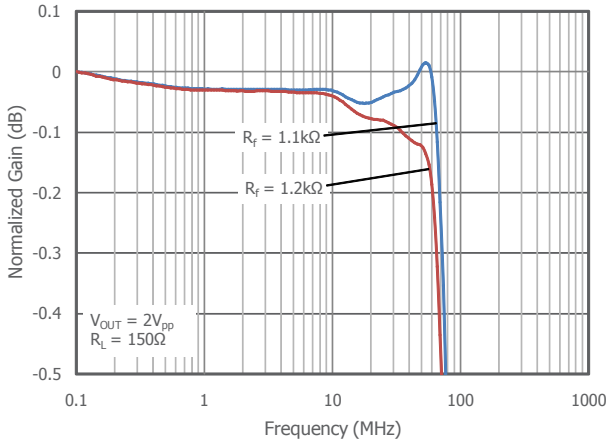
Typical Performance Characteristics - Continued

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

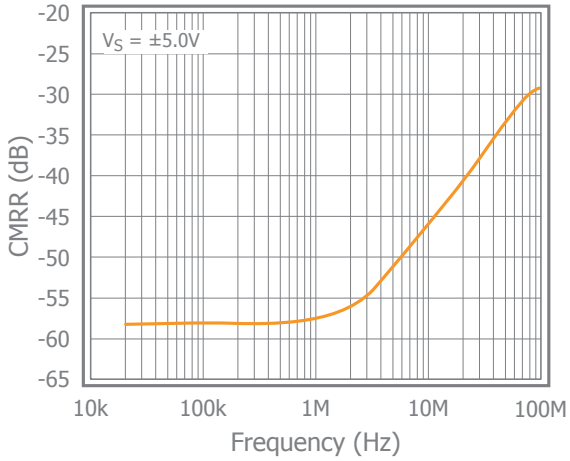
Gain Flatness



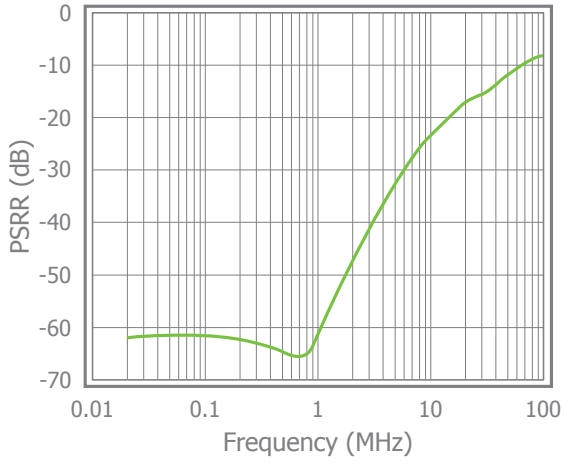
Gain Flatness at $+V_S$ = 5V, $-V_S$ = GND



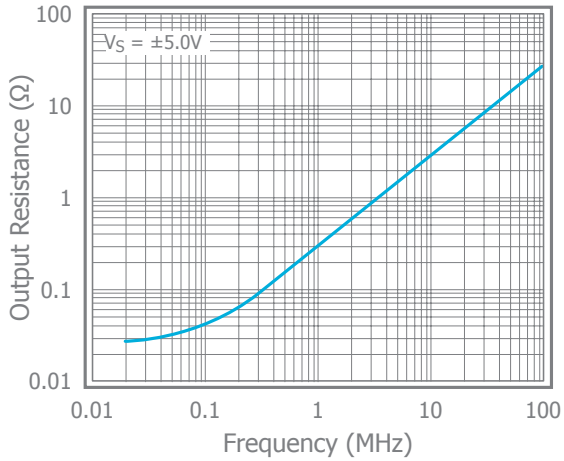
CMRR vs. Frequency



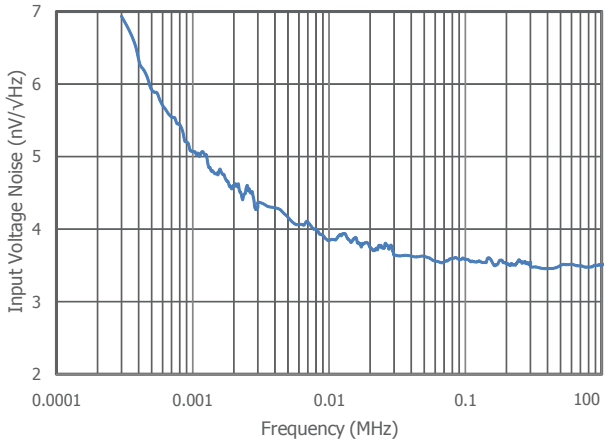
PSRR vs. Frequency



Closed Loop Output Impedance vs Frequency



Input Voltage Noise

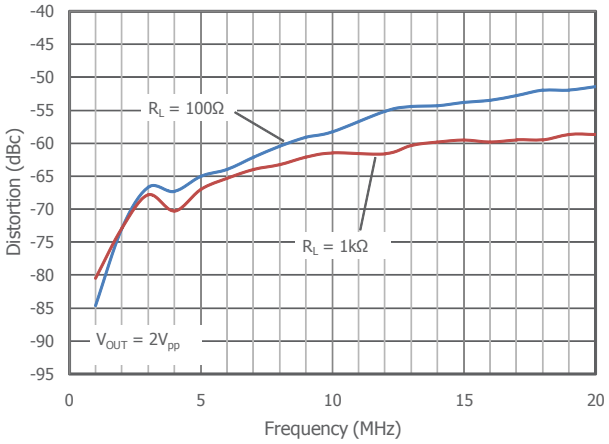


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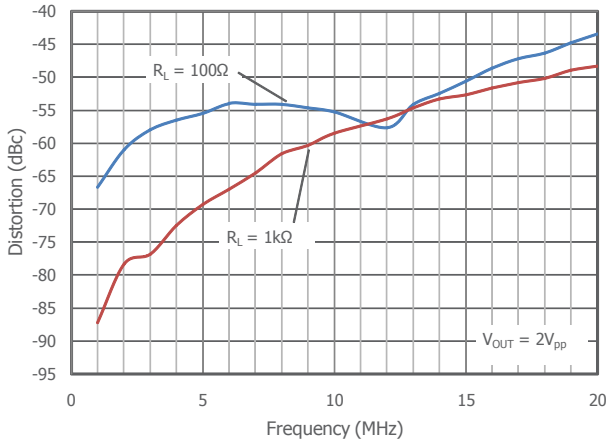
Typical Performance Characteristics - Continued

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

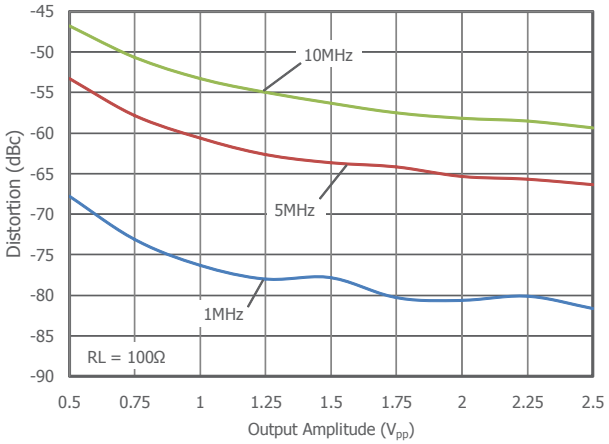
2nd Harmonic Distortion vs. R_L



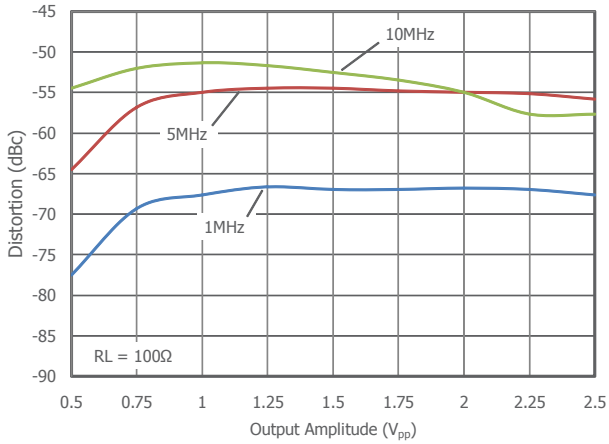
3rd Harmonic Distortion vs. R_L



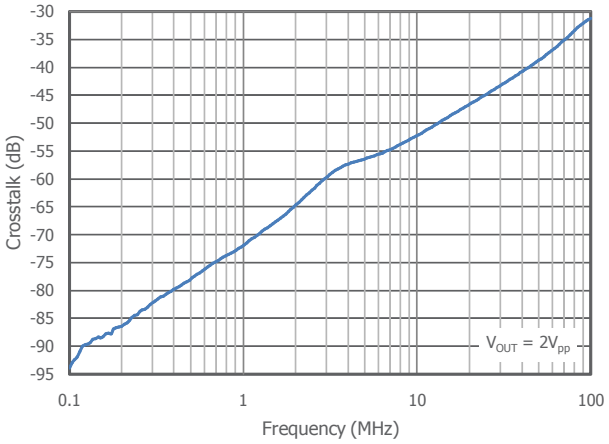
2nd Harmonic Distortion vs. V_{OUT}



3rd Harmonic Distortion vs. V_{OUT}



Crosstalk vs. Frequency

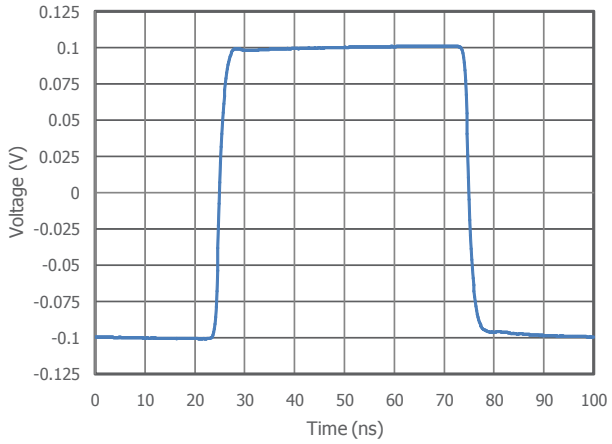


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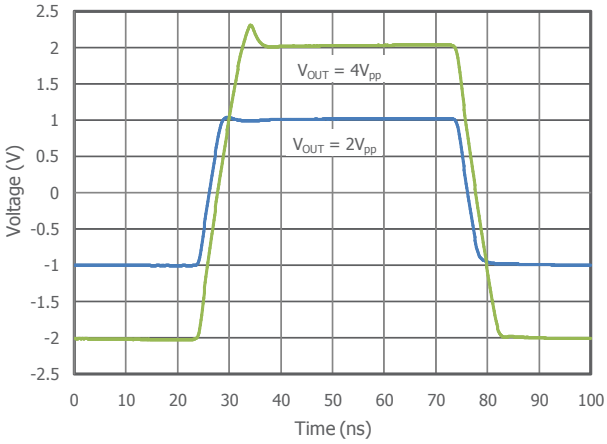
Typical Performance Characteristics - Continued

T_A = 25°C, $+V_S$ = 5V, $-V_S$ = -5V, R_f = R_g =1.2kΩ, R_L = 100Ω to GND, G = 2; unless otherwise noted.

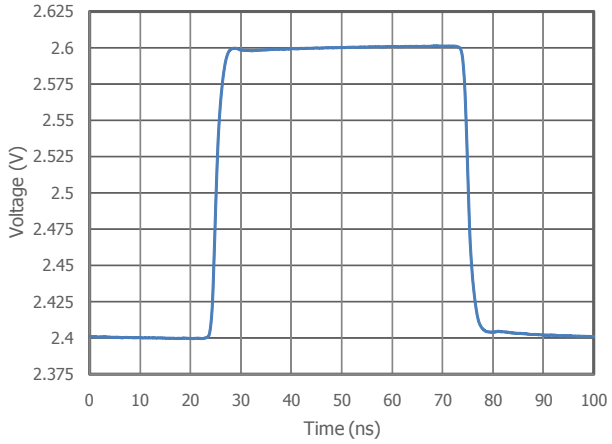
Small Signal Pulse Response



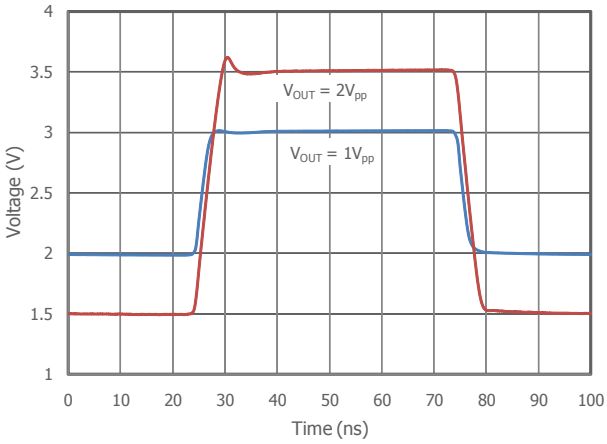
Large Signal Pulse Response



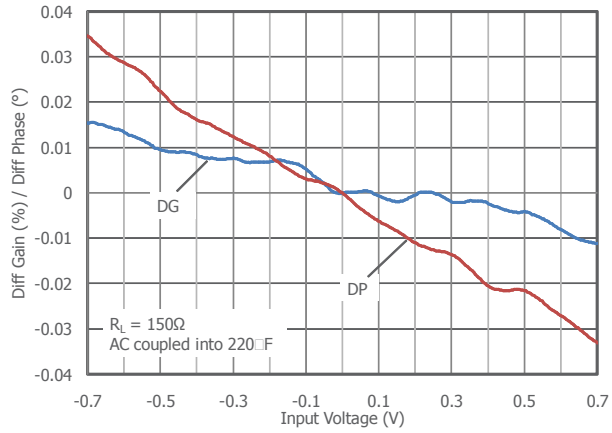
Small Signal Pulse Response at $+V_S$ = 5V, $-V_S$ = GND



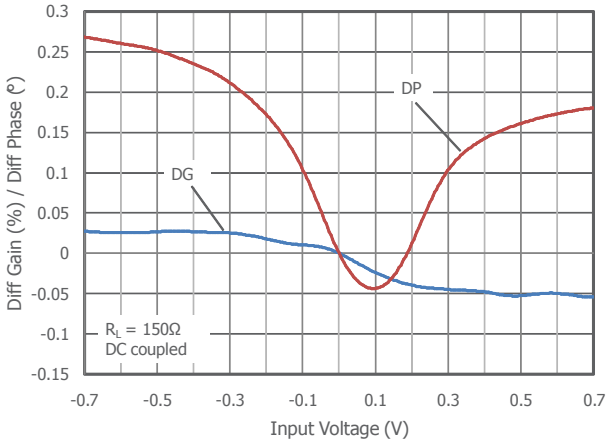
Large Signal Pulse Response at $+V_S$ = 5V, $-V_S$ = GND



Differential Gain & Phase AC Coupled Output



Differential Gain & Phase DC Coupled Output



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General Information - Current Feedback Technology

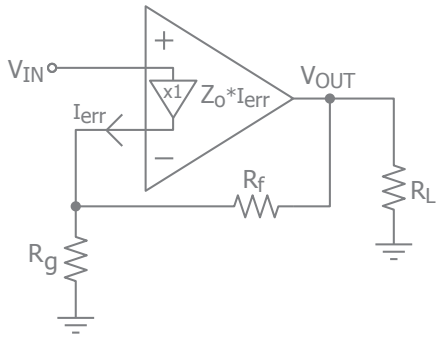
Advantages of CFB Technology

The CLCx603 Family of amplifiers utilize current feedback (CFB) technology to achieve superior performance. The primary advantage of CFB technology is higher slew rate performance when compared to voltage feedback (VFB) architecture. High slew rate contributes directly to better large signal pulse response, full power bandwidth, and distortion.

CFB also alleviates the traditional trade-off between closed loop gain and usable bandwidth that is seen with a VFB amplifier. With CFB, the bandwidth is primarily determined by the value of the feedback resistor, R_f. By using optimum feedback resistor values, the bandwidth of a CFB amplifier remains nearly constant with different gain configurations.

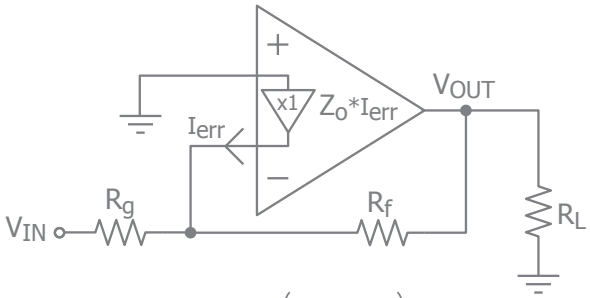
When designing with CFB amplifiers always abide by these basic rules:

- Use the recommended feedback resistor value
- Do not use reactive (capacitors, diodes, inductors, etc.) elements in the direct feedback path
- Avoid stray or parasitic capacitance across feedback resistors
- Follow general high-speed amplifier layout guidelines
- Ensure proper precautions have been made for driving capacitive loads



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_f}{R_g}\right) + \left(\frac{1}{1 + \frac{R_f}{Z_{o(j\omega)}}}\right) \quad \text{Eq. 1}$$

Figure 1. Non-Inverting Gain Configuration with First Order Transfer Function



$$\frac{V_{OUT}}{V_{IN}} = \left(-\frac{R_f}{R_g}\right) + \left(\frac{1}{1 + \frac{R_f}{Z_{o(j\omega)}}}\right) \quad \text{Eq. 2}$$

Figure 2. Inverting Gain Configuration with First Order Transfer Function

CFB Technology - Theory of Operation

Figure 1 shows a simple representation of a current feedback amplifier that is configured in the traditional non-inverting gain configuration.

Instead of having two high-impedance inputs similar to a VFB amplifier, the inputs of a CFB amplifier are connected across a unity gain buffer. This buffer has a high impedance input and a low impedance output. It can source or sink current (I_{err}) as needed to force the non-inverting input to track the value of Vin. The CFB architecture employs a high gain trans-impedance stage that senses Ierr and drives the output to a value of ($Z_o(j\omega)$ * I_{err}) volts. With the application of negative feedback, the amplifier will drive the output to a voltage in a manner which tries to drive Ierr to zero. In practice, primarily due to limitations on the value of $Z_o(j\omega)$, Ierr remains a small but finite value.

A closer look at the closed loop transfer function (Eq.1) shows the effect of the trans-impedance, $Z_o(j\omega)$ on the gain of the circuit. At low frequencies where $Z_o(j\omega)$ is very large with respect to R_f, the second term of the equation approaches unity, allowing R_f and R_g to set the gain. At higher frequencies, the value of $Z_o(j\omega)$ will roll off, and the effect of the secondary term will begin to dominate. The -3dB small signal parameter specifies the frequency where the value $Z_o(j\omega)$ equals the value of R_f causing the gain to drop by 0.707 of the value at DC.

For more information regarding current feedback amplifiers, visit www.cadeka.com for detailed application notes, such as AN-3: *The Ins and Outs of Current Feedback Amplifiers*.

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Application Information

Basic Operation

Figures 3, 4, and 5 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

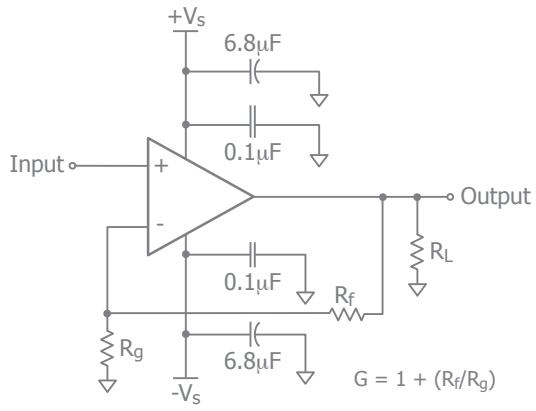


Figure 3. Typical Non-Inverting Gain Circuit

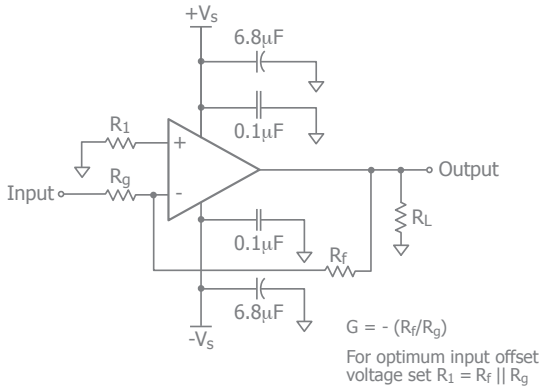


Figure 4. Typical Inverting Gain Circuit

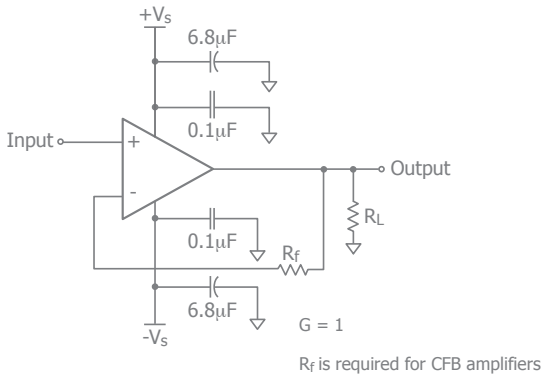


Figure 5. Typical Unity Gain (G=1) Circuit

CFB amplifiers can be used in unity gain configurations. Do not use the traditional voltage follower circuit, where the output is tied directly to the inverting input. With a CFB amplifier, a feedback resistor of appropriate value must be used to prevent unstable behavior. Refer to figure 5 and Table 1. Although this seems cumbersome, it does allow a degree of freedom to adjust the passband characteristics.

Feedback Resistor Selection

One of the key design considerations when using a CFB amplifier is the selection of the feedback resistor, R_f. R_f is used in conjunction with R_g to set the gain in the traditional non-inverting and inverting circuit configurations. Refer to figures 3 and 4. As discussed in the Current Feedback Technology section, the value of the feedback resistor has a pronounced effect on the frequency response of the circuit.

Table 1, provides recommended R_f and associated R_g values for various gain settings. These values produce the optimum frequency response, maximum bandwidth with minimum peaking. Adjust these values to optimize performance for a specific application. The typical performance characteristics section includes plots that illustrate how the bandwidth is directly affected by the value of R_f at various gain settings.

Gain (V/V	R_f (Ω)	R_g (Ω)	±0.1dB BW (MHz)	-3dB BW (MHz)
1	2.5k	--	42	240
2	1.2k	1.2k	30	200
5	1.2k	300	8	70

Table 1: Recommended R_f vs. Gain

In general, lowering the value of R_f from the recommended value will extend the bandwidth at the expense of additional high frequency gain peaking. This will cause increased overshoot and ringing in the pulse response characteristics. Reducing R_f too much will eventually cause oscillatory behavior.

Increasing the value of R_f will lower the bandwidth. Lowering the bandwidth creates a flatter frequency response and improves 0.1dB bandwidth performance. This is important in applications such as video. Further increase in R_f will cause premature gain rolloff and adversely affect gain flatness.

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Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

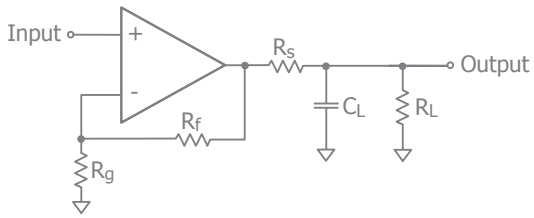


Figure 6. Addition of R_S for Driving Capacitive Loads

Table 2 provides the recommended R_S for various capacitive loads. The recommended R_S values result in <=0.5dB peaking in the frequency response. The Frequency Response vs. C_L plot, on pages 9 and 10, illustrate the response of the CLCx603 Family.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
10	40	350
50	20	200
100	15	140

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Parasitic Capacitance on the Inverting Input

Physical connections between components create unintentional or parasitic resistive, capacitive, and inductive elements.

Parasitic capacitance at the inverting input can be especially troublesome with high frequency amplifiers. A parasitic capacitance on this node will be in parallel with the gain setting resistor R_g. At high frequencies, its impedance can begin to raise the system gain by making R_g appear smaller.

In general, avoid adding any additional parasitic capacitance at this node. In addition, stray capacitance across the R_f resistor can induce peaking and high frequency ringing. Refer to the **Layout Considerations** section for additional information regarding high speed layout techniques.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLCx603 Family will typically recover in less than 30ns from an overdrive condition. Figure 7 shows the CLC1603 in an overdriven condition.

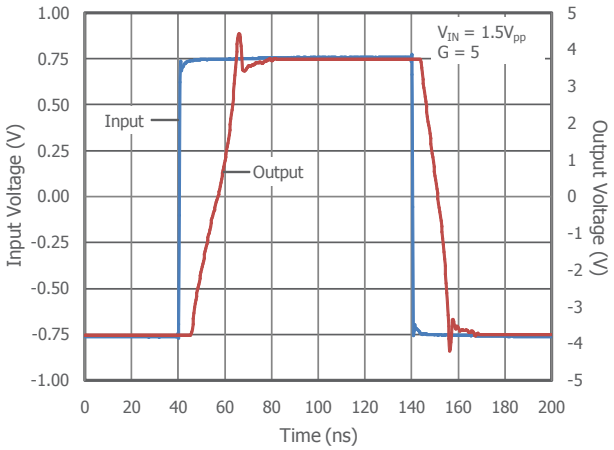


Figure 7. Overdrive Recovery

Power Dissipation

Power dissipation should not be a factor when operating under the stated 100 ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

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In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$P_D = P_{supply} - P_{load}$

Supply power is calculated by the standard power equation.

$P_{supply} = V_{supply} \times I_{RMS\ supply}$

$V_{supply} = V_{S+} - V_{S-}$

Power delivered to a purely resistive load is:

$P_{load} = ((V_{LOAD})_{RMS^2})/Rload_{eff}$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 3 would be calculated as:

$R_L \,||\, (R_f + R_g)$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$

$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 8 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8 and 14 lead SOIC packages.

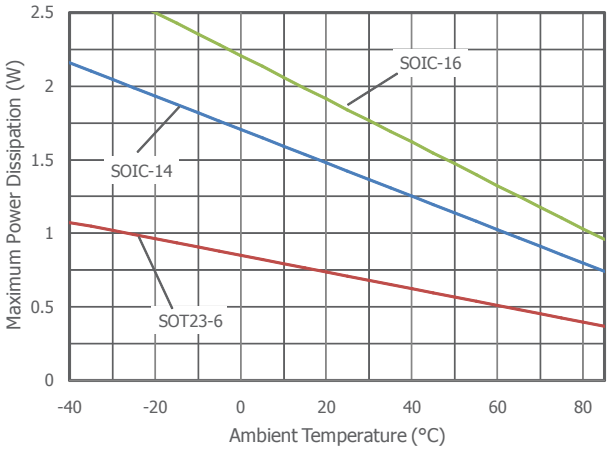


Figure 8. Maximum Power Derating

Better thermal ratings can be achieved by maximizing PC board metallization at the package pins. However, be careful of stray capacitance on the input pins.

In addition, increased airflow across the package can also help to reduce the effective Θ_{JA} of the package.

In the event the outputs are momentarily shorted to a low impedance path, internal circuitry and output metallization are set to limit and handle up to 65mA of output current. However, extended duration under these conditions may not guarantee that the maximum junction temperature (+150°C) is not exceeded.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

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Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1603
CEB018	CLC3613
CEB013	CLC3603

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-14. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.

2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

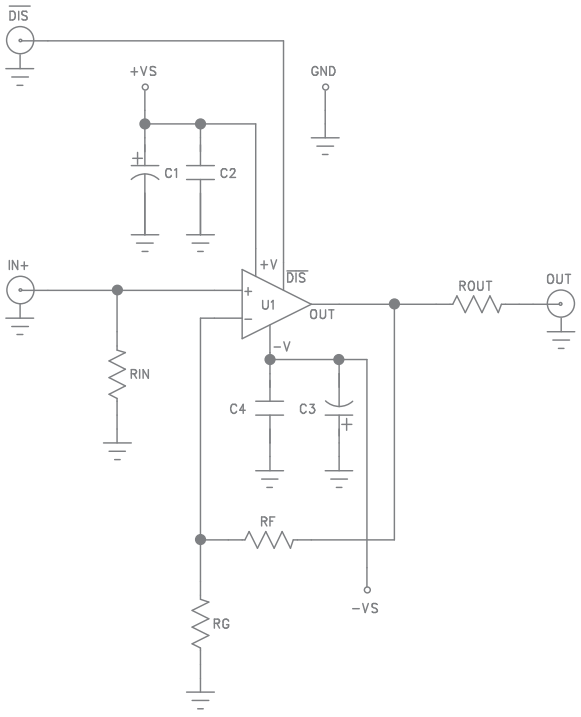


Figure 9. CEB002 Schematic

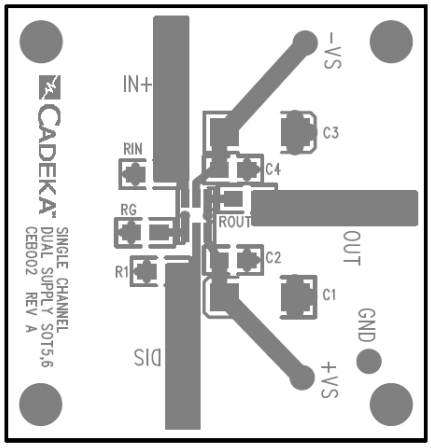


Figure 10. CEB002 Top View

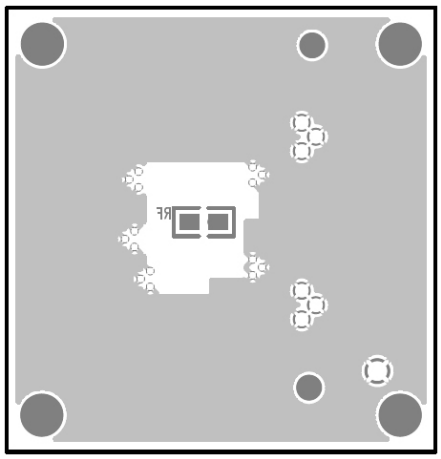


Figure 11. CEB002 Bottom View

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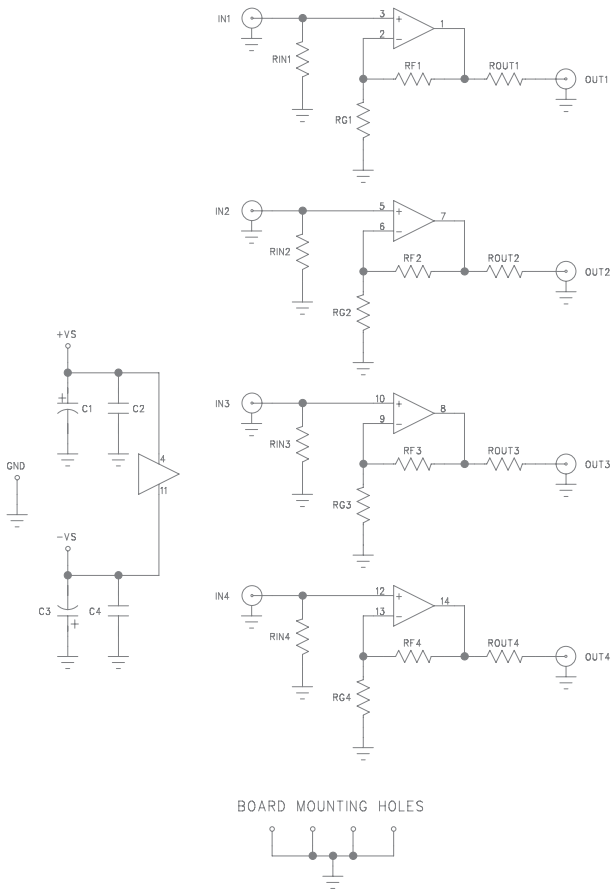


Figure 12. CEB018 Schematic

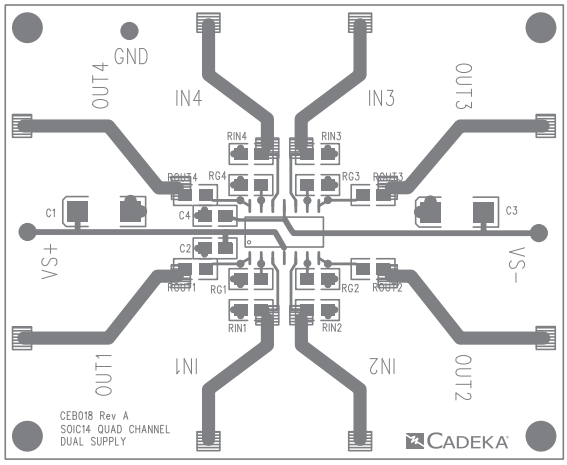


Figure 13. CEB018 Top View

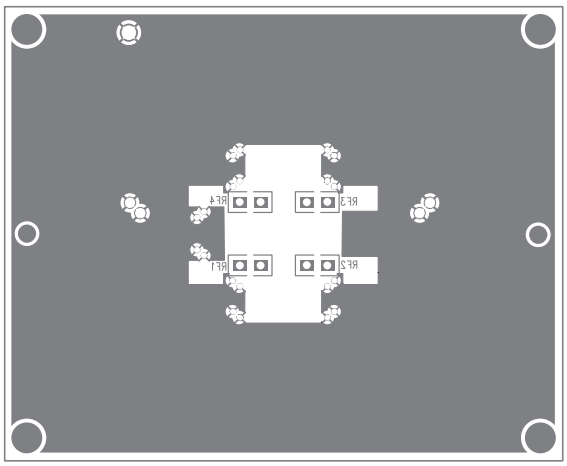


Figure 14. CEB018 Bottom View

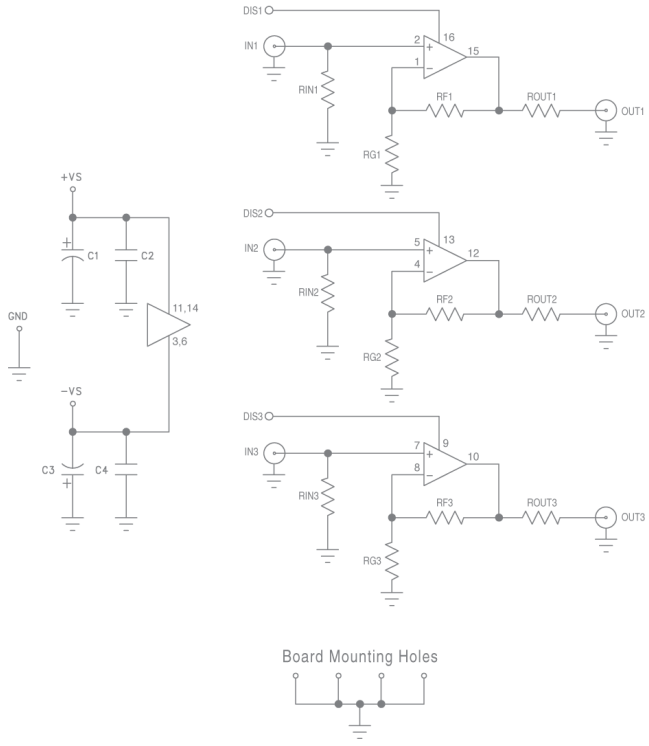


Figure 16. CEB013 Schematic

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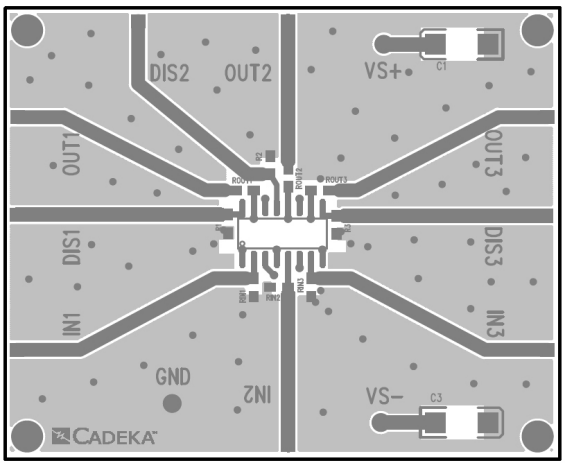


Figure 17. CEB013 Top View

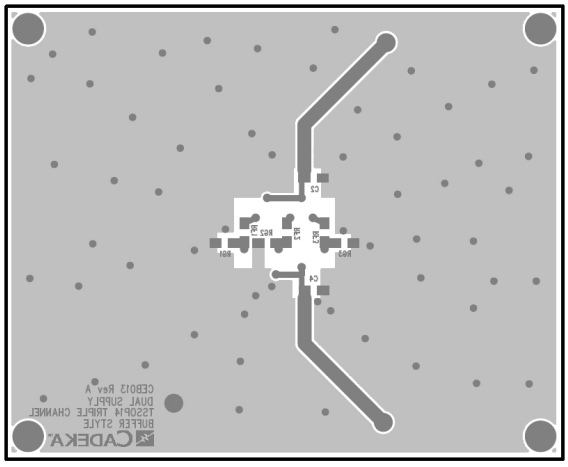
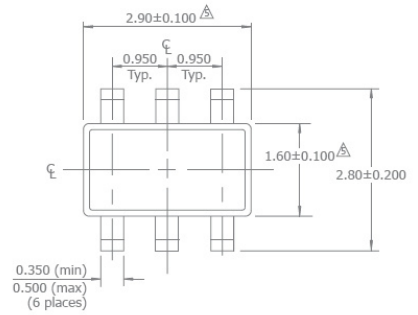


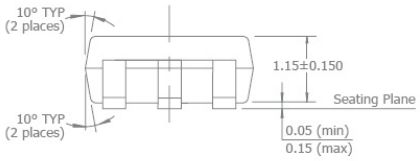
Figure 18. CEB013 Bottom View

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Mechanical Dimensions

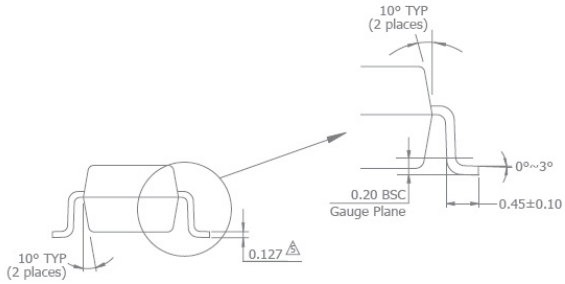
SOT23-6 Package



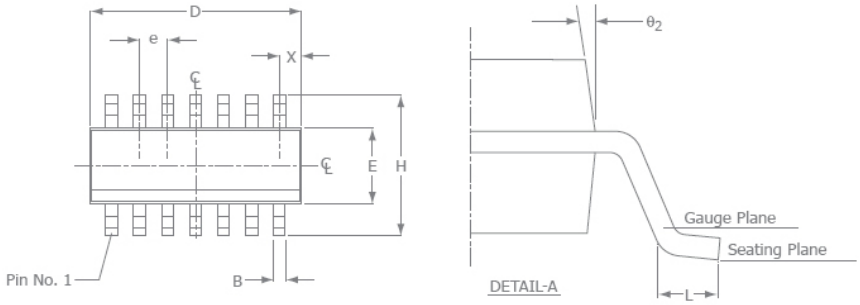


NOTES:

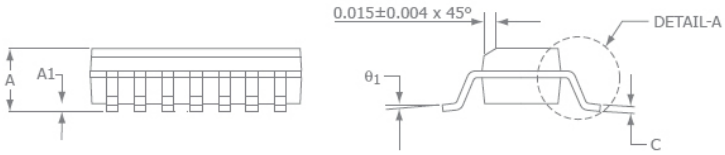
1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.
5. Dimension are exclusive of mold flash and gate burr.
6. Dimension are exclusive of solder plating.



SOIC-14



SOIC-14		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.337	0.344
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 Ref	
θ_1	0°	8°
θ_2	7° BSC	



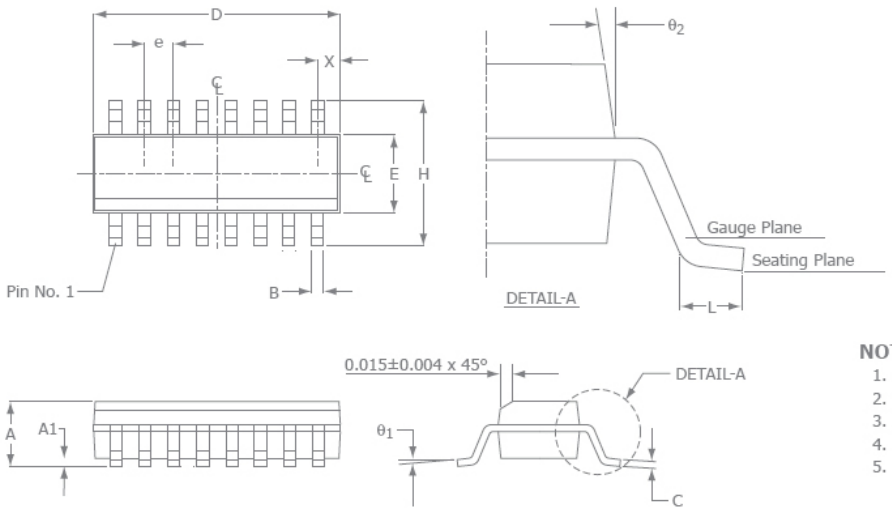
NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

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Mechanical Dimensions

SOIC-16 Package



SOIC-16		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 Ref	
θ_1	0°	8°
θ_2	7° BSC	

NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

For additional information regarding our products, please visit CADEKA at: cadeka.com

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