CLC006 Serial Digital Cable Driver with Adjustable Outputs

Check for Samples: CLC006

FEATURES

- **No External Pull-down Resistors**
- **Adjustable Output Amplitude**
- **Differential Input and Output**
- **Low Power Dissipation**
- **Single +5V or −5.2V Supply**
- **Replaces GS9008 in Most Applications**

APPLICATIONS

- **Digital Routers and Distribution Amplifiers**
- **Coaxial Cable Driver for Digital Transmission Line**
- **Twisted Pair Driver**
- **Serial Digital Video Interfaces for the Commercial and Broadcast Industry**
- **SMPTE, Sonet/SDH, and ATM Compatible Driver**
- **Buffer Applications**

KEY SPECIFICATIONS

- **650 ps Rise and Fall Times**
- **Data Rates to 400 Mbps**
- **200 mV Differential Input**
- **Low Residual Jitter (25 ps_{pp})**

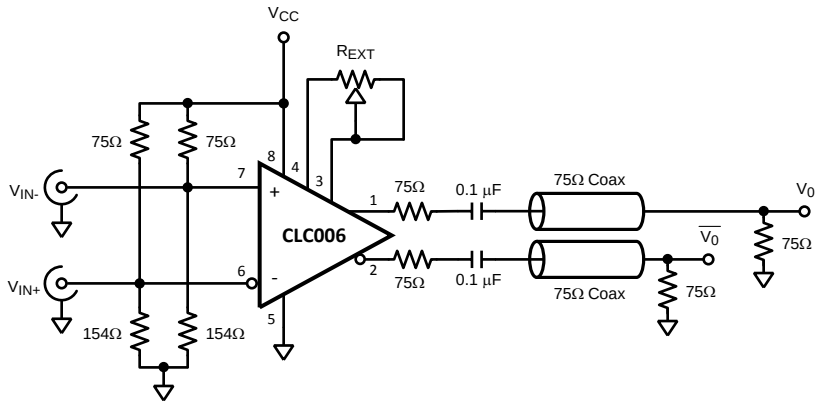
DESCRIPTION

Texas Instruments' Comlinear CLC006 is a monolithic, high-speed cable driver designed for the SMPTE 259M serial digital video data transmission standard. The CLC006 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable. Output swing is adjustable from 0.7 V_{P-P} to 2 V_{P-P} using external resistors.

The CLC006's class AB output stage consumes less power than other designs, 185 mW with both outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{P-P} to ECL levels within the specified common-mode limits. All this make the CLC006 an excellent general purpose high speed driver for digital applications.

The CLC006 is powered from a single +5V or −5.2V supply and comes in an 8-pin SOIC package.

Typical Application



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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270 Mbps Eye Pattern

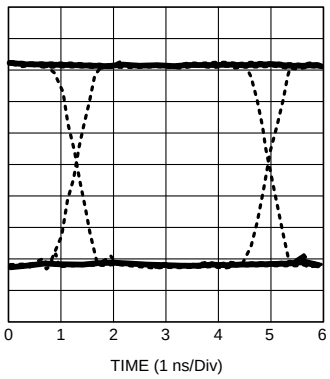


Figure 1.

Connection Diagram

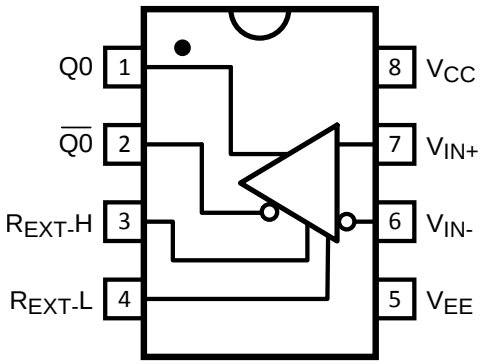


Figure 2. 8-Pin SOIC
See Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage		6V
Output Current		30 mA
Maximum Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering 10 Seconds)		+300°C
ESD Rating (Human Body Model)		1000V
Package Thermal Resistance	θ_{JA} 8–pin SOIC	+160°C/W
	θ_{JC} 8–pin SOIC	+105°C/W
Reliability Information MTTF		254 Mhr

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Supply Voltage Range (V_{CC} – V_{EE})	+4.5V to +5.5V

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Electrical Characteristics

(V_{CC} = 0V, V_{EE} = −5V; unless otherwise specified).

Parameter	Condition	Typ +25°C	Min/Max +25°C (1)	Min/Max 0°C to +70°C (1)	Min/Max −40°C to +85°C (1)	Units
STATIC DC PERFORMANCE						
Supply Current, Loaded	150Ω @ 270 Mbps (2)	37	—	—	—	mA
Supply Current, Unloaded	(3)	34	28/45	26/47	26/47	mA
Output HIGH Voltage (V_{OH})	(3)	−1.7	−2.0/1.4	−2.0/1.4	−2.0/1.4	V
Output LOW Voltage (V_{OL})	(3)	−3.3	−3.6/3.0	−3.6/3.0	−3.6/3.0	V
Input Bias Current		10	30	50	50	µA
Output Swing	R_{EXT} = ∞ (3)	1.65	1.55/1.75	1.53/1.77	1.51/1.79	V
Output Swing	R_{EXT} = 10 kΩ	1.30	—	—	—	V
Common Mode Input Range Upper Limit		−0.7	−0.8	−0.8	−0.8	V
Common Mode Input Range Lower Limit		−2.6	−2.5	−2.5	–2.5	V
Minimum Differential Input Swing		200	200	200	200	mV
Power Supply Rejection Ratio (3)		26	20	20	20	dB
AC PERFORMANCE						
Output Rise and Fall Time	(3)(4)(2)	650	425/825	400/850	400/850	ps
Overshoot		5				%
Propagation Delay		1.0				ns
Duty Cycle Distortion		50				ps
Residual Jitter		25	—	—	—	ps_{pp}
MISCELLANEOUS PERFORMANCE						
Input Capacitance		1.0				pF
Output Resistance		10				Ω
Output Inductance		6				nH

(1) Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.
(2) Measured with both outputs driving 150Ω, AC coupled at 270 Mbps.
(3) Spec is 100% tested at +25°C
(4) Measured between the 20% and 80% levels of the waveform.

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Operation

INPUT INTERFACING

The CLC006 has high impedance, emitter-follower buffered, differential inputs. Single-ended signals may also be input. Transmission lines supplying input signals must be properly terminated close to the CLC006. Either A.C. or D.C. coupling as in Figure 4 or Figure 5 may be used. Figure 4, Figure 6 and Figure 7 show how Thevenin-equivalent resistor networks are used to provide input termination and biasing. The input D.C. common-mode voltage range is 0.8V to 2.5V below the positive power supply (V_{CC}). Input signals plus bias should be kept within the specified common-mode range. For an 800 mV_{P-P} input signal, typical input bias levels range from 1.2V to 2.1V below the positive supply.

Load Type	Resistor to V_{CC} (R1)	Resistor to V_{EE} (R2)
ECL, 50Ω, 5V, V_T=2V	82.5Ω	124Ω
ECL, 50Ω, 5.2V, V_T=2V	80.6Ω	133Ω
ECL, 75Ω, 5V, V_T=2V	124Ω	187Ω
ECL, 75Ω, 5.2V, V_T=2V	121Ω	196Ω
800 mV_{P-P}, 50Ω, 5V, V_T=1.6V	75.0Ω	154Ω
800 mV_{P-P}, 75Ω, 5V, V_T=1.6V	110Ω	232Ω
800 mV_{P-P}, 2.2KΩ, 5Ω, V_T=1.6V	3240Ω	6810Ω

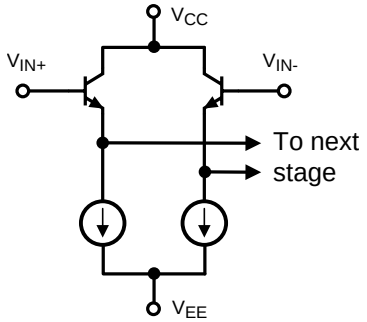


Figure 3. Input Stage

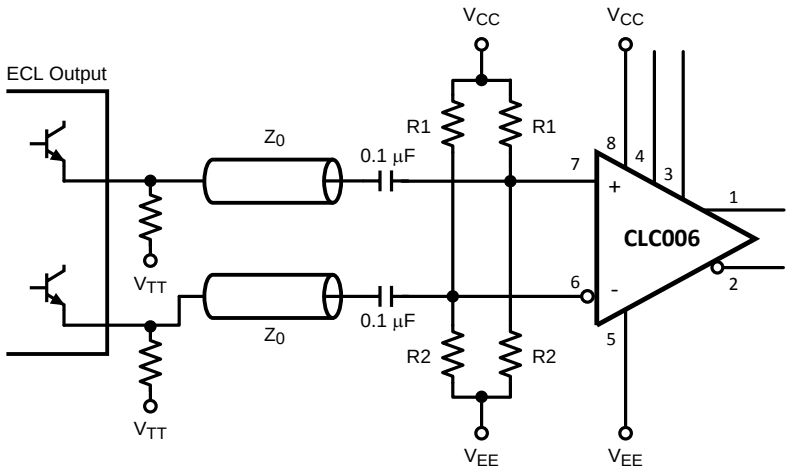


Figure 4. AC Coupled Input

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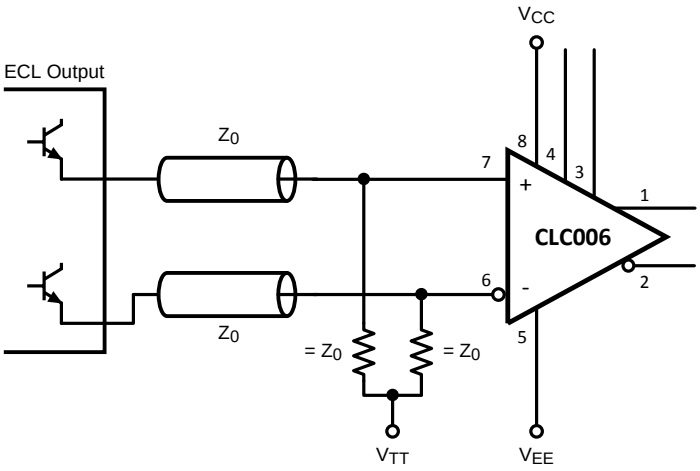


Figure 5. DC Coupled Input

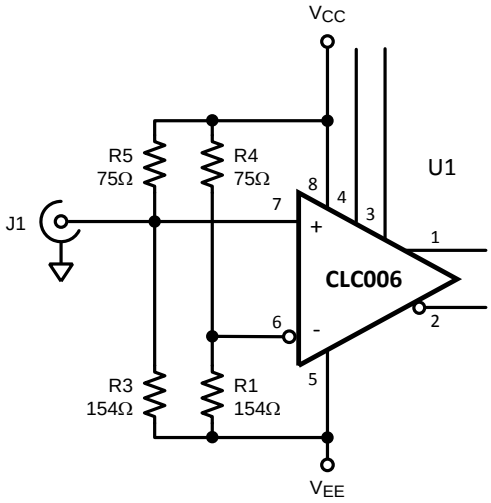


Figure 6. Single Ended 50Ω ECL input

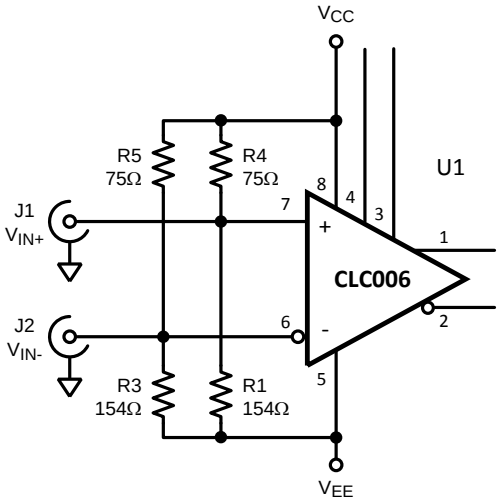


Figure 7. Differential 50Ω ECL Input

OUTPUT INTERFACING

The CLC006's class AB output stage, Figure 8, requires no standing current in the output transistors and therefore requires no biasing or pull-down resistors. Advantages of this arrangement are lower power dissipation and fewer external components. The output may be either D.C. or A.C. coupled to the load. A bandgap voltage reference sets output voltage levels which are compatible with F100K and 10K ECL when correctly terminated. The outputs do not have the same output voltage temperature coefficient as 10K. Therefore, noise margins will be reduced over the full temperature range when driving 10K ECL. Noise margins will not be affected when interfacing to F100K since F100K is fully voltage and temperature compensated.

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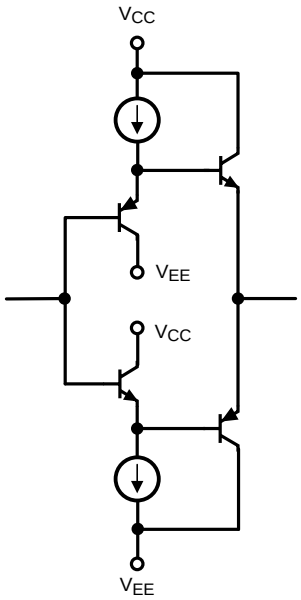


Figure 8. Output Stage

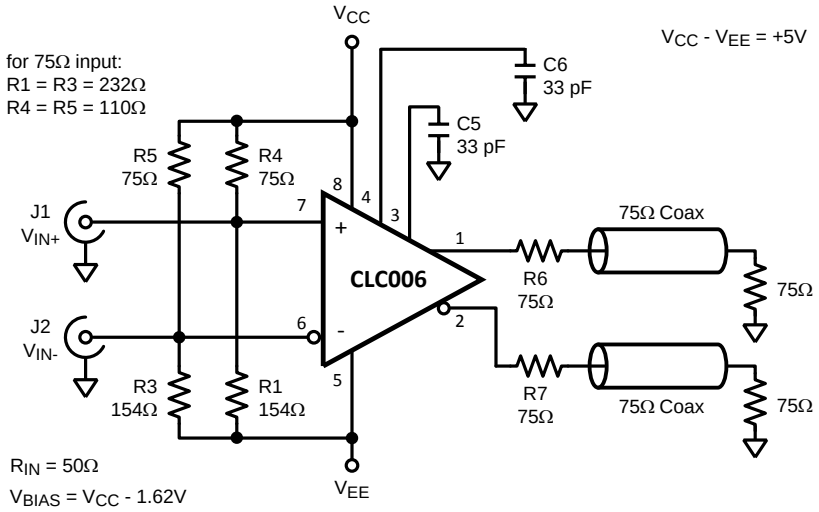


Figure 9. Differential Input DC Coupled Output

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OUTPUT AMPLITUDE ADJUSTMENT

The high and low output levels of the CLC006 are set by a circuit shown simplified in Figure 10. Output high and low levels may be set independently with external resistor networks connected between R_{EXT-H} (pin 3), R_{EXT-L} (pin 4) and the power supplies. The resistor networks affect the high and low output levels by changing the internally generated bias voltages, V_H and V_L. The nominal high and low output levels are V_{CC}−1.7V and V_{CC}−3.3V, respectively, when the pins R_{EXT-H} and R_{EXT-L} are left unconnected. Though the internal components which determine output voltage levels have accurate ratios, their absolute values may be controlled only within about ±15% of nominal. Even so, without external adjustment, output voltages are well controlled. A final design should accommodate the variation in externally set output voltages due to the CLC006's part-to-part and external component tolerances.

Output voltage swing may be reduced with the circuit shown in Figure 11. A single resistance chosen with the aid of the graph, Figure 12, is connected between pins 3 and 4. Output voltage swing may be increased with the circuit of Figure 13. Figure 14 is used to estimate a value for resistor R. Note that both of these circuits and the accompanying graphs assume that the CLC006 is loaded with the standard 150Ω. Be aware that output loading will affect the output swing and the high and low levels. It may be necessary to empirically select resistances used to set output levels when the D.C. loading on the CLC006 differs appreciably from 150Ω.

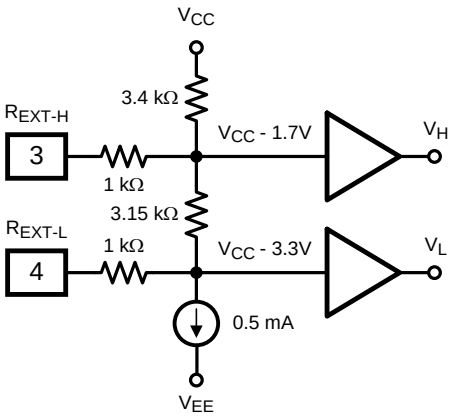


Figure 10. Equivalent Bias Generation Circuit

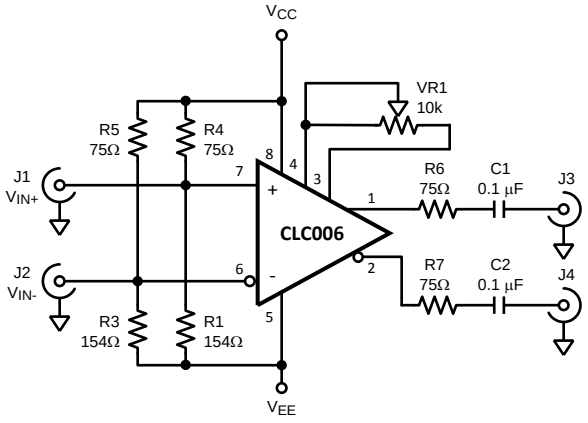


Figure 11. Differential Input Reduced Output

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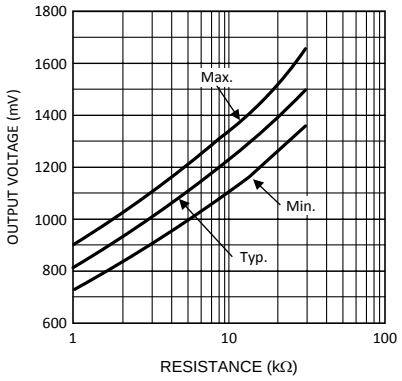


Figure 12. Resistance Pins 3 to 4 vs Output Voltage Reduced Output @ 150Ω Load

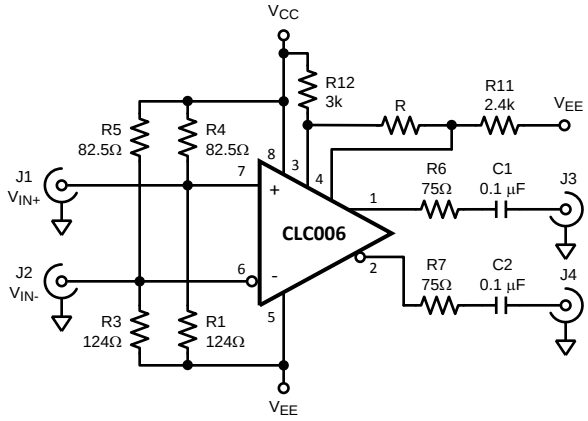


Figure 13. Differential Input Increased Output

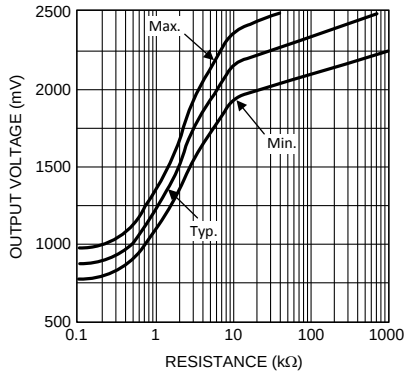


Figure 14. Resistance Pins 3 to 4 vs Output Voltage Increased Output @ 150Ω Load

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OUTPUT RISE AND FALL TIMES

Output load capacitance can significantly affect output rise and fall times. The effect of load capacitance, stray or otherwise, may be reduced by placing the output back-match resistor close to the output pin and by minimizing all interconnecting trace lengths. Figure 15 shows the effect on risetime of parallel load capacitance across a 150Ω load.

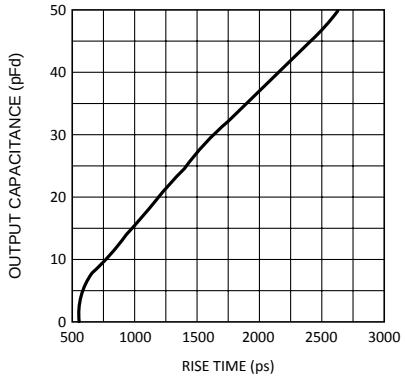


Figure 15. Rise Time vs C_L

PCB Layout Recommendations

Printed circuit board layout affects the performance of the CLC006. The following guidelines will aid in achieving satisfactory device performance.

- Use a ground plane or power/ground plane sandwich design for optimum performance.
- Bypass device power with a 0.01 µF monolithic ceramic capacitor in parallel with a 6.8 µF tantalum electrolytic capacitor located no more than 0.1” (2.5 mm) from the device power pins.
- Provide short, symmetrical ground return paths for:
  - inputs,
  - supply bypass capacitors and
  - the output load.
- Provide short, grounded guard traces located
  - under the centerline of the package,
  - 0.1” (2.5 mm) from the package pins
  - on both top and bottom of the board with connecting vias.

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REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	9

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLC006BM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	CLC00 6BM>D	Samples
CLC006BMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	CLC00 6BM>D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

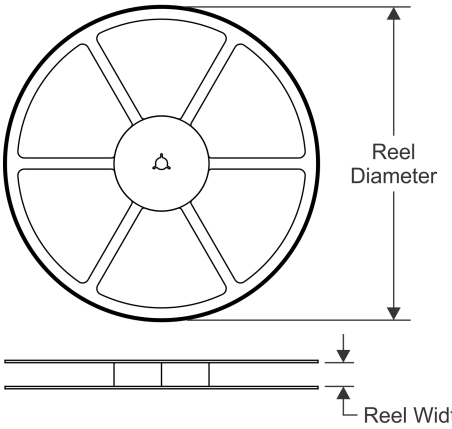
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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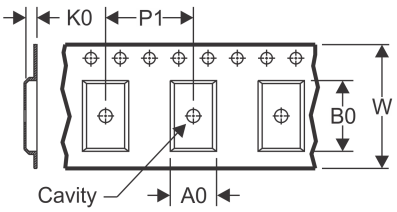
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

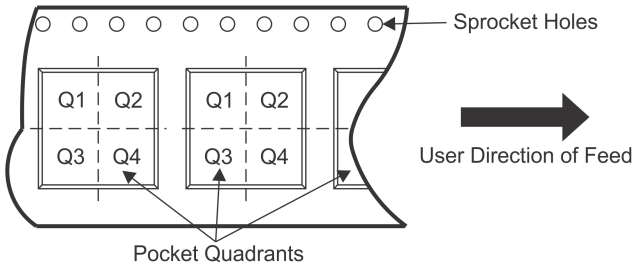


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

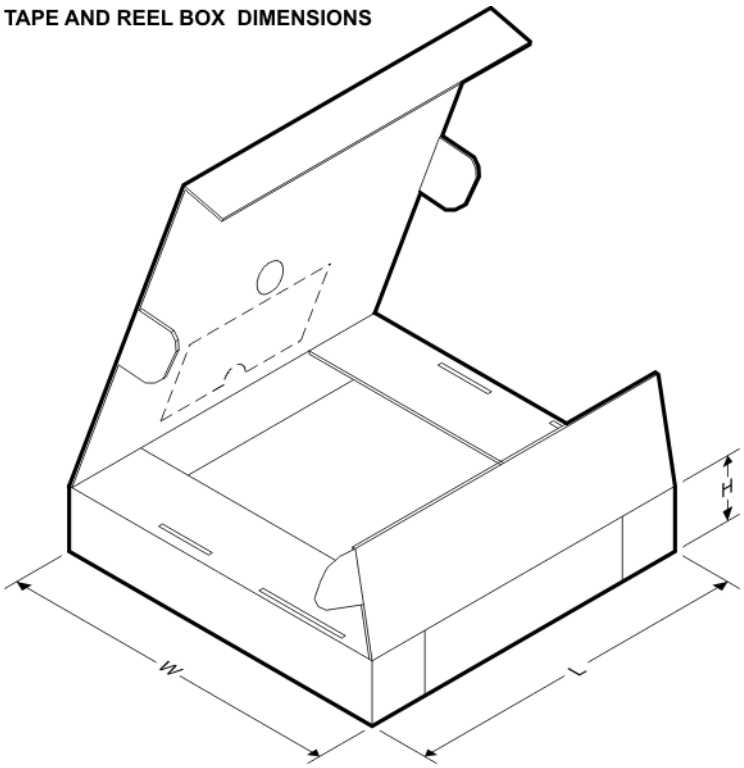
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

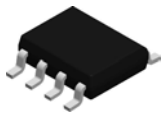
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLC006BMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLC006BMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

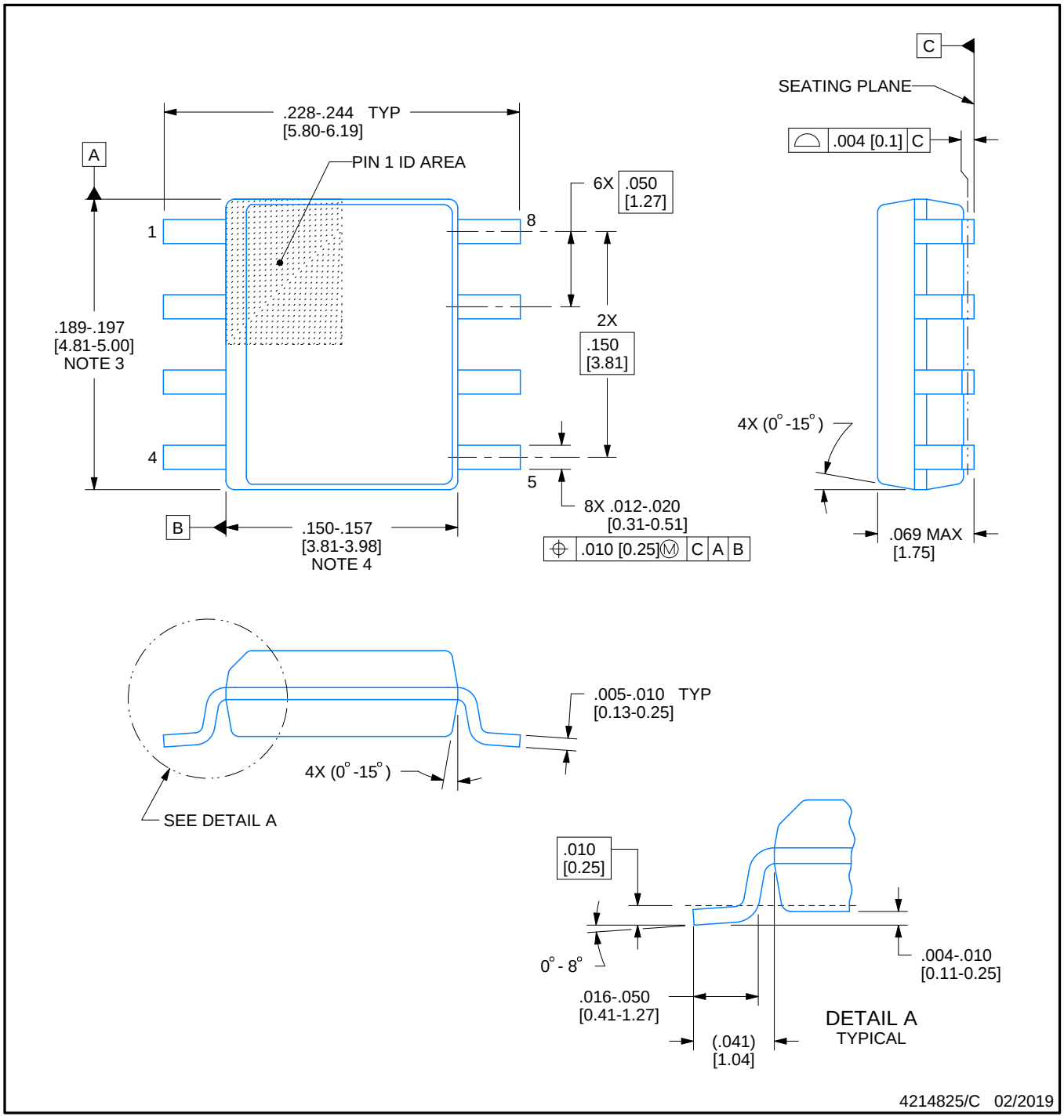


PACKAGE OUTLINE

D0008A

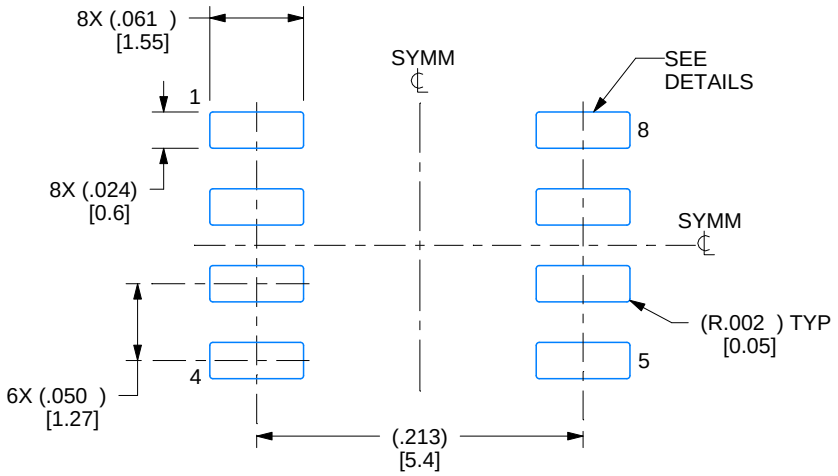
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

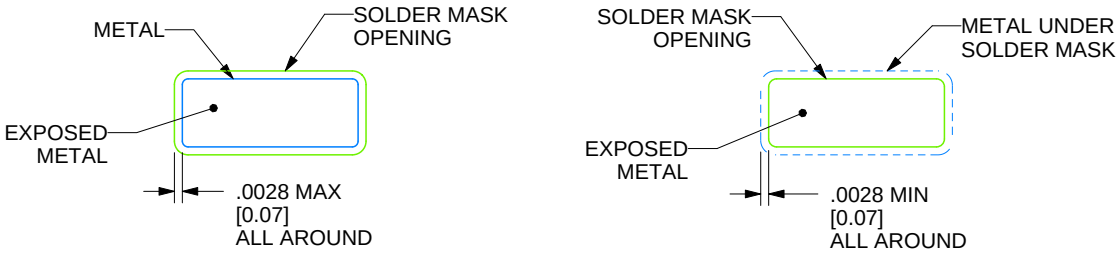


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

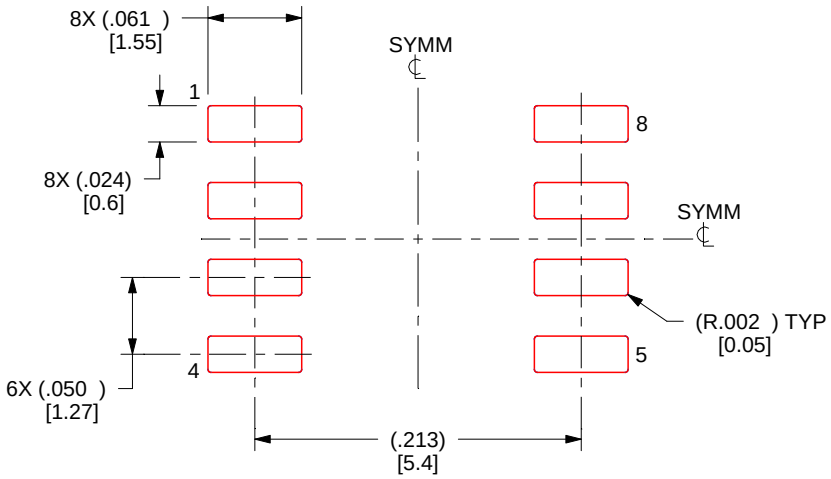
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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