CL88020

Sequential Linear LED Driver with Four Taps

Features

- Optimized for 120 V_{AC} Nominal Input Voltage
  - 120 V_{AC} ± 15% input voltage
- Targeted for 8.5W Output Power
- Programmable Overtemperature Protection
  - Provides Gradual Reduction in Light Output with Increasing Temperature
- Active Line Regulation
  - Provides Fairly Constant Output Power over Variations in AC Line Voltage
  - Typical Line Regulation of –12% to +0%
- Four Taps with Two Current Set Resistors
  - Allows Optimization of THD
- Optional Reduced Light Output Ripple
  - Provides Continuous Power to the LED
  - Eliminates Strobing
  - Uses an External Ceramic Storage Capacitor
- TRIAC Dimmer Compatible
- Available in a Thermally Enhanced 8-Lead SOIC Package with Heat Slug
  - Larger Creepage Distances between High Voltage and Low Voltage Pins

Applications

- LED Lamps
- LED Lighting Fixtures

Description

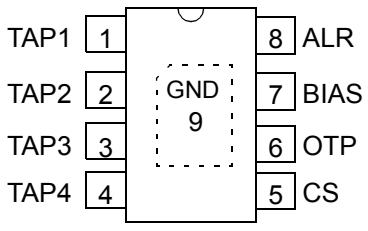
The CL88020 LED Driver Integrated Circuit (IC) is an off-line sequential linear LED driver designed to provide 8.5W of LED power from a 120 V_{AC} nominal input voltage.

CL88020 is designed to drive a long string of inexpensive, low-current LEDs directly from the AC mains. A basic driver circuit consists of Microchip Technology Inc.'s CL88020 LED driver IC, six resistors and a bridge rectifier. Two to four additional components are optional for various levels of transient protection, also with a low-cost NTC to assure remote overtemperature protection (OTP). No capacitors, EMI filters, or power factor correction circuits are needed unless the optional reduced light output ripple feature is desired.

A string of series/parallel LEDs is tapped at four locations. Four linear current regulators sink current at each tap through a single control point and are sequentially turned on and off. High efficiency is achieved by shutting off upstream regulators when downstream regulators achieve regulation. This makes controlling overall input current easier than trying to control multiple current paths, thereby tracking the input sine wave voltage. CL88020 uses a self-commutation technique using only the tap currents themselves; this technique inherently provides smooth transitions from one regulator to the next, without relying on tap voltages or the rectified AC to coordinate the transitions.

PIN DIAGRAM

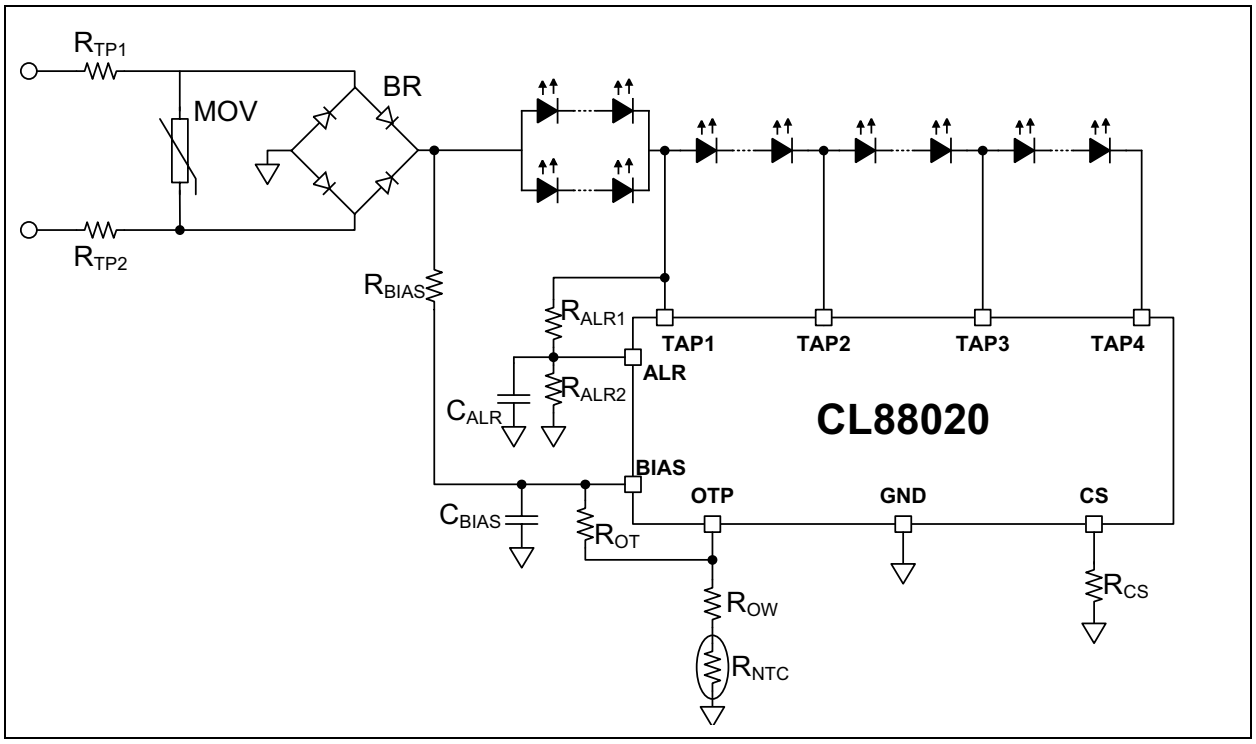
CL88020
8-Pin SOIC



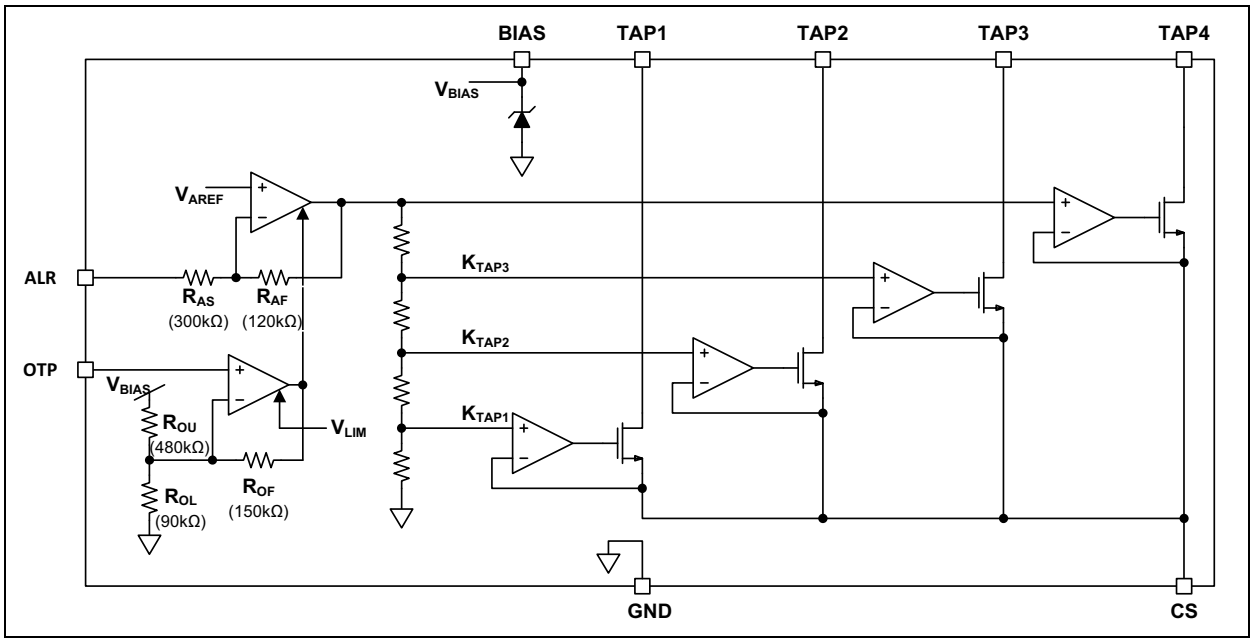
* Includes Exposed Thermal Pad (EP); see Table 2-1

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TYPICAL APPLICATION CIRCUIT



INTERNAL BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

TAP_{1-4} to GND (non-conducting) ..... –0.5V to +352V

OTP, ALR, CS to GND .....–0.3V to (BIAS + 0.5V)

BIAS to GND .....–0.3V to 14V

Maximum current into BIAS pin..... 10 mA

ESD Rating (OTP, ALR, CS, BIAS, GND pins) Human Body Model .....750 V

Operating junction temperature ..... –40°C to +125°C

Storage temperature ..... –65°C to +150°C

Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. CL88020 is susceptible to electrostatic discharge (ESD).

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all specifications are for $T_A = T_J = +25°C$. BIAS = 12V. V_{TAP} = 20V, ALR pin open, OTP = 5V unless otherwise noted. Boldface specifications apply over the full temperature range $T_A = T_J = –15°C$ to +95°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply (P_{VDD})						
Maximum TAP current capability for TAP 1	$I_{TAP,max}$	105	—	—	mA	R_{SET} = 6.19Ω
Maximum TAP current capability for TAP 2		110	—	—		R_{SET} = 7.50Ω
Maximum TAP current capability for TAP 3		130	—	—		
Maximum TAP current capability for TAP 4		130	—	—		
TAP on resistance for TAP 1	R_{TAP}	—	—	67	Ω	V_{TAP} = 6V
TAP on resistance for TAP 2		—	—	56		
TAP on resistance for TAP 3		—	—	56		
TAP on resistance for TAP 4		—	—	52		
Voltage at BIAS pin	V_{BIAS}	12.0	12.5	13.64	V	I_{BIAS} = 0.8 - 5 mA
Quiescent current consumption	$I_{BIAS,Q}$	—	550	750	µA	Note 1
Limiting current (measured at TAP 4)	I_{LIM}	12.96	15.25	17.54	mA	V_{ALR} = 0V, R_{SET} = 100Ω
Regulated Tap current for TAP 4	I_{TAP4}	121.1	127.5	133.9	mA	R_{SET} = 10Ω;
TAP 3 to TAP 4 current ratio	K_{TAP3}	0.883	0.929	0.975		
TAP 2 to TAP 4 current ratio	K_{TAP2}	0.747	0.786	0.825		
TAP 1 to TAP 4 current ratio	K_{TAP1}	0.542	0.571	0.600		
Self-commutation (TAP 1 to TAP 2)	$\Delta V_{CS(REG)}$	10	—	—	mV	Rset = 100Ω (V_{CS} at V_{TAP2} = 20V) - (V_{CS} at V_{TAP1} = 20V)
Self-commutation (TAP 2 to TAP 3)		10	—	—	mV	Rset = 100Ω (V_{CS} at V_{TAP3} = 20V) - (V_{CS} at V_{TAP2} = 20V)
Self-commutation (TAP 3 to TAP 4)		10	—	—	mV	Rset = 100Ω (V_{CS} at V_{TAP4} = 20V) - (V_{CS} at V_{TAP3} = 20V)

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all specifications are for $T_A = T_J = +25°C$. BIAS = 12V. V_{TAP} = 20V, ALR pin open, OTP = 5V unless otherwise noted. Boldface specifications apply over the full temperature range $T_A = T_J = –15°C$ to +95°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
TAP 1 to TAP 2 cross regulation	X-Reg	-2	—	2	mV	Rset = 100Ω I_{TAP2} = 2 mA V_{TAP1} = 20V
TAP 2 to TAP 3 cross regulation		-2	—	2	mV	Rset = 100Ω I_{TAP3} = 2 mA V_{TAP2} = 20V
TAP 3 to TAP 4 cross regulation		-2	—	2	mV	Rset = 100Ω I_{TAP4} = 2 mA V_{TAP3} = 20V
Nominal TAP 4 current	$I_{LR,nom}$	—	12.75	—	mA	Rset = 100Ω V_{ALR} = 1.275V V_{TAP4} = 20V
TAP4 current to $I_{LR,NOM}$ ratio	$I_{LR,HI}$	0.801	0.843	0.885		Rset = 100Ω V_{ALR} = 1.776V V_{TAP4} = 20V
TAP4 current to $I_{LR,LO}$ ratio	$I_{LR,LO}$	1.073	1.129	1.186		Rset = 100Ω V_{ALR} = 0.863V V_{TAP4} = 20V
OPT current limit	OTP	9.01	10.60	12.19	mA	V_{OTP} = 1.6V; R_{SET} = 100Ω V_{TAP4} = 20V

Note 1: Does not include the bias current.

TABLE 1-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_J	-40°C	—	+125°C	°C	Note 1
Storage Temperature Range	T_A	-65°C	—	+150°C	°C	
Package Thermal Resistances						
Thermal Resistance, 8LD-SOIC	θ_{JC}	—	+8°C	—	°C/W	Note 2

Note 1: The Operating Temperature Range is specified at the junction. The junction temperature must be computed using the thermal resistance (TR) from junction-to-case, and the case-to-ambient TR of the PCB design.

2: Thermal resistance is measured from junction to bottom metal slug.

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2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN DESCRIPTION

Pin #	Name	Description
1	TAP1	Drives the most upstream LED string
2	TAP2	Drives the first and second LED strings
3	TAP3	Drives the first, second and third LED strings
4	TAP4	Drives all 4 LED strings
5	CS	Used to set the currents in the Taps
6	OTP	Provides remote Over-Temperature protection.
7	BIAS	Provides power to the IC using an internal shunt regulator. It is recommended to be bypassed with a low ESR ceramic capacitor (at least 1 µF)
8	ALR	An external resistive voltage divider and capacitor provide line regulation for the TAP currents
9	GND	Regulator ground

2.1 TAP1 Pin

Open drain power FET connection to the first/top LED string.

2.2 TAP2 Pin

Open drain power FET connection to the second LED string.

2.3 TAP3 Pin

Open drain power FET connection to the third LED string.

2.4 TAP4 Pin

Open drain power FET connection to the fourth/bottom LED string.

2.5 Current Set Pin (CS)

A resistor from this pin to ground sets the LED string current.

2.6 Over-temperature Protection Pin (OTP)

This input is connected to a resistor/NTC-thermistor combination to reduce the LED current when the temperature becomes too high.

2.7 BIAS Pin

An input pin to provide voltage to the chip. The BIAS pin is the input to a shunt regulator and must be fed by a current source, not a fixed voltage.

2.8 Active Line Regulation Pin (ALR)

This input pin is connected to an RC network to sense the input main voltage and regulate the LED string current against variations in AC input voltage.

2.9 Ground Terminal (GND)

Reference ground for all input voltages.

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3.0 FUNCTIONAL DESCRIPTION

3.1 Introduction

The CL88020 Sequential Linear LED Driver is designed to drive a long string of inexpensive, low-current LEDs directly from the AC mains. A string of series/parallel LEDs is tapped at four locations. Four linear current regulators sink current at each tap through a single control point and are sequentially turned on and off.

This **IC** is targeted to drive a string of LEDs from a nominal 120 V_{AC} input voltage and provide 8.5W of output power.

It has an internal line regulation circuit to regulate the output power as the line voltage changes from minimum to maximum. It also includes a remote over-temperature protection which allows thermal de-rating of the output power using a remote NTC to sense the LED temperature.

3.2 Principle of Operation

The CL88020 employs a very simple method of implementing single-point control and self-commutation, as shown in Figure 3-1. The single current sense resistor to ground (R_{CS}) comprises single-point control. Each taps' error amplifier shares this single control point, although only one err amp is active at any one time.

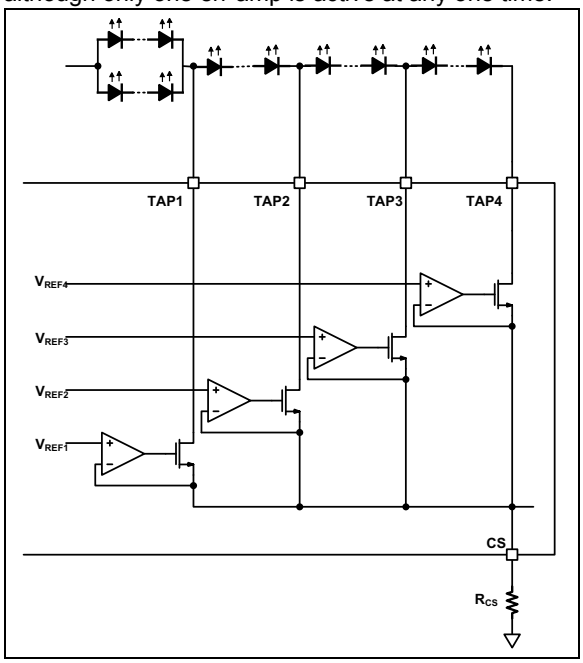


FIGURE 3-1: *Tap Commutation.*

Each current regulator has its own reference voltage, derived from a resistive voltage divider such that:

$$V_{REF4} > V_{REF3} > V_{REF2} > V_{REF1}$$

Initially, V_{CS} is at 0V, causing all the current regulators to be turned on but not conducting. Once the rectified AC rises high enough to forward bias the first LED string segment, the first current regulator begins conducting. Eventually it achieves regulation. At this point V_{REF1} and V_{CS} are in equilibrium. As the rectified AC continues to rise, the next LED segment becomes forward biased. Since the second regulator's reference voltage (V_{REF2}) is higher than V_{CS}, the second regulator is already on and begins conducting (although not regulating), injecting current (I_{TAP2}) into the single control point., raising the V_{CS} voltage. The first regulator responds to the increase in V_{CS} by reducing I_{TAP1} such that V_{CS} remains equal to V_{REF1}.

EQUATION 3-1:

$$I_{TAP1} = \frac{V_{REF1}}{R_{CS}} - I_{TAP2}$$

I_{TAP1} continues to decrease as I_{TAP2} increases. When the rectified AC rises sufficiently for the second regulator to achieve regulation, V_{CS} increases to be equal with V_{REF2}. With V_{CS} now greater than V_{REF1}, the first regulator is effectively shut off and the second regulator takes over. This repeats for the other taps and also works in reverse as the rectified AC passes the peak and begins decreasing.

This simple self-commutating mechanism and single-point control automatically sequences the current regulators and assures smooth tap-to-tap transitions.

3.2.1 ACTIVE LINE REGULATION (ALR)

Without compensating for line voltage variations, as the AC voltage increases, downstream LED segments become active. In addition, the dwell time at the higher tap currents increases as AC voltage goes up. This causes brightness to increase with AC voltage, resulting in poor line regulation.

The ALR circuit maintains fairly constant output power over variations in AC line voltage. It is not a closed loop system that directly monitors and corrects output power. Instead it monitors the voltage applied to the LED string and uses it to adjust the reference voltage provided by the OTP circuit. The circuit used for achieving the active line regulation is shown in Figure 3-2.

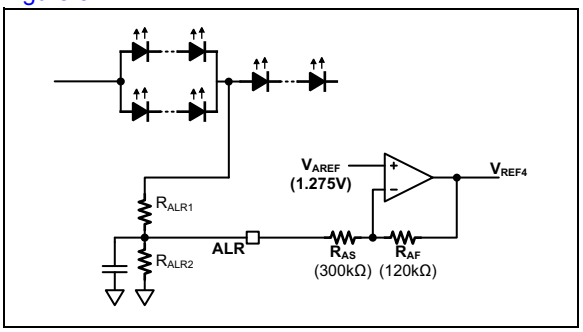


FIGURE 3-2: *ALR Circuit.*

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Under normal operation (OTP not activated) the OTP limiting voltage is essentially the reference voltage used to set the tap currents. The ALR circuit adjusts this voltage up or down to compensate for variations in the AC line voltage as represented by the voltage at the ALR pin.

EQUATION 3-2:

$$V_{REF4} = 1.275V - \left(\frac{V_{ALR} - 1.275V}{300k\Omega} \cdot 120k\Omega\right)$$

The external resistor divider at the ALR pin is usually chosen such that the average voltage at the pin is 1.275V at nominal 120 V_{AC} input. The ALR divider is connected after the first LED segment to increase its sensitivity to changes in the AC line voltage.

The function of the limiter circuit is three-fold. Except during OTP, the limiting voltage is fixed. First, during the initial application of power, the ALR filter capacitor (C_{ALR}) is at 0V. This would result in high LED current until C_{ALR} charges up. Without a limiter, this would cause a bright flash at turn-on. The second purpose of the limiter is during dimming, where the average ALR voltage will be low, causing the LED drive current to be high. This defeats the dimmer and could result in excessive currents. Lastly, during an overtemperature condition, the OTP circuit gradually lowers the limiting voltage from its fixed value. This reduces the power applied to the LEDs, lowering their temperature until an equilibrium is established.

3.2.2 OVERTEMPERATURE PROTECTION (OTP)

OTP uses an inexpensive, external NTC thermistor to remotely sense LED temperature. The thermistor can be located in close proximity to the LEDs, providing near-direct LED temperature monitoring. The OTP temperature is adjustable via selection of NTC resistance. It is essential that OTP operate linearly, gradually reducing output power as temperature increases. The thermistor is arranged in a full-bridge configuration with the active arm consisting of the NTC and a discrete resistor to V_{BIAS} (Figure 3-3). The passive arm consists of internal resistors. The thermistors' resistance versus temperature curve asymptotically approaches 0Ω as temperature rises. To provide a well-defined window between the threshold temperature and the extinguishing temperature, a small segment of the thermistors' resistance-temperature curve must be used.

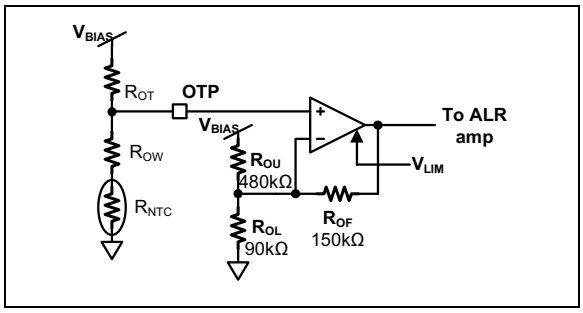


FIGURE 3-3: *OTP Equivalent Circuit.*

R_{OF} and the parallel combination of R_{OU} and R_{OL} determine OTP gain and set the width of the OTP window — the higher the gain, the narrower the window. Offset is determined by the passive arm of the bridge and sets the location of the OTP window along the temperature axis.

If OTP is unused, the OTP pin should be connected to V_{DD}.

The output of the OTP amplifier (which is used as a limit for the ALR amplifier) can be expressed as:

EQUATION 3-3:

$$V_{REF4} = R_{OF} \cdot \left[V_{OTP} \cdot \left(\frac{1}{R_{OF}} + \frac{1}{R_{OU}} + \frac{1}{R_{OL}}\right) - \frac{V_{BIAS}}{R_{OU}}\right]$$

$$= (2.979 \cdot V_{OTP} - (0.3125 \cdot V_{BIAS}))$$

Note that in the above equation, it is assumed that the input voltage is at nominal value and there is no adjustment to the reference due to the ALR circuit.

The output of the OTP amplifier is internally clamped to 1.575V, which corresponds to a voltage of 1.787V at the OTP pin when V_{BIAS} is 12.0 volts. As the voltage at the OTP pin decreases to 1.686V, the output of the OTP amplifier falls to 1.275V. It is at this point, the OTP circuit starts modifying the TAP currents and causes thermal derating.

Using two fixed resistors and one NTC, both the breakpoint and the slope of the derating curve can be set independently.

For example, consider a case with a breakpoint of 85°C with a derating curve such that the LED driver is at 20% of full power at 110°C. So, the VREF4 voltages at 85°C and 110°C are 1.275V and 0.255V respectively. The NTC thermistor used is a 470 kΩ, with a Bvalue of 4500K. The NTC resistance at a given temperature (Tc, expressed in °C) can be expressed as:

EQUATION 3-4:

$$R_{NTC,\,Tc} = R_{NTC,\,25C} \cdot e^{-B \cdot \left(\frac{1}{298K} - \frac{1}{Tc + 273}\right)}$$

Using Equation 3-4, the corresponding NTC resistances at 85°C and 110°C are 33.4 kΩ and 14.2 kΩ. Using these NTC resistance values, R_{OW} and R_{OT} can then be computed. The final set of values that are computed assuming 12.0 volts V_{BIAS} are provided in the Table 3-1.

TABLE 3-1: OVERTEMPERATURE PROTECTION

Parameter	25C	85C	110C
R_{OT}	511 kΩ	511 kΩ	511 kΩ
R_{OW}	49.9 kΩ	49.9 kΩ	49.9 kΩ
R_{NTC}	470 kΩ	33.4 kΩ	14.2 kΩ
V_{OTP}	6.05V	1.68V	1.34V
V_{REF4}	1.575V	1.262V	0.234V

3.2.3 RIPPLE REDUCTION (OPTIONAL)

Low output ripple is achieved using a capacitor and four diodes. The capacitor may one or more paralleled ceramic capacitors or a single electrolytic. Multiple ceramic capacitors may be needed due to their poor voltage coefficient. The four diodes may be obtained in a single small package.The LED and rectifier arrangement is shown in Figure 3-4.

With this method all currents, including ripple capacitor charging and discharging currents, are controlled, passing through the same single control point. This allows the input current wave-shape to be maintained and avoids peak-charging the ripple-reduction capacitor.

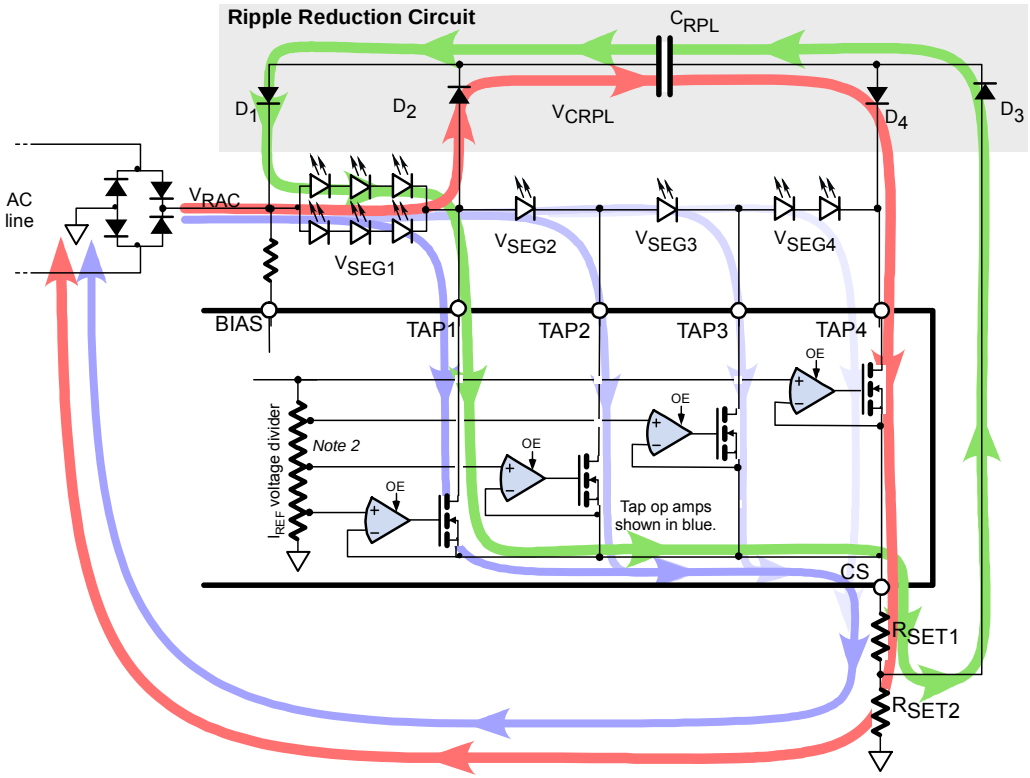


FIGURE 3-4: *Ripple Reduction Circuit.*

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The CL88020 with the ripple reduction circuit operates in four phases: recharge, hold-up, direct and under certain conditions, idle. Note that all active current paths include Segment 1, assuring uninterrupted light output during all phases of operation, excluding the idle phase.

Recharge (red path)

Recharging of the ripple capacitor (C_{RPL}) occurs when ($V_{RAC} – V_{SEG1}$) > V_{CRPL}. The maximum voltage that C_{RPL} can be charged to is:

$$V_{CRP(max)} = V_{SEG2} + V_{SEG3} + V_{SEG4}$$

The numbers of LEDs for each segment must be chosen carefully so as not to exceed C_{RPL}'s voltage rating while at the same time allowing C_{RPL} to charge up to a voltage sufficient to drive at least SEG1. To provide continuous light output, the recharge path must include LEDs.

Hold-Up (green path)

When the rectified AC falls below V_{CRPL}, the capacitor takes over, supplying the LEDs. The discharge path flows through R_{SET1} only. Since this is lesser sense resistance than for the other current paths, the current for the hold-up phase will be higher. This allows for normal currents to be drawn from the AC line to better track the input voltage sine wave while allowing a higher current during the hold-up interval.

Direct (purple paths)

When V_{CRPL}< V_{RAC} < (V_{CRPL} + V_{SEG1}), the LEDs are supplied directly from the AC line. The window when the direct phase is active is determined by V_{SEG1}.

Idle (no path)

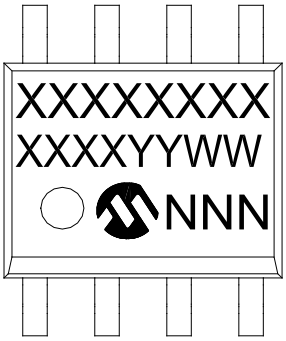
At low AC line voltages, there is not enough voltage to charge C_{RPL} sufficiently to power SEG1 and strobing will occur. Also, strobing will occur if C_{RPL} is too small.

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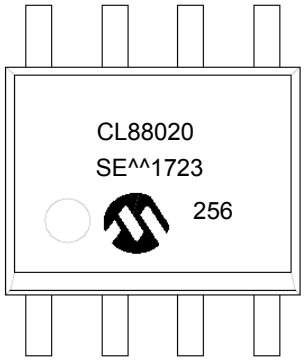
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Pin SOIC



Example



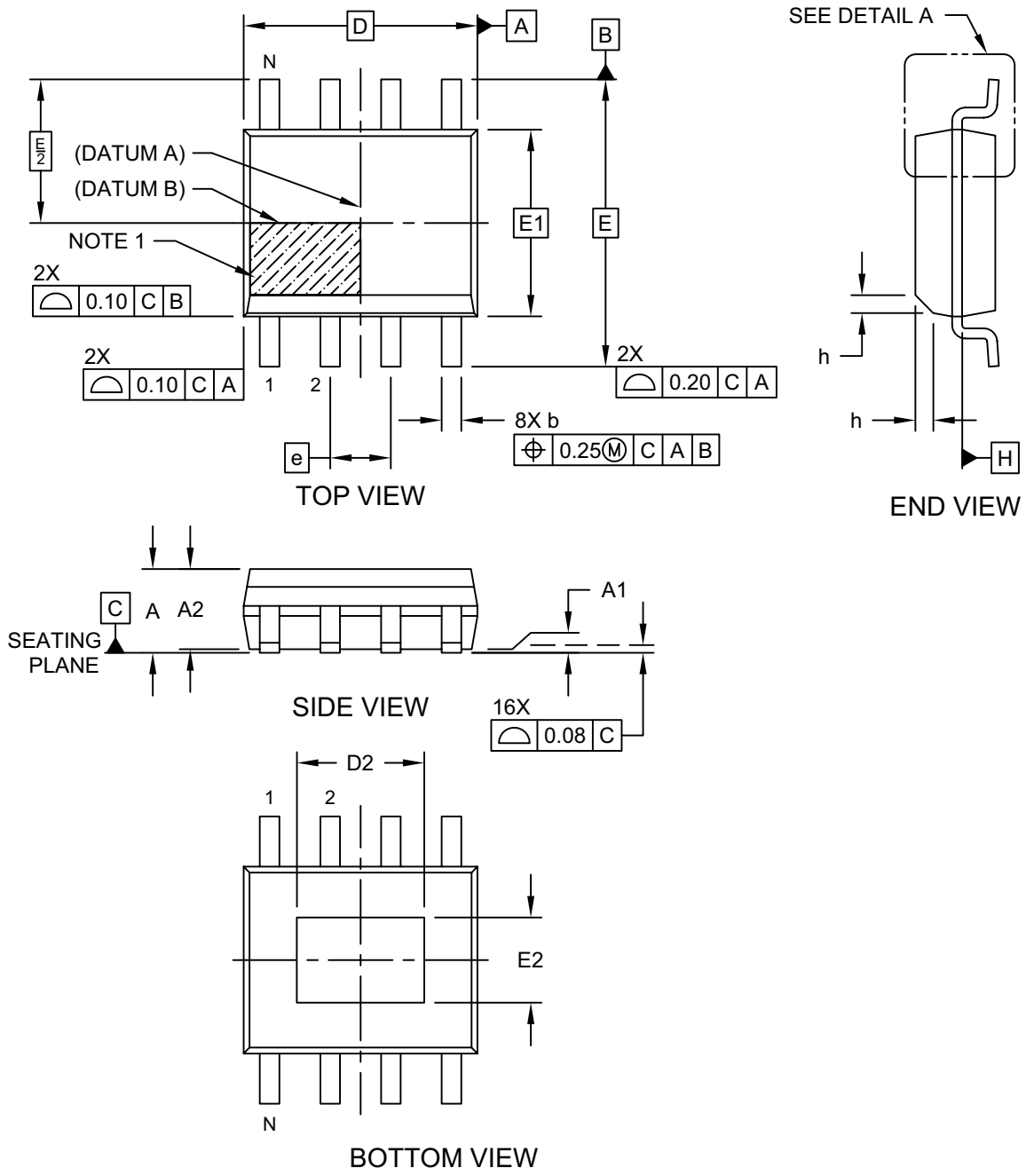
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

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8-Lead Small Outline Integrated Circuit (5DX) - .150 In. (3.90 mm) Body [SOIC] With 3.30x2.41 mm Exposed Pad

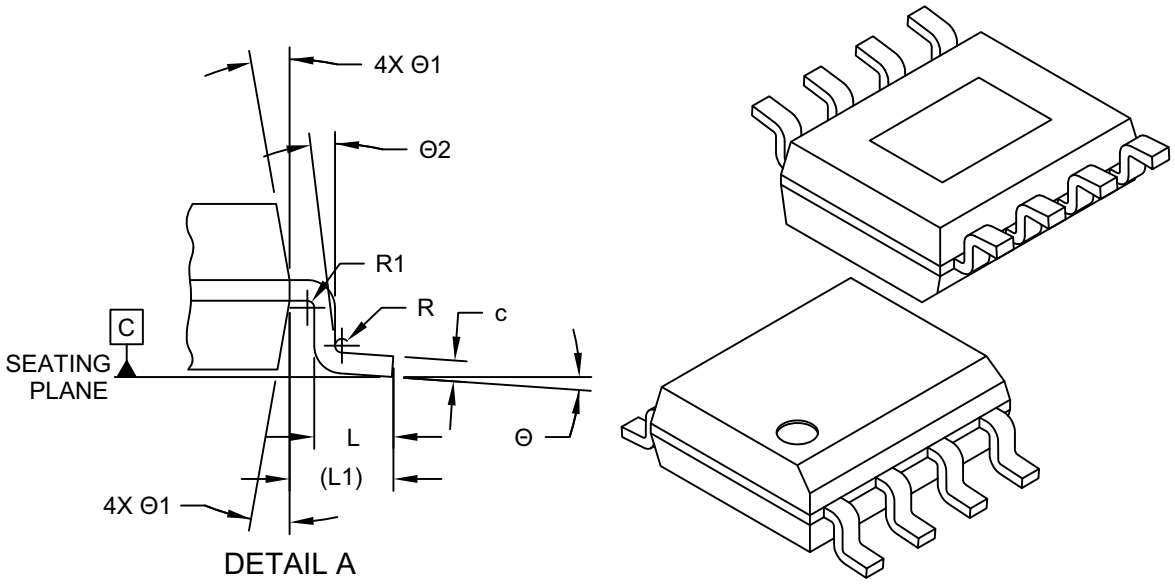
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-419A Sheet 1 of 2

8-Lead Small Outline Integrated Circuit (5DX) - .150 In. (3.90 mm) Body [SOIC] With 3.30x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.70
Molded Package Thickness	A2	1.25	1.45	-
Standoff §	A1	0.00	-	0.15
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Exposed Pad Width	E2	1.78	-	-
Exposed Pad Length	D2	2.67	-	-
Chamfer (Optional)	h	0.15	-	-
Foot Length	L	0.40	0.71	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Foot Angle	Θ	0°	-	8°
Lead Angle	Θ2	0°	-	-
Mold Draft Angle	Θ1	0°	-	15°

Notes:

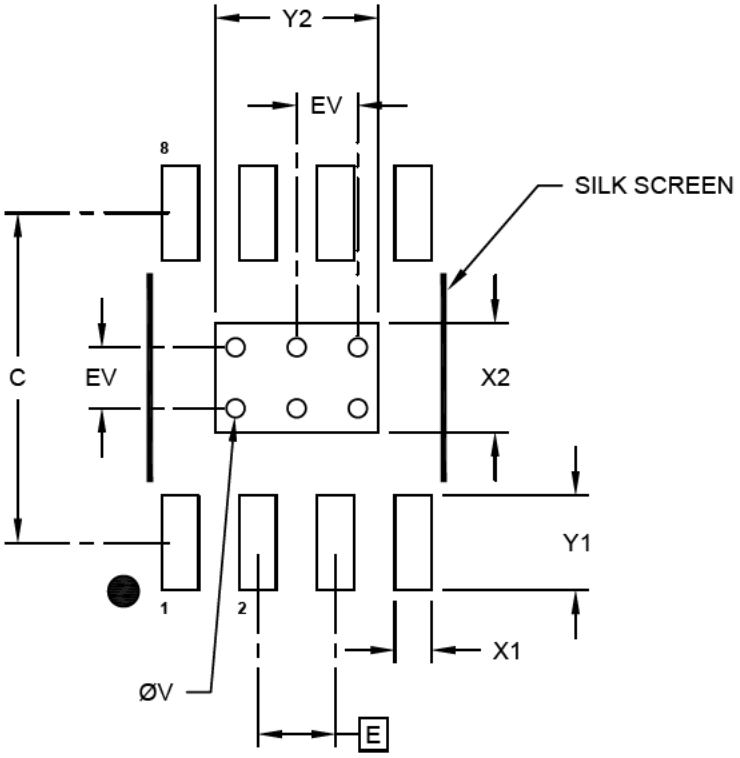
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-419A Sheet 2 of 2

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RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Width	X2	1.78		
Optional Center Pad Length	Y2	2.67		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X20)	X1			0.60
Contact Pad Length (X20)	Y1			1.55
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2419A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (May 2017)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-	X	-	XX
	Device	Tape and Reel		Temperature Range	Package

Device:	CL88020	=	Sequential Linear LED Driver with 4 Taps
Tape and Reel Option	T	=	Tape and Reel
Temperature Range	E	=	-40°C to +125°C (Extended)
Package:	SE	=	

Examples:

a) CL88020T-E/SE: Sequential Linear LED Driver with 4 Taps

NOTES:

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