CF001 Series GaAs Pseudomorphic HEMT and MESFET Chips



- Super Low Noise: 0.8 dB at 12 GHz
- High Gain: Usable to 44 GHz
- P_{1dB} Power: Up to +19 dBm
- Active Layers Include: Pseudomorphic HEMT, Epitaxial and Ion Implanted
- Wafer Qualification Procedure
- Customer Wafer Selection Available

Celeritek CF001 Series Chips

Celeritek CF001 Series chips are GaAs-based transistors which include the CF001-01, CF001-02 and CF001-03 models. They are 300 µm gate width, sub-half-micron gate length GaAs devices with Celeritek's proprietary Silicon Nitride passivation.

Celeritek's Wafer Qualification Procedure for CF001 Series FETs consists of DC, RF and reliability testing of both individual die and generic 6 to 18 GHz amplifier modules.

The CF001-01 provides high gain up to 26 GHz. It is suitable for general purpose and driver amplifier applications with up to +19 dBm power from a single FET. These devices can also be used in oscillator applications.

The CF001-03 model is Celeritek's state-of-the-art low noise and high associated gain GaAs Pseudomorphic HEMT device. It is suitable for narrow and wide band low noise and high gain amplifiers up to 40 GHz. Its rugged construction allows it to withstand the same input power as conventional MESFETs.

All CF001 Series devices are available in chip form and are suitable for airborne, shipboard and ground-based equipment. Screening includes MIL-STD-750 Class B, Class S and commercial screening. These devices are also available in packaged form. Please consult the CFB001 Series and CFA001 Series data sheets or contact the factory for further information.

CELERITEK

Mimix Broadband, Inc., 10795 Rockley Rd., Houston, Texas 77099
Tel: 281.988.4600 Fax: 281.988.4615 mimixbroadband.com

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CF001 Series GaAs Chips

Specifications (T_A = 25°C)				CF001-01			CF001-02			CF001-03		
Active Layer				Ion Implanted			Epitaxial			Pseudomorphic HEMT		
Symbol	**Parameters and Conditions**	**Frequency (GHz)**	**Units**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
NF_{opt}	Optimum Noise Figure V_{DS} = 3.0 V, I_{DS} = 15 mA	12.0	dB		1.6	2.4		1.2	1.8		0.8	1.2
Ga	Gain at NF_{opt} V_{DS} = 3.0 V, I_{DS} = 15 mA	12.0	dB	7.5	8.5		8.5	9.5		9.5	10.5	
$\|S_{21}\|^2$	50 Ohm Insertion Gain V_{DS} = 6.0 V, I_{DS} = 40 mA	2.0 10.0 18.0	dB dB dB		13.0 9.5 6.0			14.0 10.5 7.0			15.0 11.5 8.0	
P_{1dB}	Power Output @ 1 dB GC V_{DS} = 6.0 V, I_{DS} = 40 mA	12.0	dBm		19.0			17.0			17.0	
g_m	Transconductance V_{DS} = 3.0 V, V_{GS} = 0 V		mS		60			75			90	
I_{DSS}	Drain Current V_{DS} = 3.0 V, V_{GS} = 0 V		mA	40	60	120	30	60	120	30	60	120
V_P	Pinchoff Voltage V_{DS} = 3.0 V, I_{DS} = 1 mA		Volts	-0.7	-1.3	-2.5	-0.5	-1.3	-2.5	-0.5	-1.3	-2.5
BV_{GD}	Breakdown Voltage, Gate-Drain I_{GD} = 100 µA		Volts	-5.5	-8.0		-5.5	-8.0		-5.5	-8.0	
R_{th}	Thermal Resistance		°C/W		150			150			150	

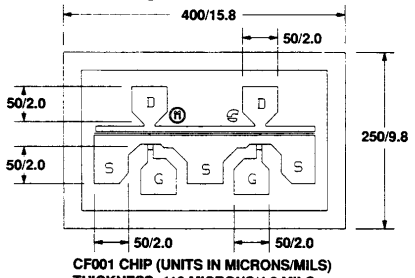
Absolute Maximum Ratings

Parameter	Symbol	Ratings
Drain-Source Voltage	V_{DS}	8V
Gate-Source Voltage	V_{GS}	-5V
Drain Current	I_{DS}	I_{DSS}
Continuous Dissipation	P_T	800 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	-65°C to +175°C

Typical Noise Parameters - CF001-03 V_{DS} = 3.0 V, I_{DS} = 15 mA

Frequency (GHz)	NF opt (dB)	Ga (dB)	Gamma opt (Mag)	Gamma opt (Ang)	Rn/50
2.0	0.35	19.4	0.85	9	0.69
4.0	0.43	16.2	0.76	19	0.48
6.0	0.51	14.0	0.70	35	0.38
8.0	0.60	12.4	0.65	54	0.31
10.0	0.70	11.4	0.60	73	0.26
12.0	0.80	10.8	0.55	90	0.21
14.0	0.91	10.2	0.52	107	0.17
16.0	1.02	9.8	0.49	123	0.12
18.0	1.14	9.3	0.48	142	0.09
20.0	1.27	8.8	0.49	162	0.06
22.0	1.40	8.2	0.53	-179	0.05
24.0	1.54	7.6	0.58	-165	0.05
26.0	1.68	7.0	0.58	-161	0.08

Chip Outline Drawing



CF001 CHIP (UNITS IN MICRONS/MILS)
THICKNESS: 110 MICRONS/4.3 MILS

Die Attach and Bonding Procedures

Die Attach: Conductive epoxy or eutectic die attach is recommended. For eutectic die attach: Preform: AuSn (80% Au, 20% Sn); Stage Temperature: 290°C, ±5°C; Handling Tool: Tweezers; Time: 1 min or less.

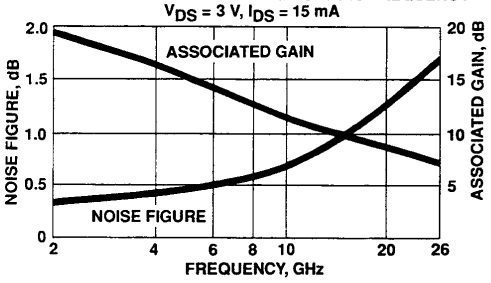
Wire Bonding: Wire Size: 0.7 to 1.0 mil in diameter (pre-stressed); Thermocompression bonding is preferred over thermosonic bonding. For thermocompression bonding: Stage Temperature: 250°C; Bond Tip Temperature: 150°C; Bonding Tip Pressure: 18 to 40 gms depending on size of wire.

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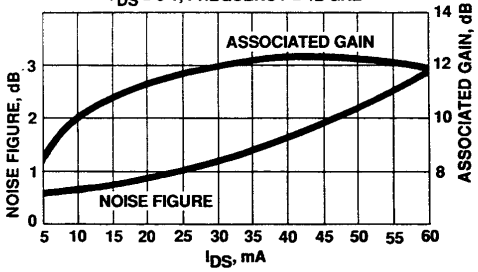
CF001 Series GaAs Chips

Typical Performance (T_A = 25°C)

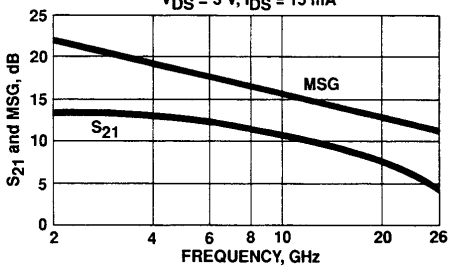
CF001-03
NOISE FIGURE AND ASSOCIATED GAIN vs FREQUENCY
V_{DS} = 3 V, I_{DS} = 15 mA



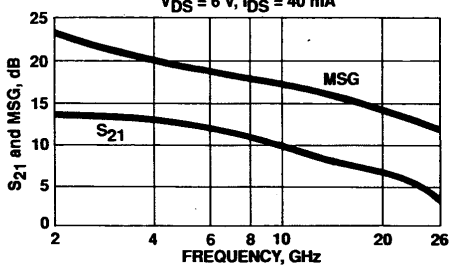
CF001-03
NOISE FIGURE AND ASSOCIATED GAIN vs I_{DS}
V_{DS} = 3 V, FREQUENCY = 12 GHZ



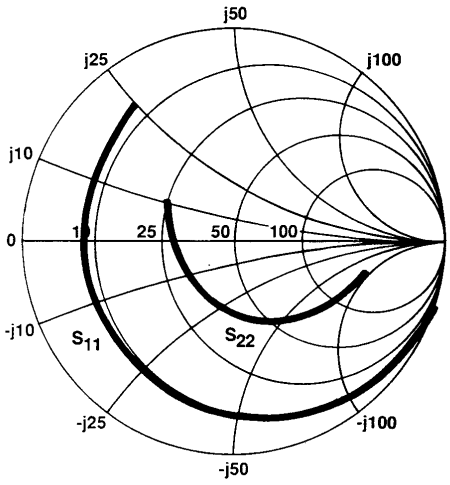
CF001-03
S_{21} AND MSG vs FREQUENCY at LOW NOISE BIAS
V_{DS} = 3 V, I_{DS} = 15 mA



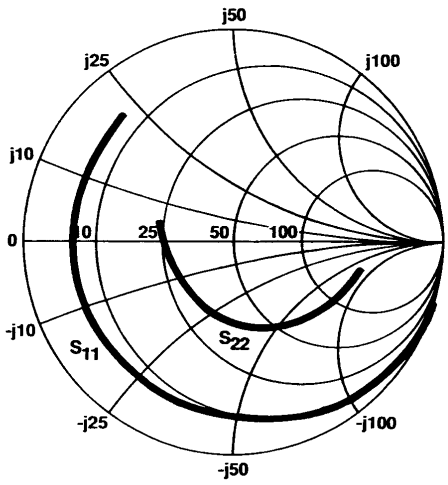
CF001-01
S_{21} AND MSG vs FREQUENCY at POWER BIAS
V_{DS} = 6 V, I_{DS} = 40 mA



CF001-03
S_{11} AND S_{22} vs FREQUENCY at LOW NOISE BIAS
V_{DS} = 3 V, I_{DS} = 15 mA



CF001-01
S_{11} AND S_{22} vs FREQUENCY at POWER BIAS
V_{DS} = 6 V, I_{DS} = 40 mA



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CF001 Series GaAs Chips

Typical Scattering Parameters, Common Source (S-Parameters Include Bonding Wire Parasitics)

CF001-01 at Power Bias V_{DS} = 6 V, I_{DS} = 40 mA

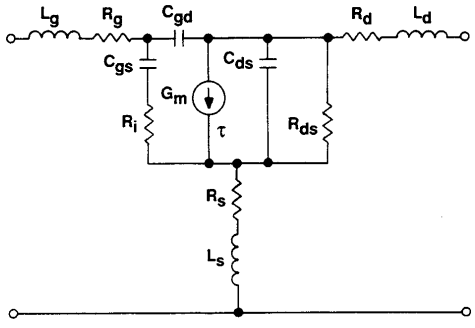
Frequency	S_{11}		S_{21}			S_{12}			S_{22}		K	MSG
(GHz)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(Mag)	(Ang)		(dB)
2.0	0.98	-24	13.2	4.56	156	-33.2	0.02	73	0.53	-10	0.27	23.2
4.0	0.93	-51	12.7	4.31	136	-27.7	0.04	62	0.50	-25	0.34	20.2
6.0	0.88	-72	11.7	3.83	118	-25.3	0.05	51	0.48	-35	0.46	18.5
8.0	0.84	-98	10.8	3.47	100	-23.8	0.06	38	0.43	-51	0.55	17.3
10.0	0.79	-122	9.5	2.99	82	-24.1	0.06	23	0.38	-68	0.83	16.8
12.0	0.79	-140	8.4	2.64	67	-23.3	0.07	18	0.38	-83	0.79	15.9
14.0	0.78	-154	7.6	2.41	55	-23.2	0.07	10	0.39	-93	0.86	15.4
16.0	0.78	-166	7.1	2.27	44	-22.5	0.07	5	0.36	-101	0.90	14.8
18.0	0.77	178	6.7	2.16	30	-21.8	0.08	-2	0.32	-113	0.93	14.2
20.0	0.76	159	6.2	2.04	15	-21.0	0.09	-13	0.27	-131	0.95	13.6
22.0	0.79	141	5.2	1.82	-2	-20.8	0.09	-20	0.27	-163	0.91	13.0
24.0	0.78	132	3.7	1.52	-13	-20.9	0.09	-21	0.30	176	1.12	12.3
26.0	0.81	129	2.3	1.31	-21	-20.5	0.09	-19	0.39	168	0.91	11.4

CF001-03 at Low Noise Bias V_{DS} = 3 V, I_{DS} = 15 mA

Frequency	S_{11}		S_{21}			S_{12}			S_{22}		K	MSG
(GHz)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(Mag)	(Ang)		(dB)
2.0	0.99	-24	13.2	4.57	160	-30.8	0.03	76	0.57	-16	0.08	22.0
4.0	0.95	-50	12.9	4.43	140	-25.0	0.06	61	0.54	-32	0.16	19.0
6.0	0.90	-69	12.1	4.02	124	-22.7	0.07	50	0.52	-43	0.25	17.4
8.0	0.85	-93	11.5	3.76	106	-21.0	0.09	35	0.46	-60	0.33	16.2
10.0	0.79	-118	10.6	3.38	88	-20.5	0.09	20	0.40	-79	0.47	15.5
12.0	0.78	-139	9.8	3.08	73	-19.6	0.10	10	0.38	-95	0.46	14.7
14.0	0.77	-156	9.1	2.85	60	-19.4	0.11	1	0.35	-107	0.52	14.2
16.0	0.76	-171	8.6	2.69	46	-18.6	0.12	-8	0.31	-120	0.55	13.6
18.0	0.77	171	8.0	2.52	32	-18.2	0.12	-18	0.25	-142	0.59	13.1
20.0	0.76	152	7.4	2.35	16	-17.9	0.13	-29	0.22	-171	0.64	12.6
22.0	0.79	136	6.3	2.05	0	-17.7	0.13	-38	0.26	158	0.60	12.0
24.0	0.77	129	4.7	1.72	-10	-18.3	0.12	-39	0.30	145	0.78	11.5
26.0	0.80	125	3.6	1.52	-17	-18.2	0.12	-39	0.36	145	0.70	10.9

Device Model

Parameters	CF001-01 VDS = 6V, IDS = 40mA	CF001-03 VDS = 3V, IDS = 15mA	Units
L_g	0.19	0.26	nH
R_g	1.0	1.0	Ω
C_{gs}	0.32	0.24	pF
R_i	1.9	1.6	Ω
C_{gd}	0.023	0.029	pF
G_m	66	66	mS
τ	2.7	2.1	ps
C_{ds}	0.12	0.10	pF
R_{ds}	161	171	Ω
R_d	1.3	1.3	Ω
L_d	0.21	0.23	nH
R_s	1.1	1.6	Ω
L_s	0.04	0.04	nH



Wafer Qualification Procedure

- 100% DC Test, 100% Visual Insp.
- Sample Chip Performance Test — NF, Power, S-Parameters, IP3, Power Blast
- Sample Circuit Performance Tests 6-18 GHz Module — NF, Power, Gain, VSWR
- Reliability Assesment — Power Blast & Burn-In

80% of tested samples must meet specifications for wafer acceptance.

3236 Scott Boulevard
Santa Clara, California 95054
(408) 986-5060
Fax: (408) 986-5095

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Specifications subject to change.

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