General Description

The AAT1157 SwitchReg™ is a member of AnalogicTech's Total Power Management IC™ (TPMIC™) product family. The step-down switching converter is ideal for applications where fixed frequency and low ripple are required over the full range of load conditions. The 2.7V to 5.5V input voltage range makes the AAT1157 ideal for single-cell lithium-ion/polymer battery applications. Capable of up to 1.2A with internal MOSFETs, the current-mode controlled IC provides high efficiency over a wide operating range. Fully integrated compensation simplifies system design and lowers external parts count. The device operates at a fixed 1MHz switching frequency across all load conditions.

The AAT1157 is available in the Pb-free, 16-pin 3x3mm QFN package and is rated over the -40°C to +85°C temperature range.

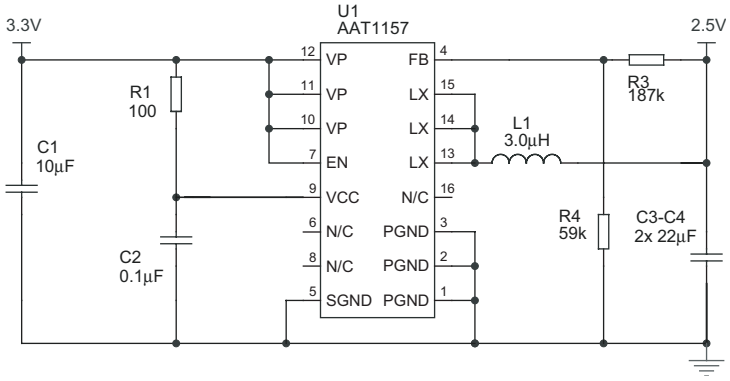
Features

- V_{IN} Range: 2.7V to 5.5V
- Up to 95% Efficiency
- 110 mΩ $R_{DS(ON)}$ Internal Switches
- <1µA Shutdown Current
- 1MHz Buck Switching Frequency
- Fixed or Adjustable $V_{OUT} \geq 0.8V$
- Integrated Power Switches
- Current Mode Operation
- Internal Compensation
- Stable with Ceramic Capacitors
- Constant PWM Operation for Low Output Ripple
- Internal Soft Start
- Over-Temperature Protection
- Current Limit Protection
- 16-Pin QFN 3x3mm Package
- -40°C to +85°C Temperature Range

Applications

- HDD MP3 Players
- Notebook Computers
- PDAs
- Point-of-Load Regulation
- Set Top Boxes
- Smart Phones
- Wireless Notebook Adapters

Typical Application

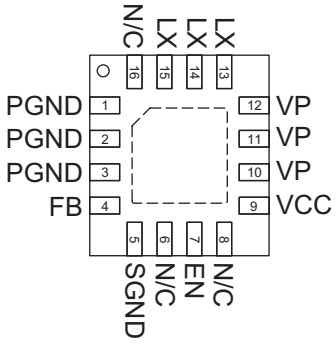


Pin Descriptions

Pin #	Symbol	Function
1, 2, 3	PGND	Main power ground return pin. Connect to the output and input capacitor return. (See board layout rules.)
4	FB	Feedback input pin. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an internal resistive divider. For an adjustable output, an external resistive divider is connected to this pin.
5	SGND	Signal ground. Connect the return of all small signal components to this pin. (See board layout rules.)
7	EN	Enable input pin. A logic high enables the converter; a logic low forces the AAT1157 into shutdown mode reducing the supply current to less than 1µA. The pin should not be left floating.
6, 8, 16	N/C	Not internally connected.
9	VCC	Bias supply. Supplies power for the internal circuitry. Connect to input power via low pass filter with decoupling to SGND.
10, 11, 12	VP	Input supply voltage for the converter power stage. Must be closely decoupled to PGND.
13, 14, 15	LX	Connect inductor to these pins. Switching node internally connected to the drain of both high- and low-side MOSFETs.
EP		Exposed paddle (bottom); connect to PGND directly beneath package.

Pin Configuration

QFN33-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{CC}, V_P	V_{CC}, V_P to GND	6	V
V_{LX}	LX to GND	-0.3 to V_P + 0.3	V
V_{FB}	FB to GND	-0.3 to V_{CC} + 0.3	V
V_{EN}	EN to GND	-0.3 to -6	V
T_J	Operating Junction Temperature Range	-40 to150	°C
V_{ESD}	ESD Rating[2] - HBM	3000	V

Thermal Characteristics

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance (QFN33-16)[3]	50	°C/W
θ_{JC}	Maximum Thermal Resistance (QFN33-16)	4.2	°C/W
P_D	Maximum Power Dissipation (QFN33-16) (T_A = 25°C)[3, 4]	2.0	W

Recommended Operating Conditions

Symbol	Description	Value	Units
T	Ambient Temperature Range	-40 to 85	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Human body model is 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
3. Mounted on a demo board (FR4, in still air). Exposed pad must be mounted to PCB.
4. Derate 20mW/°C above 25°C.

Electrical Characteristics[1]

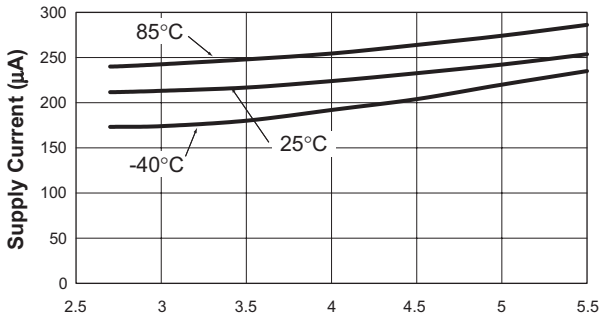
V_{IN} = V_{CC} = V_P = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{OUT}	Output Voltage Tolerance	V_{IN} = V_{OUT} + 0.2 to 5.5V, I_{OUT} = 0 to 1.2A	-4		+4	%
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	V_{IN} = 4.2V, I_{LOAD} = 0 to 1.2A		±2.5		%
$\Delta V_{OUT}(V_{OUT}*\Delta V_{IN})$	Line Regulation	V_{IN} =2.7 to 5.5V		±0.1		%/V
I_Q	Quiescent Supply Current	No Load		160	300	µA
I_{SHDN}	Shutdown Current	V_{EN} = 0V, V_{IN} = 5.5V			1.0	µA
I_{LIM}	Current Limit	T_A = 25°C	1.7			A
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising, V_{EN} = V_{CC}			2.5	V
		V_{IN} Falling, V_{EN} = V_{CC}	1.2			
$V_{UVLO(HYS)}$	Under-Voltage Lockout Hysteresis			250		mV
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		1.4			V
I_{IL}	Input Low Current	V_{IN} = V_{FB} = 5.5V			1.0	µA
I_{IH}	Input High Current	V_{IN} = V_{FB} = 0V			1.0	µA
$R_{DS(ON)H}$	High Side Switch On Resistance	T_A = 25°C		110	150	mΩ
$R_{DS(ON)L}$	Low Side Switch On Resistance	T_A = 25°C		100	150	mΩ
F_{OSC}	Oscillator Frequency	T_A = 25°C	750	1000	1250	kHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C

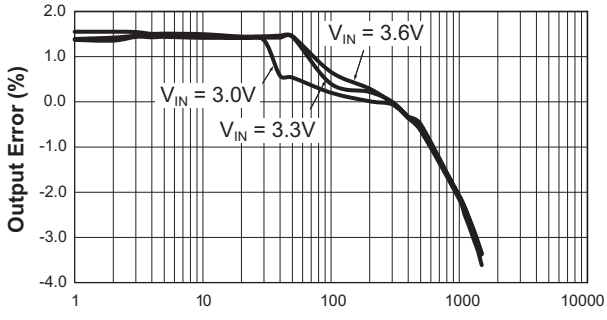
1. The AAT1157 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

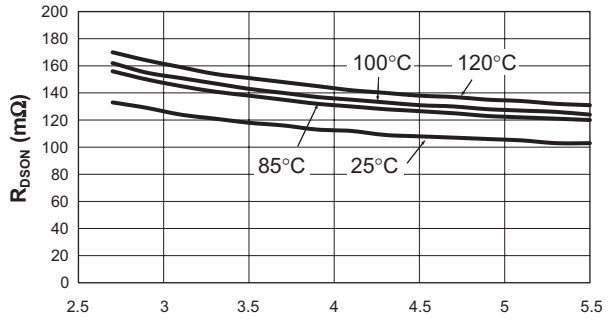
No Load Supply Current vs. Input Voltage



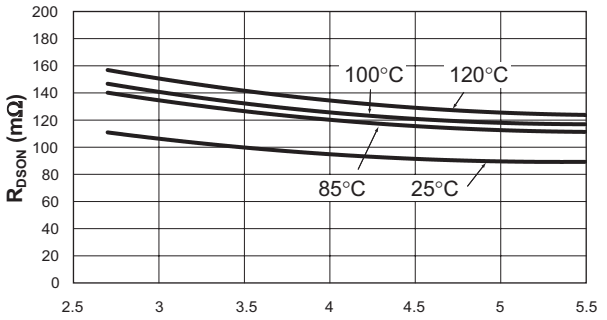
DC Regulation
(V_{OUT} = 2.5V)



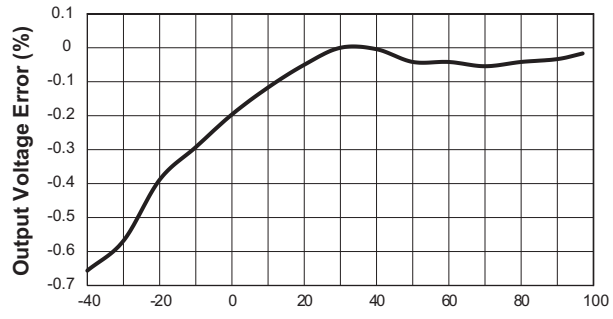
P-Channel R_{DSON} vs. Input Voltage



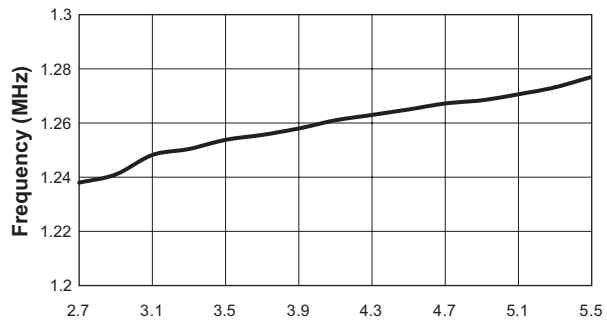
N-Channel R_{DSON} vs. Input Voltage



Output Voltage vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 2.5V; I_{OUT} = 1.0A)

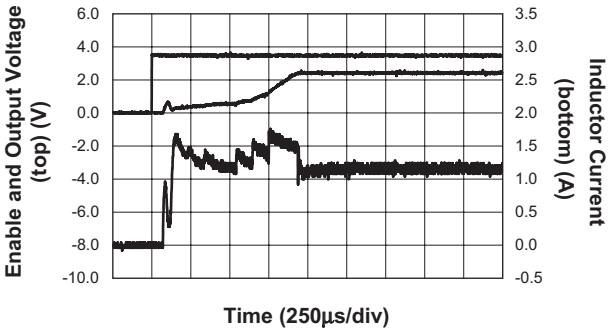


Frequency vs. Input Voltage
(V_{OUT} = 1.8V)

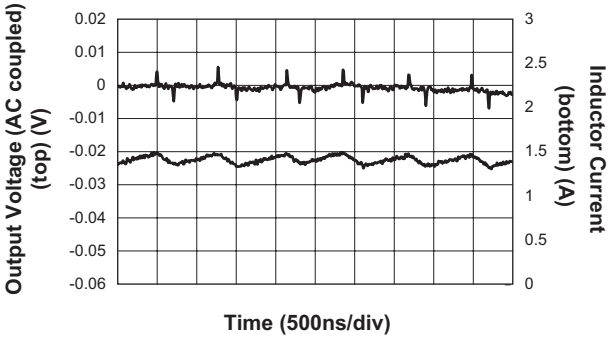


Typical Characteristics

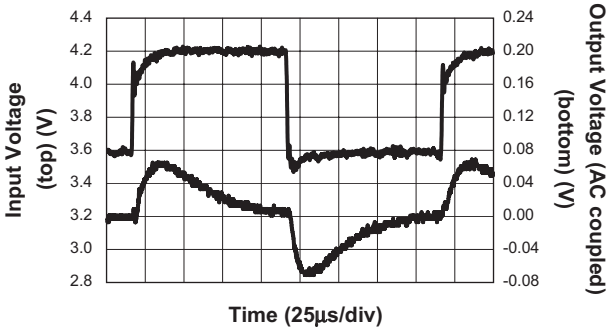
Soft Start
(V_{OUT} = 2.5V; I_{OUT} = 1.2A; V_{IN} = 3.6V)



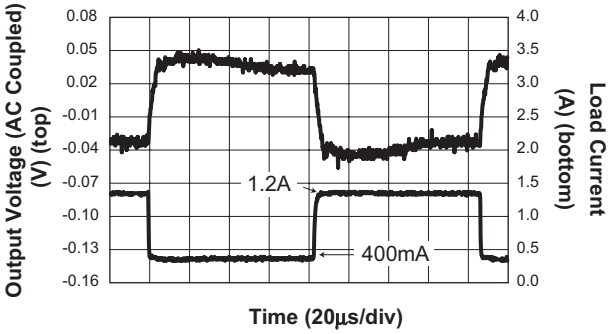
Output Ripple
(V_{OUT} = 2.5V; I_{OUT} = 1.2A; V_{IN} = 3.6V)



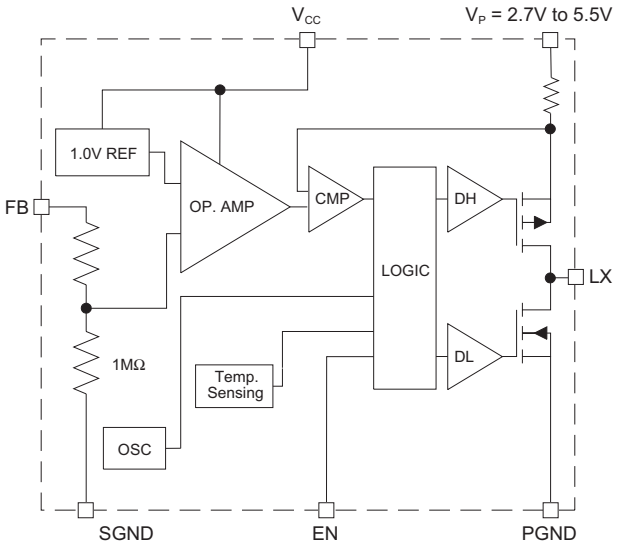
Line Transient
(I_{OUT} = 1.2A; V_O = 2.5V)



Load Transient Response
(400mA-1.2A; V_{IN} = 3.3V; V_{OUT} = 2.5V)



Functional Block Diagram



Applications Information

Control Loop

The AAT1157 is a peak current mode buck converter. The inner wide bandwidth loop controls the inductor peak current. The inductor current is sensed through the P-channel MOSFET (high side) and is also used for short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The loop appears as a voltage-programmed current source in parallel with the output capacitor.

The voltage error amplifier output programs the current loop for the necessary inductor current to force a constant output voltage for all load and line conditions. The external voltage feedback resistive divider divides the output voltage to the error amplifier reference voltage of 0.6V. The low-DC gain voltage error amplifier eliminates the need for external compensation components while providing sufficient DC loop gain for good load regulation. The voltage loop crossover frequency and phase margin are set by the output capacitor.

Soft Start/Enable

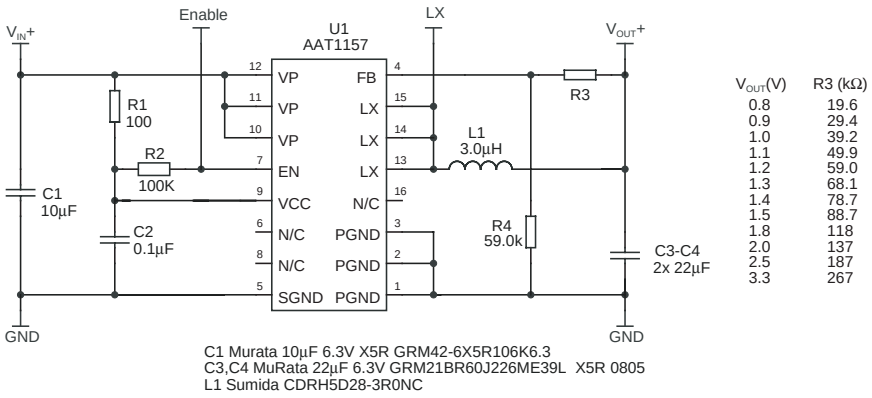
Soft start increases the inductor current limit point in discrete steps once the input voltage or enable input is applied. It limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT1157 into a non-switching shutdown state. The total input current during shutdown is less than 1µA.

Power and Signal Source

Separate small signal ground and power supply pins isolate the internal control circuitry from the noise associated with the output power MOSFET switching. The low-pass filter R1 and C2 shown in the Figure 1 schematic filters the input noise associated with the power switching.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current sensed through the high-side P-channel MOSFET is limited. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once the over-temperature or over-current fault is removed, the AAT1157 automatically recovers.



V_{OUT}(V)	R3 (kΩ)
0.8	19.6
0.9	29.4
1.0	39.2
1.1	49.9
1.2	59.0
1.3	68.1
1.4	78.7
1.5	88.7
1.8	118
2.0	137
2.5	187
3.3	267

Figure 1: AAT1157 Evaluation Board Schematic
Lithium-Ion to 2.5V Converter.

Inductor

The output inductor should limit the ripple current to 330mA at the maximum input voltage. This matches the inductor current downslope with the fixed internal slope compensation. For a 2.5V output and the ripple set to a maximum input voltage of 4.2V, the inductance value required to limit the ripple current to 330mA is 3.0µH. From this calculated value, a standard value can be selected.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

$$L = \frac{V_{OUT}}{\Delta I_{PP} \cdot F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

$$= \frac{2.5V}{0.33A \cdot 1MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right)$$

$$= 3.07\mu H$$

For a maximum ripple current of 330mA, the peak switch and inductor current at 1.2A is 1.365A. A standard value of 3.0µH can be used in this example. The 3.0µH Sumida series CDRH5D28 inductor has a 24mΩ maximum DCR and a 2.4A DC current rating.

Input Capacitor

The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the AAT1157. A low ESR/ESL ceramic capacitor is ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing radiated and conducted EMI while facilitating optimum performance of the AAT1157. Ceramic X5R or X7R capacitors are ideal for this function. The size required will vary depending on the load, output voltage, and input voltage source impedance characteristics. Values range from 1µF to 10µF. The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the RMS current in the input capacitor is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current reaches a maximum when V_{IN} is two times the output voltage where it is approximately one half of the load current. Losses associated with the input ceramic capacitor are typically minimal and are not an issue. The proper placement of the input capacitor can be seen in the evaluation board layout (C1 in Figure 2).

Output Capacitor

Since there are no external compensation components, the output capacitor has a strong effect on loop stability. Larger output capacitance reduces the crossover frequency while increasing the phase margin. For the 2.5V 1.2A design using the 3.0µH inductor, a 40µF capacitor provides a stable output. Table 1 provides a list of suggested output capacitor values for various output voltages. In addition to assisting in stability, the output capacitor limits the output ripple and provides holdup during large load transitions. The output capacitor RMS ripple current is given by:

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}}$$

For an X7R or X5R ceramic capacitor, the ESR is very low and the dissipation due to the RMS current of the capacitor is not a concern. Tantalum capacitors with sufficiently low ESR to meet output voltage ripple requirements also have an RMS current rating well beyond that actually seen in this application.

Layout

Figures 2 and 3 display the suggested PCB layout for the AAT1157. The following guidelines should be used to help insure a proper layout.

1. The input capacitor (C1) should connect as closely as possible to V_P (Pins 10, 11, and 12) and PGND (Pins 1, 2, and 3).
2. C3-C4 and L1 should be connected as closely as possible. The connection from L1 to the LX node should be as short as possible.
3. The trace connecting the FB pin to resistors R3 and R4 should be as short as possible by placing R3 and R4 immediately next to the AAT1157. The sense trace connection R3 to the output voltage should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to the PGND (Pins 1, 2, and 3) and SGND (Pin 5) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground. SGND (Pin 5) can also be used to remotely sense the output ground at the point of load to improve regulation.
5. A low pass filter (R1 and C2) provides a cleaner bias source for the AAT1157 active circuitry. C2 should be placed as closely as possible to SGND (Pin 5) and V_{CC} (Pin 9).
6. For good heat transfer, four 15 mil vias spaced on a 26 mil grid connect the QFN central paddle to the bottom side ground plane, as shown in Figures 2 and 3.

Thermal Calculations

There are three types of losses associated with the AAT1157: MOSFET switching losses, conduction losses, and quiescent current losses. The conduction losses are due to the R_{DSON} characteristics of the internal P- and N-channel MOSFET power devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the total losses is given by:

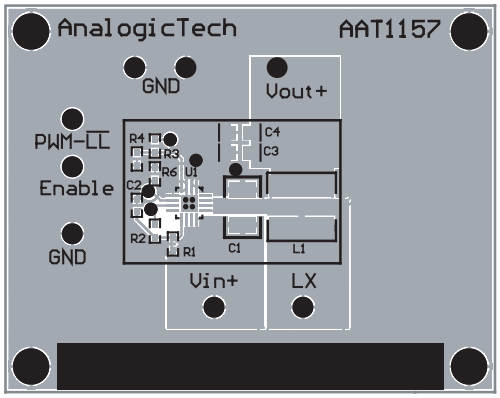


Figure 2: Evaluation Board Top Side.

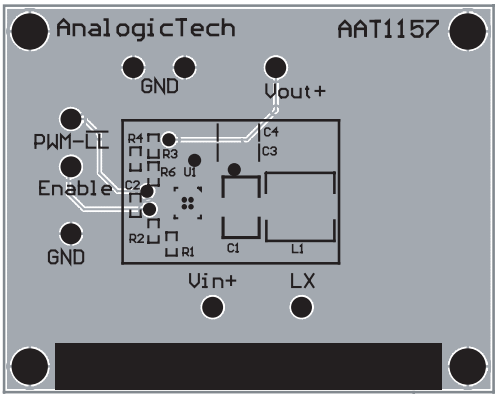


Figure 3: Evaluation Board Bottom Side.

$$P = \frac{I_O^2 \cdot (R_{DSON(HS)} \cdot V_O + R_{DSON(LS)} \cdot (V_{IN} - V_O))}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_O \cdot V_{IN} + I_Q) \cdot V_{IN}$$

Where I_Q is the AAT1157 quiescent current.

Once the total losses have been determined, the junction temperature can be derived from the θ_{JA} for the QFN package. Close attention should be paid to the proper layout for the QFN package. Proper size and placement of thermal routing vias below the central paddle is necessary for good heat transfer to other PCB layers and their ground planes. The θ_{JA} for the QFN package with no connection to the central paddle is 50°C/W. The actual θ_{JA} will vary with the number and type of vias. The PCB board size, number of board layers, and ground plane characteristics also influence the θ_{JA}. A good thermal connection from the paddle to the PCB ground plane layers can significantly reduce θ_{JA}.

$$T_J = P \cdot \Theta_{JA} + T_{AMB}$$

Adjustable Output

Resistors R3 and R4, as shown in Figure 1, force the output to regulate higher than the 0.6V reference voltage level. The optimum value for R4 is 59kΩ. Values higher than this can cause stability problems, while lower values can degrade light load efficiency. For a 2.5V output with R4 set to 59kΩ, R3 is 187kΩ.

$$R3 = \left(\frac{V_O}{V_{REF}} - 1\right) \cdot R4 = \left(\frac{2.5V}{0.6V} - 1\right) \cdot 59k\Omega = 187k\Omega$$

Table 1: Suggested Component Values.

Output Voltage (V)	L1 (µH)	Output Capacitor (C3-C4) (µF)	R3 for R4 = 59kΩ (kΩ)
0.8	1.5 - 2.6	3x 22	19.6
1.0	1.5 - 3.3	2x 22	39.2
1.2	2.2 - 3.3	2x 22	59
1.5	2.2 - 4.7	2x 22	88.7
1.8	3.0 - 4.7	2x 22	118
2.5	3.0 - 4.7	2x 22	187
3.3	2.2 - 4.7	22	267

Buck-Boost Output

Figure 4 shows how to configure the AAT1157 in a buck boost configuration with an external MOSFET and Schottky diode. The converter has a 3.3V 600mA output with an input voltage ranging from 2.7V to 5.5V.

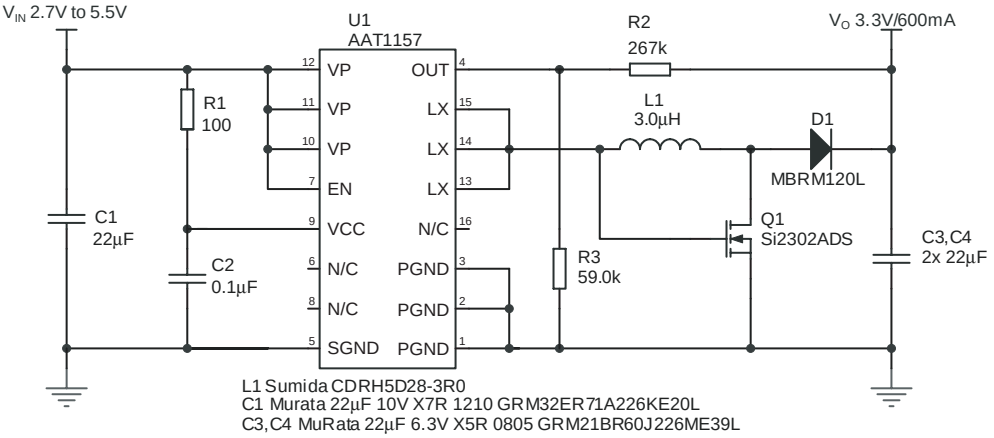


Figure 4: AAT1157 Buck Boost Converter.

Design Example

Specifications

I_{OUT} 1.2A

I_{RIPPLE} 330mA

V_{OUT} 2.5V

V_{IN} 3.0V to 4.2V

F_S 1MHz

T_{AMB} = 85°C

Maximum Input Capacitor Ripple:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = 0.59\text{Arms}$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot 0.59^2\ A = 1.7mW$$

Inductor Selection:

$$L = \frac{V_{OUT}}{\Delta I_{PP} \cdot F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{2.5V}{0.33A \cdot 1MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 3.07\mu H$$

Select Sumida inductor CDRH5D28 3.0µH.

$$\Delta I = \frac{V_O}{L \cdot F} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{2.5V}{3.0\mu H \cdot 1MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 340mA$$

$$I_{PK} = I_{OUT} + \frac{\Delta I}{2} = 1.2A + 0.17A = 1.37A$$

$$P = I_O^2 \cdot DCR = (1.2A)^2 \cdot 31m\Omega = 45mW$$

Output Capacitor Ripple Current:

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN} - V_{OUT})}{L \cdot F \cdot V_{IN}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{2.5V \cdot (4.2V - 2.5V)}{3.0\mu H \cdot 1MHz \cdot 4.2V} = 97.4\text{mArms}$$

$$Pesr = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (97.4mA)^2 = 47.4\mu W$$

AAT1157 Dissipation and Junction Temperature Estimate:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DSON(HS)} \cdot V_O + R_{DSON(LS)} \cdot (V_{IN} - V_O))}{V_{IN}} + (t_{sw} \cdot F \cdot I_O + I_Q) \cdot V_{IN}$$

$$= \frac{1.2A^2 \cdot (0.17\Omega \cdot 2.5V + 0.16\Omega \cdot (4.2V - 2.5V))}{4.2V} + (20nsec \cdot 1MHz \cdot 1.2A + 275\mu A) \cdot 4.2V$$

$$= 341mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{TOTAL} = 85°C + 50°C/W \cdot 0.341W = 102°C$$

Surface Mount Inductors

Manufacturer	Part Number	Value (µH)	Max DC Current (A)	DCR (mΩ)	Size (mm) L x W x H	Type
Sumida	CDRH5D28-2R6	2.6	2.6	18	5.7x5.7x3.0	Shielded
Sumida	CDRH5D28-3R0	3.0	2.4	24	5.7x5.7x3.0	Shielded
Sumida	CDRH5D28-4R2	4.2	2.2	31	5.7x5.7x3.0	Shielded
TaiyoYuden	NPO5DB4R7M	4.7	1.4	38	5.9x6.1x2.8	Shielded
Sumida	CDRH4D28-2R2	2.2	2.04	31	5.0x5.0x3.0	Shielded
Sumida	CDRH4D28-2R7	2.7	1.6	43	5.0x5.0x3.0	Shielded
Sumida	CDRH4D28-3R3	3.3	1.57	49	5.0x5.0x3.0	Shielded
Sumida	CDRH5D18-4R1	4.1	1.95	57	5.7x5.7x2.0	Shielded
Sumida	CDRH3D16/HP-2R2	2.2	2.3	59	4.0x4.0x1.8	Shielded
Sumida	CDRH3D16/HP-3R3	3.3	1.8	85	4.0x4.0x1.8	Shielded
MuRata	LQH55DN4R7M03	4.7	2.7	41	5.0x5.0x4.7	Non-Shielded
MuRata	LQH66SN4R7M03	4.7	2.2	25	6.3x6.3x4.7	Shielded

Surface Mount Capacitors

Manufacturer	Part Number	Value (µF)	Voltage (V)	Temp. Co.	Case
MuRata	GRM21BR60J106ME01L	10	6.3	X5R	0805
MuRata	GRM21BR60J226ME01L	22	6.3	X5R	0805
MuRata	GRM31CR60J106KA01L	10	6.3	X5R	1206

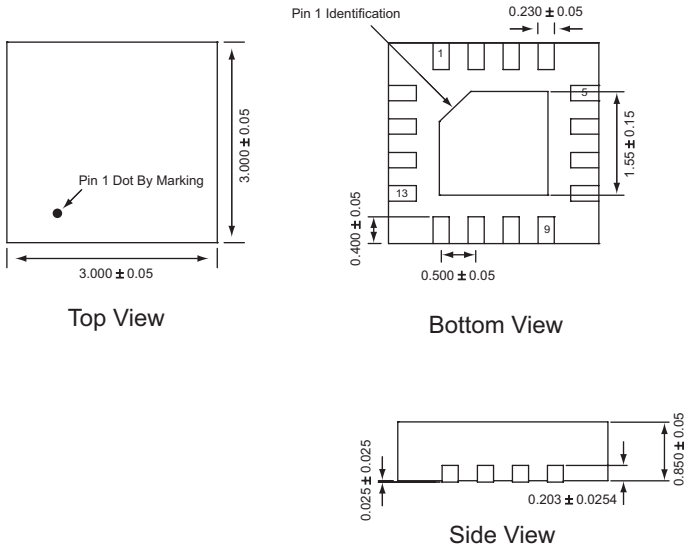
Ordering Information

Output Voltage	Package	Marking[1]	Part Number (Tape and Reel)[2]
FB = 0.8V, Adjustable ≥ 0.8V	QFN33-16	OEXYY	**AAT1157IVN-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/pbfree.

Package Information

QFN33-16



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611