CDP1871A, CDP1871AC

REFERENCE APP NOTE 7374

August 1996

CMOS Keyboard Encoder

Features

- **Directly Interfaces with CDP1800-Series Microprocessor**
- **Low Power Dissipation**
- **Three-State Outputs**
- **Scans and Generates Code for 53 Key ASCII Keyboard Plus 32 HEX Keys (SPST Mechanical Contact Switches)**
- **Shift, Control, and Alpha Lock Input**
- **RC-Controlled Debounce Circuitry**
- **Single Supply 4V to 10.5V . . . . . (CDP1871A)**
  4V to 6.5V . . . . . (CDP1871AC)
- **N-Key Lockout**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1871ACE	CDP1871AE	E40.6
PLCC	-40°C to +85°C	CDP1871ACQ	-	N44.65
SBDIP	-40°C to +85°C	CDP1871ACD	CDP1871AD	D40.6
Burn-In		CDP1871ACDX	-	D40.6

Description

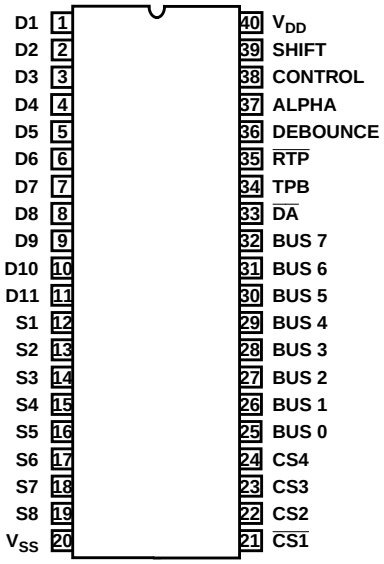
The CDP1871A is a keyboard encoder designed to directly interface between a CDP1800-series microprocessor and a mechanical keyboard array, providing up to 53 ASCII coded keys and 32 HEX coded keys, as shown in the system diagram (Figure 1).

The keyboard may consist of simple single-pole single-throw (SPST) mechanical switches. Inputs are provided for alpha-lock, control, and shift functions, allowing 160 unique codes. An external R-C input is available for user-selectable debounce times. The N-key lock-out feature prevents unwanted key codes if two or more keys are pressed simultaneously.

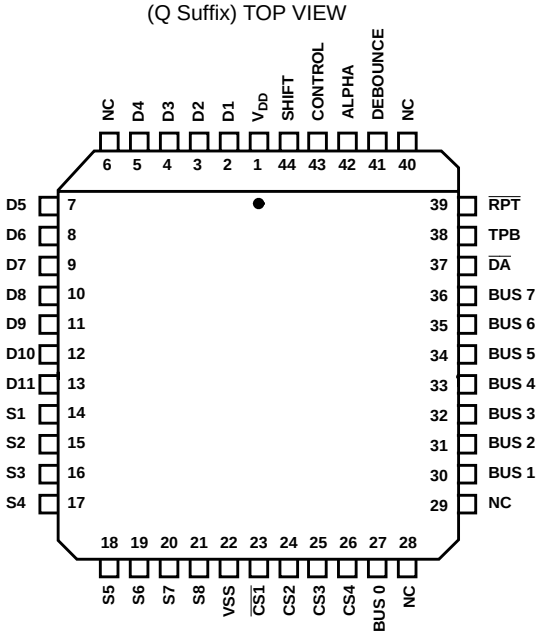
The CDP1871A and CDP1871AC are functionally identical. They differ in that the CDP1871A has a recommended operating voltage range of 4V to 10.5V, and the CDP1871AC has a recommended operating voltage range 4V to 6.5V. These types are supplied in 40 lead dual-in-line ceramic packages (D suffix), and 40 lead dual-in-line plastic packages (E suffix), and 44 lead plastic chip-carrier packages (Q suffix).

Pinouts

40 LEAD PDIP, CERDIP
TOP VIEW



44 LEAD PLCC
(Q Suffix) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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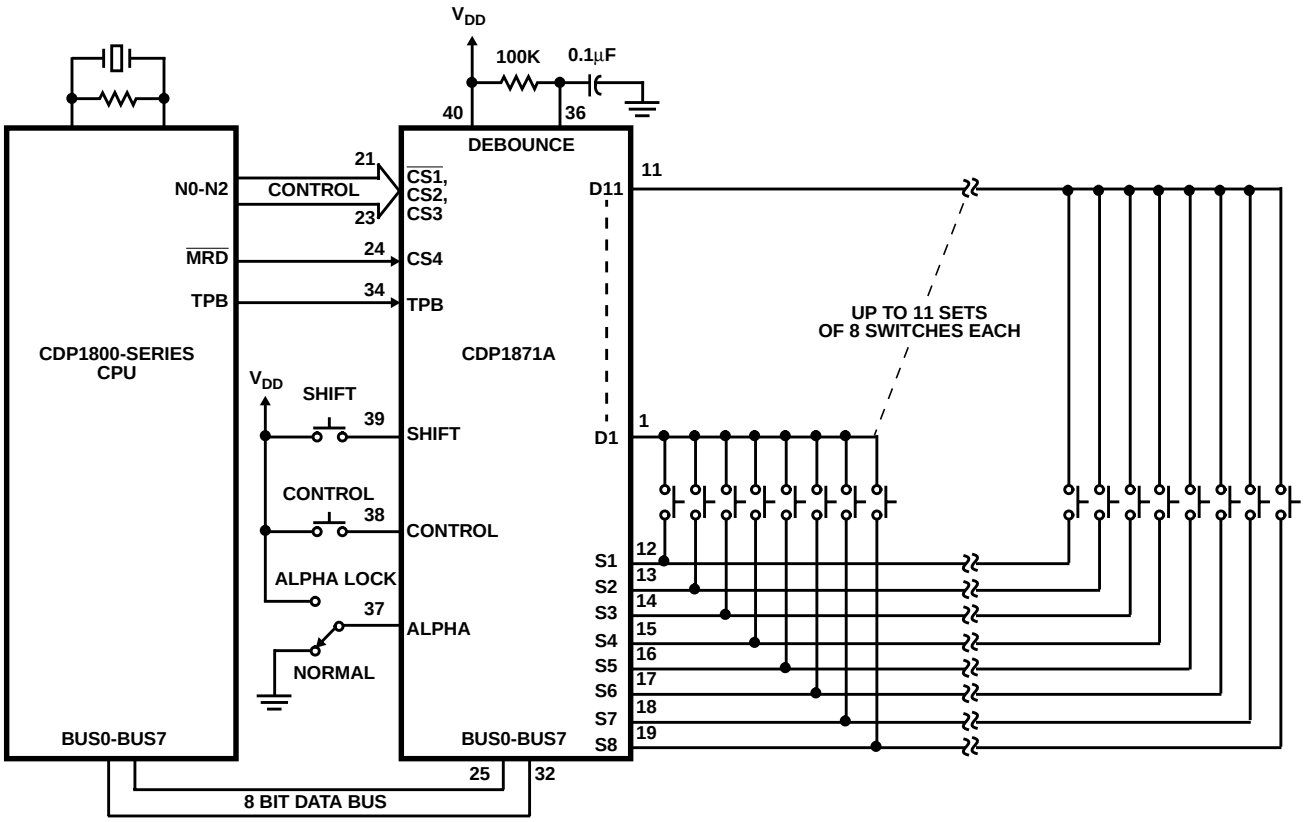


FIGURE 1. TYPICAL CDP1800 SERIES MICROPROCESSOR SYSTEM USING THE CDP1871A

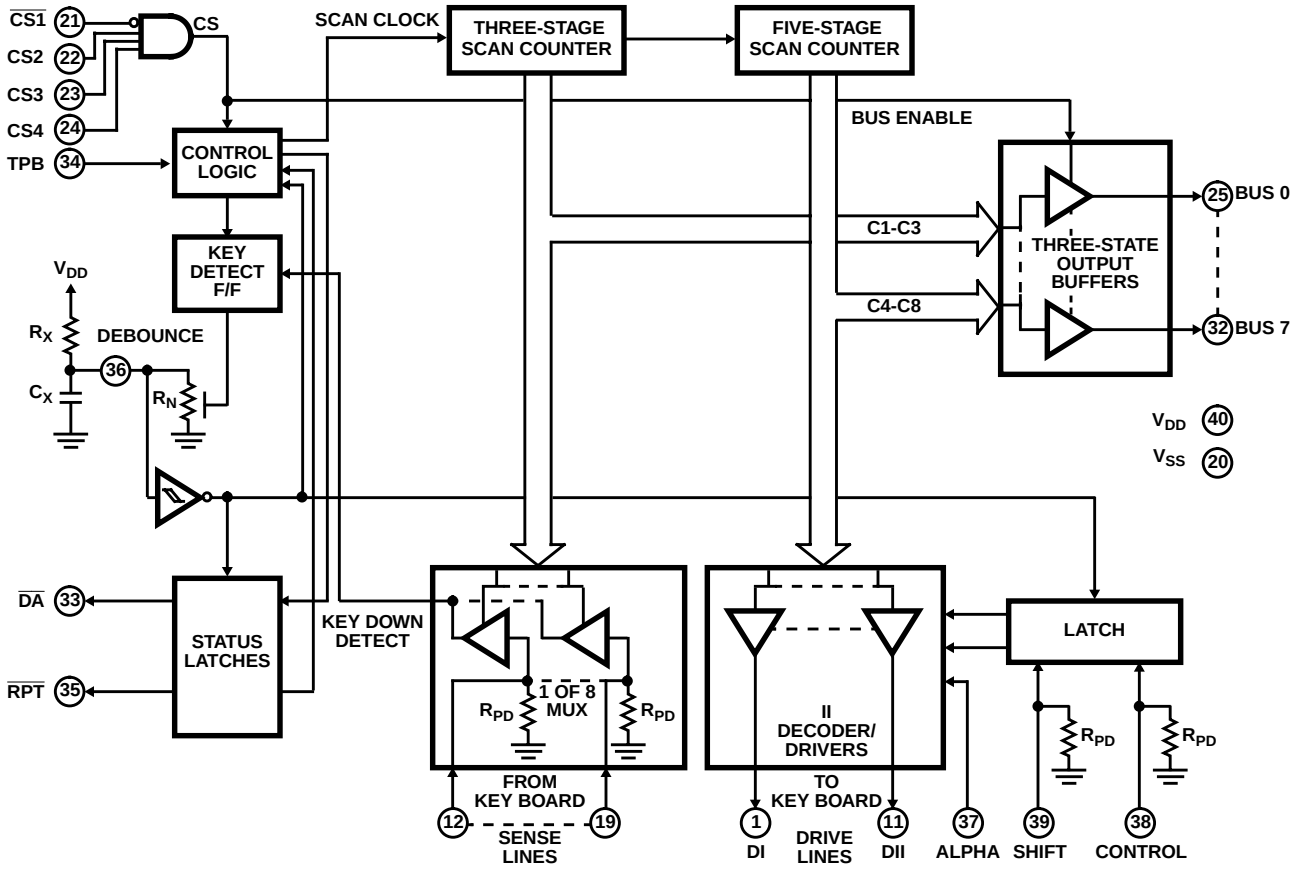


FIGURE 2. CDP1871A BLOCK DIAGRAM

Absolute Maximum Ratings

(All Voltages Referenced to V_{SS} Terminal)
CDP1871A. . . . . -0.5V to +11V
CDP1871AC . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	60	N/A
PLCC Package	50	N/A
SBDIP Package	60	18

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D. . . . . -55^oC to $+125^oC$
Package Type E and Q . . . . . -40^oC to $+85^oC$
Storage Temperature Range (T_{STG}) . . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . $+265^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

At T_A = -40 to $+85^oC$. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1871AD, CDP1871AE		CDP1871ACD, CDP1871ACE		
			MIN	MAX	MIN	MAX	
Supply Voltage Range			4	10.5	4	6.5	V
Recommended Input Voltage Range			V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Frequency, TPB (Keyboard Capacitance = 200 pF)	f_{CL}	5	DC	0.4	DC	0.4	MHz
		10	DC	0.8	-	-	MHz

NOTE:

1. Printed-circuit board mount: 57mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.

Static Electrical Specifications

At T_A = -40 to $+85^oC$, Unless Otherwise Specified

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0.5	5	-	0.1	50	-	1	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current (Except Debounce and D1-D11)	I_{OL}	0.4	0, 5	5	0.5	1	-	0.5	1	-	mA
		0.5	0, 10	10	1	2	-	-	-	-	mA
Debounce	I_{OL}	0.4	0, 5	5	0.75	1.5	-	0.75	1.5	-	mA
		0.5	0, 10	10	1	2	-	-	-	-	mA
D1-D11	I_{OL}	0.4	0, 5	5	0.05	0.1	-	0.05	0.1	-	mA
		0.5	0, 10	10	0.1	0.2	-	-	-	-	mA

Static Electrical Specifications At T_A = -40 to +85°C, Unless Otherwise Specified **(Continued)**

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1871AD CDP1871AE MIN	LIMITS CDP1871AD CDP1871AE (NOTE 1) TYP	LIMITS CDP1871AD CDP1871AE MAX	LIMITS CDP1871ACD CDP1871ACE MIN	LIMITS CDP1871ACD CDP1871ACE (NOTE1) TYP	LIMITS CDP1871ACD CDP1871ACE MAX	UNITS
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.3	-0.6	-	-0.3	-0.6	-	mA
		9.5	0, 10	10	-0.75	-1.5	-	-	-	-	mA
Input Low Voltage (Except Debounce)	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage (Except Debounce)	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V
Debounce Schmitt Trigger Input Voltage	V_D	0.4	-	5	2.0	3.3	4.0	2.0	3.3	4.0	V
Positive Trigger Voltage		0.5	-	10	4.0	6.3	8.0	-	-	-	V
Negative Trigger Voltage	V_N	0.4	-	5	0.8	1.8	3.0	0.8	1.8	3.0	V
		0.5	-	10	1.9	4.0	6.0	-	-	-	V
Hysteresis	V_H	0.4	0, 5	5	0.3	1.6	2.6	0.3	1.6	2.6	V
		0.5	0, 10	10	0.7	2.3	4.7	-	-	-	V
Output Voltage Low Level	V_{OL}	-	0, 5	5	-	0	0.05	-	0	0.05	V
		-	0, 10	10	-	0	0.05	-	-	-	V
Output Voltage High Level	V_{OH}	-	0, 5	5	4.95	5	-	4.95	5	-	V
		-	0, 10	10	9.95	10	-	-	-	-	V
Input Leakage Current (Except S1-S8, Shift, Control)	I_{IN}	-	0, 5	5	-	0.01	1	-	0.01	1	µA
		-	0, 10	10	-	0.01	1	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	0.01	1	-	0.02	2	µA
		0, 10	0, 10	10	-	0.02	2	-	-	-	µA
Pull-Down Resistor Value (S1-S8, Shift, Control)	R_{PD}	-	-	-	7	14	24	7	14	24	kΩ
Operating Current (All Outputs Unloaded) f_{CL} = 0.4MHz	I_{OPER}	0.5, 4.5	0, 5	5	-	0.6	-	-	0.6	-	mA
f_{CL} = 0.8MHz		1, 9	0, 10	10	-	2.7	-	-	-	-	mA

NOTE:

1. Typical values are for T_A = +25°C and nominal V_{DD}.

Functional Description of CDP1871A Terminals

D1 - D11 (Outputs):

Drive lines for the 11 x 8 keyboard switch matrix. These outputs are connected through the external switch matrix to the sense lines (S1 - S8).

S1 - S8 (Inputs):

Sense lines for the 11 x 8 keyboard maxtrix. These inputs have internal pull-down resistors and are driven high by appropriate drive line when a keyboard switch is closed.

$\overline{CS1}$, CS2, CS3, CS4 (Inputs):

Chip select inputs, which are used to enable the three-state data bus outputs (BUS 0 - BUS 7) and to enable the resetting of the status flag ($\overline{DA}$), which occurs on the low-to-high transition of TPB. These four inputs are normally connected to the N-lines (N0-N2) and $\overline{MRD}$ output of the CDP1800-series microprocessor. (Table 2)

BUS 0 - BUS 7 (Outputs):

Three-state data bus outputs which provide the ASCll and HEX codes of the detected keys. The outputs are normally connected to the BUS 0 - BUS 7 terminals of the CDP1800-series microprocessor.

$\overline{DA}$ (Output):

The data available output flag which is set low when a valid key closure is detected. It is reset high by the low-to-high transition of TPB when data is read from the CDP1871A. This output is normally connected to a flag input ($\overline{EF1}$ - $\overline{EF4}$) of the CDP1800-series microprocessor.

TPB (Input):

The input clock used to drive the scan generator and reset the status flag ($\overline{DA}$). This input is normally connected to the TPB output of the CDP1800-series microprocessor.

$\overline{RPT}$ (Output):

The repeat output flag which is used to indicate that a key is still closed after data has been read from the CDP1871A ($\overline{DA}$ = high). It remains low as long as the key is closed and is used for an autorepeat function, under CPU control. This output is normally connected to a flag input ($\overline{EF1}$ - $\overline{EF4}$) of the CDP1800-series microprocessor.

DEBOUNCE (Input):

This input is connected to the junction of an external resistor to V_{DD} and capacitor to V_{SS}. It provides a debounce time delay ($t \cong RC$) after the release of a key. If a debounce is not desired, the external pull-up resistor is still required.

ALPHA, SHIFT, CONTROL (Inputs):

A high on the SHIFT or CONTROL inputs will be internally latched (after the debounce time) and the drive and sense line decoding will be modified as shown in Table 3. They are normally connected to the keyboard, but produce no code by themselves. The SHIFT and CONTROL inputs have internal pull-down resistors to simplify use with momentary contact switches. The ALPHA input is not latched and is designed for a standard SPDT switch to provide an alpha-lock function. When ALPHA = 1 the drive and sense line decoding will be modified as shown in Table 3.

V_{DD}, V_{SS}:

V_{DD} is the positive supply voltage input. V_{SS} is the most negative supply voltage terminal and is normal connected to ground. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

TABLE 1. SWITCH INPUT FUNCTIONS

CONTROL	SHIFT	ALPHA	KEY FUNCTION
0	0	0	Normal
1	X	X	Control
0	1	X	Shift
0	0	1	Alpha

NOTE: X = Don't Care

TABLE 2. VALID N-LINE CONNECTIONS

CPU	CDP1871A SIGNAL				CPU INPUT INSTRUCTION
	CS4	CS3	CS2	$\overline{CS1}$	
CDP1800- Series Signal	$\overline{MRD}$	N2	N0	N1	INP5
	$\overline{MRD}$	N0	N1	N2	INP3
	$\overline{MRD}$	N2	N1	N0	INP6

TABLE 3. DRIVE AND SENSE LINE KEYBOARD CONNECTIONS (NOTE 2)

SENSE LINES	DRIVE LINES																
	D_1		D_2		D_3		D_4		D_5		D_6		D_7	D_8	D_9	D_{10}	D_{11}
S_1	SP	0	(	8	‘	@	H	H	P	P	X	X	Space	80_{16}	88_{16}	90_{16}	98_{16}
	0		8		@	NUL	h	BS	p	DLE	x	CAN					
S_2	!	1	)	9	A	A	I	I	Q	Q	Y	Y		81_{16}	89_{16}	91_{16}	99_{16}
	1		9		a	SOH	i	HT	q	DC1	y	EM					
S_3	“	2	*	:	B	B	J	J	R	R	Z	Z	Line Feed	82_{16}	$8A_{16}$	92_{16}	$9A_{16}$
	2		:		b	STX	j	LF	r	DC2	z	SUB					
S_4	#	3	+	;	C	C	K	K	S	S	{	[	Escape	83_{16}	$8B_{16}$	93_{16}	$9B_{16}$
	3		;		c	ETX	k	VT	s	DC3	[	ESC					
S_5	$	4	<	,	D	D	L	L	T	T	|	\		84_{16}	$8C_{16}$	94_{16}	$9C_{16}$
	4		,		d	EOT	I	FF	t	DC4	\	FS					
S_6	%	5	=	-	E	E	M	M	U	U	}	]	Carriage Return	85_{16}	$8D_{16}$	95_{16}	$9D_{16}$
	5		-		e	ENQ	m	CR	u	NAK	]	GS					
S_7	&	6	>	.	F	F	N	N	V	V	~	↑		86_{16}	$8E_{16}$	96_{16}	$9E_{16}$
	6		.		f	ACK	n	SO	v	SYN	↑	RS					
S_8	‘	7	?	/	G	G	O	O	W	W	Del	-	Delete	87_{16}	$8F_{16}$	97_{16}	$9F_{16}$
	7		/		g	BEL	o	SI	W	ETB	-	US					

KEY:

SHIFT (Note 1)	ALPHA (Note 1)
NORMAL	CONTROL (Note 1)

NOTES:

1. CONTROL overrides SHIFT and ALPHA = No Response
2. Showing ASCII outputs for all combinations with and without SHIFT, ALPHA LOCK and CONTROL.
3. Drive lines 8, 9, 10 and 11 generate non-ASCII hex values which can be used for special codes.

TABLE 4. HEXIDECIMAL VALUES OF ASCII CHARACTERS

						MSD							
					b7 →	0	0	0	0	1	1	1	1
					b6 →	0	0	1	1	0	0	1	1
BITS					b5 →	0	1	0	1	0	1	0	1
	b4	b3	b2	b1	HEX ↓	0	1	2	3	4	5	6	7
LSD	0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	“	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	/	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	B	VT	ESC	+	;	K	[	k	{
	1	1	0	0	C	FF	FS	,	<	L	\	l	|
	1	1	0	1	D	CR	GS	-	=	M	]	m	}
	1	1	1	0	E	SO	RS	.	>	N	↑	n	~
	1	1	1	1	F	SI	US	/	?	O	-	o	DEL

Operation

The CDP1871A is made up of two major sections: the counter/scan-selection logic and the control logic (Figure 2). The counter and scan-selection logic scans the keyboard array using the drive lines (D1-D11) and the sense lines (S1-S8). The outputs of the internal 5-stage scancounter are conditionally encoded by the ALPHA, SHIFT, and CONTROL inputs (Table 1, Table 3) and are used to drive the D1-D11 output lines high one at a time. Each D1-D11 output may drive up to eight keys, which are sampled by the sense line inputs (S1-S8). The S1-S8 inputs are enabled by the internal 3-stage scancounter.

The control logic interfaces with the CDP1800-series I/O and timing signals to establish timing and status conditions for the CDP1871A.

The TPB input clocks the scancounters and is also used to reset the Data Available output ($\overline{DA}$). When a valid keydown condition is detected on a sense line, the control logic inhibits the clock to the scancounters on the next low-to-high transition of TPB and the $\overline{DA}$ output is set low. The scancounter outputs (C1 - C8) represent the ASCII and HEX key codes and are used to drive the BUS 0 - BUS 7 outputs, which interface directly to the CDP1800-Series data bus. The BUS 0 - BUS 7 outputs, which are normally three-stated, are enabled by decoding the CS inputs during a CPU input instruction (Table 2). The low-to-high transition of TPB during the input instruction resets the $\overline{DA}$ output high. Once the $\overline{DA}$ output has been reset, it cannot go low again until the present key is released and a new keydown condition is detected. (This prevents unwanted repeated keycode outputs which may be caused by fast software routines).

After the depressed key is released and the debounce delay (determined by RX, CX) has occurred, the scan clock inhibit is removed, allowing the scancounters to advance on the following high-to-low transitions of TPB. This provides an N-key lockout feature, which prevents the entry of erroneous codes when two or more keys are pressed simultaneously. The first key pressed in the scanning order is recognized, while all other keys pressed are ignored until the first key is released

and read by the CPU, at which time the next key pressed in the scanning order is detected. If the first key remains closed after the CPU reads the data and resets the $\overline{DA}$ output, on the low-to-high transition of TPB, an auxiliary signal ($\overline{RPT}$) is generated and is available to the CPU to indicate an auto-repeat condition. The $\overline{RPT}$ output is reset high at the end of the debounce delay after the depressed key is released.

The DEBOUNCE input provides a terminal connection for an external user-selected RC circuit to eliminate false detection of a keydown condition caused by keyboard noise. The operation of the DEBOUNCE circuit is shown in Figure 2 (Pin 36). When a valid keydown is detected, the on-chip active-resistor device (R_N) is enabled and the external capacitor (C_X) is discharged, providing a key closure debounce time $\cong R_N C_X$. This discharge is sensed by the Schmitt-trigger inverter, which clocks the $\overline{DA}$ flip-flop (latching the $\overline{DA}$ output low and inhibiting the scan clock). (The $\overline{DA}$ F/F is reset by the low-to-high transition of TPB when the CS inputs are enabled). When a valid key-release is detected RN is disabled and C_X begins to charge through the external resistor (R_X), providing a key-release debounce time $\cong R_X C_X$. This charge time is again sensed by the Schmitt-trigger inverter, enabling the scan clock to continue on the next high-to-low transitions of TPB, after the current keycode data is read by the CPU.

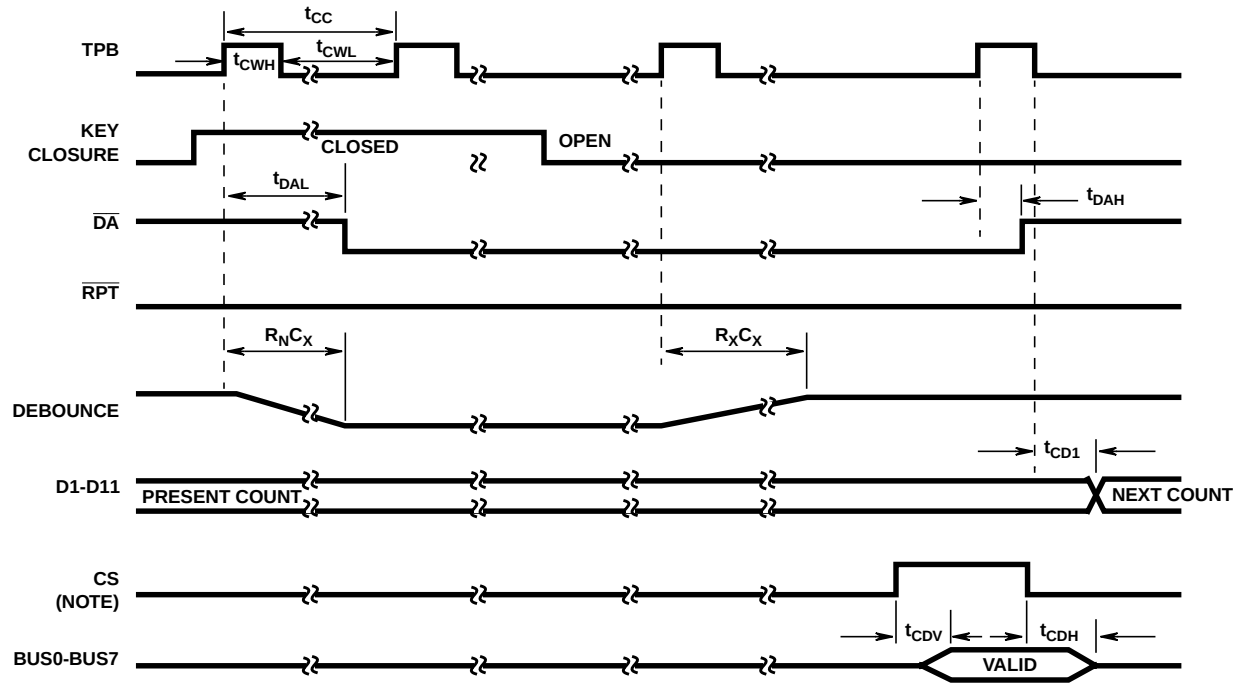
Dynamic Electrical Specifications

At T_A = -40 to +85°C, V_{DD} ±5%, Unless Otherwise Specified

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1871AD, CDP1871AE			CDP1871ACD, CDP1871ACE			
			MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Clock Cycle Time	t_{CC}	5	-	-	-	-	-	-	Note 2
		10	-	-	-	-	-	-	Note 2
Clock Pulse Width High	t_{CWH}	5	100	40	-	100	40	-	ns
		10	50	20	-	-	-	-	ns
Data Available Valid Delay	t_{DAL}	5	-	260	500	-	260	500	ns
		10	-	130	250	-	-	-	ns
Data Available Invalid Delay	t_{DAH}	5	-	70	150	-	70	150	ns
		10	-	35	75	-	-	-	ns
Scan Count Delay (Non-Repeat)	t_{CD1}	5	-	850	1900	-	850	1900	ns
		10	-	425	950	-	-	-	ns
Data Out Valid Delay	t_{CDV}	5	-	120	250	-	120	250	ns
		10	-	60	125	-	-	-	ns
Data Out Hold Time	t_{CDH}	5	-	100	200	-	100	200	ns
		10	-	50	100	-	-	-	ns
Repeat Valid Delay	t_{RPL}	5	-	150	400	-	150	400	ns
		10	-	75	200	-	-	-	ns
Repeat Invalid Delay	t_{RPH}	5	-	350	700	-	350	700	ns
		10	-	170	350	-	-	-	ns

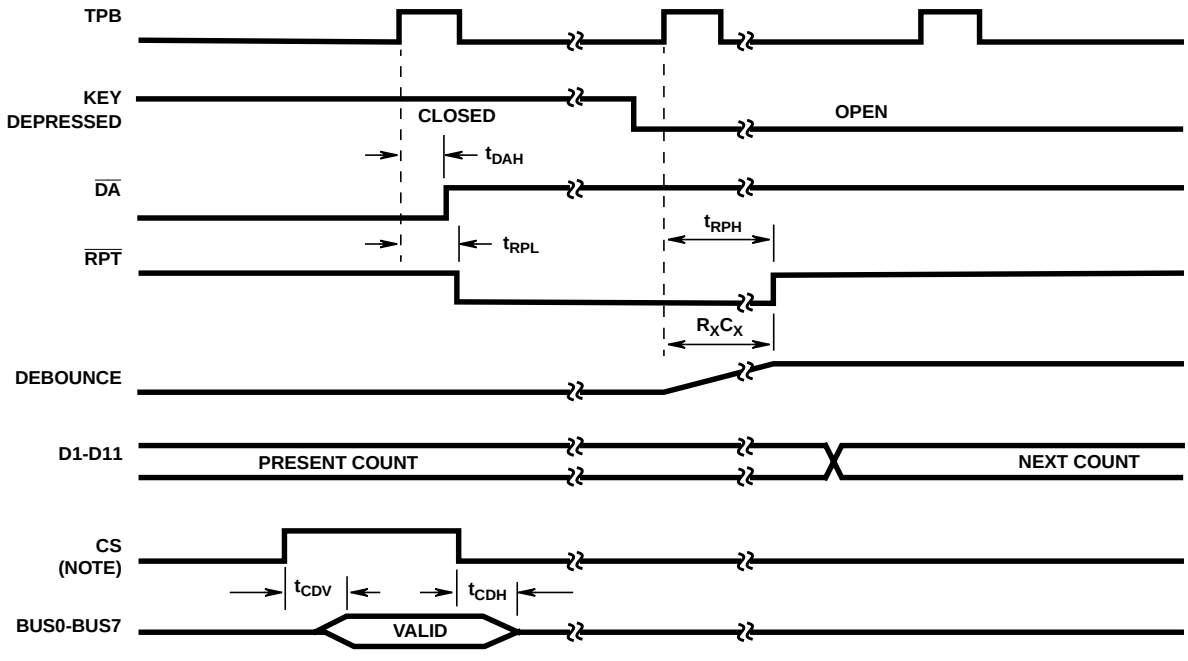
NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. $t_{CC} = t_{CWH} + t_{CWL}$
   $t_{CWL} = t_{CD1} + KC$
   k = 0.9ns per pF
   c = Keyboard capacitance (pF)



NOTE: CS = $\overline{CS1}$ • CS2 • CS3 • CS4
$\overline{CS1}$, CS2, CS3 = (CPU N-LINES)
CS4 ($\overline{MRD}$) is High for CPU Input Instruction

FIGURE 3. CDP1871A DYNAMIC TIMING DIAGRAM (NON-REPEAT)



NOTE: CS = $\overline{CS1}$ • CS2 • CS3 • CS4
$\overline{CS1}$, CS2, CS3 = (CPU N-LINES)
CS4 ($\overline{MRD}$) is High for CPU Input Instruction

FIGURE 4. FIGURE 4. CDP1871A DYNAMIC TIMING DIAGRAM (REPEAT)

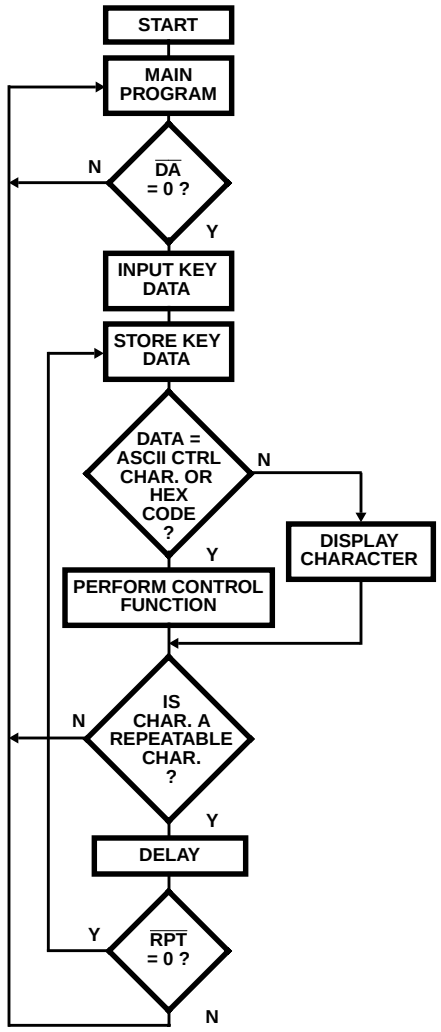


FIGURE 5. TYPICAL SYSTEM SOFTWARE FLOWCHART FOR CDP1871A, CDP1871AC

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