# CDP1855, CDP1855C

## 8-Bit Programmable Multiply/Divide Unit

March 1997

### Features

- **Cascadable Up to 4 Units for 32-Bit by 32-Bit Multiply or 64 ÷ 32-Bit Divide**
- **8-Bit by 8-Bit Multiply or 16 ÷ 8-Bit Divide in 5.6μs at 5V or 2.8μs at 10V**
- **Direct Interface to CDP1800-Series Microprocessors**
- **Easy Interface to Other 8-Bit Microprocessors**
- **Significantly Increases Throughput of Microprocessor Used for Arithmetic Calculations**

### Ordering Information

| PACKAGE | TEMP. RANGE | 5V | 10V | PKG. NO. |
|---|---|---|---|---|
| PDIP | -40°C to +85°C | CDP1855CE | CDP1855E | E28.6 |
| Burn-In | | CDP1855CEX | - | E28.6 |
| SBDIP | -40°C to +85°C | CDP1855CD | CDP1855D | D28.6 |
| Burn-In | | CDP1855CDX | - | D28.6 |

### Description

The CDP1855 and CDP1855C are CMOS 8-bit multiply/divide units which can be used to greatly increase the capabilities of 8-bit microprocessors. They perform multiply and divide operations on unsigned, binary operators. In general, microprocessors do not contain multiply or divide instructions and even efficiently coded multiply or divide subroutines require considerable memory and execution time. These multiply/divide units directly interface to the CDP1800-series microprocessors via the N-lines and can easily be configured to fit in either the memory or I/O space of other 8-bit microprocessors.

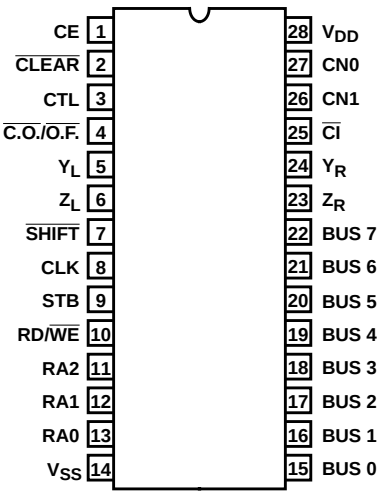
The multiple/divide unit is based on a method of multiplying by add and shift right operations and dividing by subtract and shift left operations. The device is structured to permit cascading identical units to handle operands up to 32 bits.

The CDP1855 and CDP1855C are functionally identical. They differ in that the CDP1855 has a recommended operating voltage range of 4V to 10.5V, and the CDP1855C, a recommended operating voltage range of 4V to 6.5V.

The CDP1855 and CDP1855C types are supplied in a 28 lead hermetic dual-in-line ceramic package (D suffix) and in a 28 lead dual-in-line plastic package (E suffix). The CDP1855C is also available in chip form (H suffix).

### Pinout

**28 LEAD DIP**
TOP VIEW




### Circuit Configuration

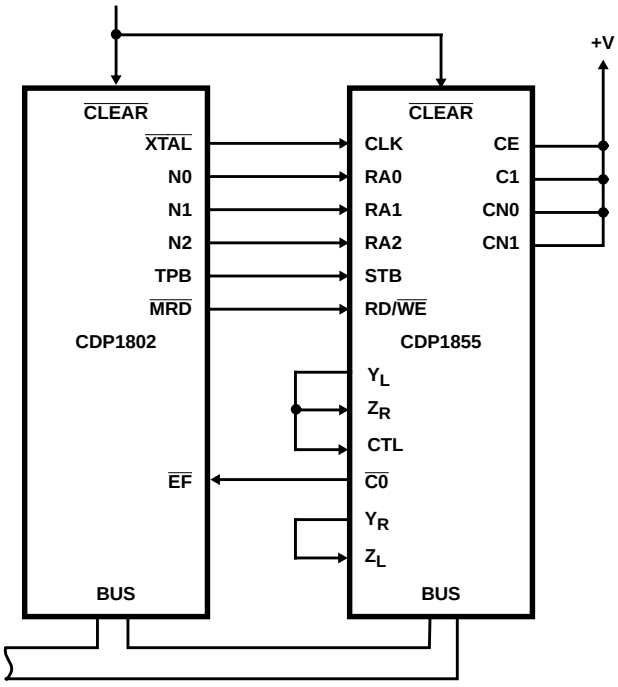



**FIGURE 1. MDU ADDRESSED AS I/O DEVICE**

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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## Absolute Maximum Ratings

DC Supply Voltage Range, ($V_{DD}$)
(All voltage values referenced to $V_{SS}$ terminal)
CDP1855 . . . . . -0.5V to +11V
CDP1855C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to $V_{DD}$ +0.5V
DC Input Current, Any One Input. . . . . ±10mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ ($^{o}$C/W) | $\theta_{JC}$ ($^{o}$C/W) |
|---|---|---|
| PDIP Package | 55 | N/A |
| SBDIP Package | 50 | 12 |

Device Dissipation Per Output Transistor
For $T_A$ = Full Package-Temperature Range
(All Package Types) . . . . . 100mW
Operating Temperature Range ($T_A$) . . . . . -40$^{o}$C to +85$^{o}$C
Storage Temperature Range ($T_{STg}$) . . . . . -65$^{o}$C to +150$^{o}$C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265$^{o}$C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Static Electrical Specifications At $T_A$ = -40 to +85$^{o}$C, $V_{DD}$ ±10%, Unless Otherwise Specified

| PARAMETER | | CONDITIONS $V_O$ (V) | CONDITIONS $V_{IN}$ (V) | CONDITIONS $V_{DD}$ (V) | LIMITS CDP1855 MIN | LIMITS CDP1855 (NOTE1) TYP | LIMITS CDP1855 MAX | LIMITS CDP1855C MIN | LIMITS CDP1855C (NOTE1) TYP | LIMITS CDP1855C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Quiescent Device Current | $I_{DD}$ | - | 0, 5 | 5 | - | 0.01 | 50 | - | 0.02 | 200 | µA |
| | | - | 0, 10 | 10 | - | 1 | 200 | - | - | - | µA |
| Output Low Drive (Sink) Current | $I_{OL}$ | 0.4 | 0, 5 | 5 | 1.6 | 3.2 | - | 1.6 | 3.2 | - | mA |
| | | 0.5 | 0, 10 | 10 | 2.6 | 5.2 | - | - | - | - | mA |
| Output High Drive (Source) Current | $I_{OH}$ | 4.6 | 0, 5 | 5 | -1.15 | -2.3 | - | -1.15 | -2.3 | - | mA |
| | | 9.5 | 0, 10 | 10 | -2.6 | -5.2 | - | - | - | - | mA |
| Output Voltage Low Level (Note 2) | $V_{OL}$ | - | 0, 5 | 5 | - | 0 | 0.1 | - | 0 | 0.1 | V |
| | | - | 0, 10 | 10 | - | 0 | 0.1 | - | - | - | V |
| Output Voltage High Level (Note 2) | $V_{OH}$ | - | 0, 5 | 5 | 4.9 | 5 | - | 4.9 | 5 | - | V |
| | | - | 0, 10 | 10 | 9.9 | 10 | - | - | - | - | V |
| Input Low Voltage | $V_{IL}$ | 0.5, 4.5 | - | 5 | - | - | 1.5 | - | - | 1.5 | V |
| | | 0.5, 9.5 | - | 10 | - | - | 3 | - | - | - | V |
| Input High Voltage | $V_{IH}$ | 0.5, 4.5 | - | 5 | 3.5 | - | - | 3.5 | - | - | V |
| | | 0.5, 9.5 | - | 10 | 7 | - | - | - | - | - | V |
| Input Leakage Current | $I_{IN}$ | - | 0, 5 | 5 | - | - | ±1 | - | - | ±1 | µA |
| | | - | 0, 10 | 10 | - | - | ±1 | - | - | - | µA |
| Three-State Output Leakage Current | $I_{OUT}$ | 0, 5 | 0, 5 | 5 | - | - | ±1 | - | - | ±1 | µA |
| | | 0, 10 | 0, 10 | 10 | - | - | ±10 | - | - | - | µA |
| Operating Current (Note 3) | $I_{DD1}$ | - | 0, 5 | 5 | - | 1.5 | - | - | 1.5 | 3 | mA |
| | | - | 0, 10 | 10 | - | 6 | 12 | - | - | - | mA |
| Input Capacitance | $C_{IN}$ | - | - | - | - | 5 | 7.5 | - | 5 | 7.5 | pF |
| Output Capacitance | $C_{OUT}$ | - | - | - | - | 10 | 15 | - | 10 | 15 | pF |

NOTES:

1. Typical values are for $T_A$ = +25$^{o}$C and nominal $V_{DD}$.
2. $I_{OL}$ = $I_{OH}$ = 1µA
3. Operating current is measured at 3.2MHz with open outputs.

**Recommended Operating Conditions** At $T_A$ = Full package temperature range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

| PARAMETER | $V_{DD}$ (V) | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|
| | | CDP1855 | | CDP1855C | | |
| | | MIN | MAX | MIN | MAX | |
| DC Operating Voltage Range | - | 4 | 10.5 | 4 | 6.5 | V |
| Input Voltage Range | - | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | V |
| Maximum Clock Input Frequency | 5 | 3.2 | - | 3.2 | - | MHz |
| | 10 | 6.4 | - | - | - | MHz |
| Minimum 8 x 8 Multiply (16 ÷ 8 Divide) Time | 5 | - | 5.6 | - | 5.6 | µs |
| | 10 | - | 2.8 | - | - | µs |

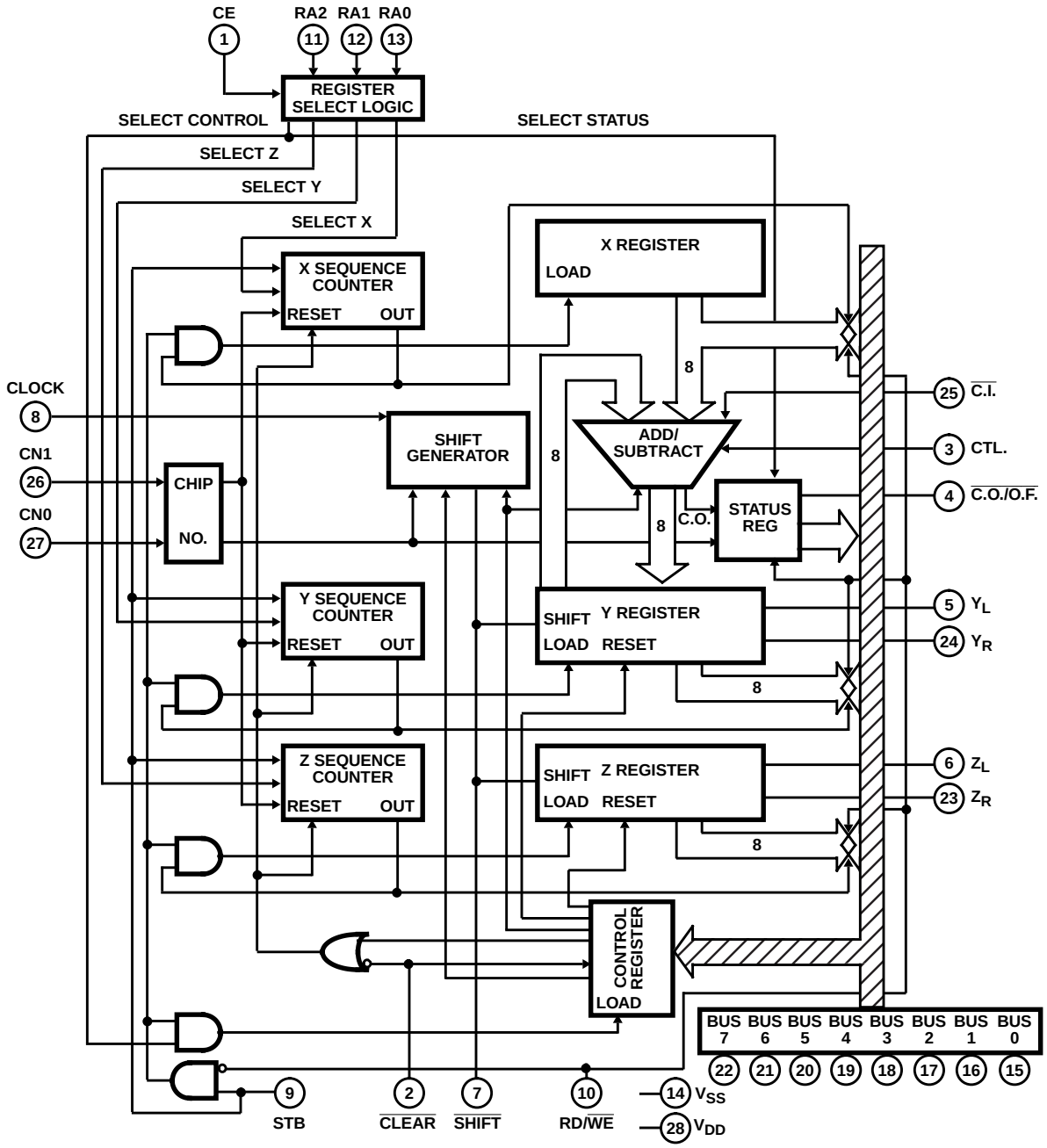



**FIGURE 2. BLOCK DIAGRAM OF CDP1855 AND CDP1855C**

## Functional Description

The CDP1855 is a multiply-divide unit (MDU) designed to be compatible with CDP1800 series microprocessor systems. It can, in fact, be interfaced to most 8-bit microprocessors (see Figure 5). The CDP1855 performs binary multiply or divide operations as directed by the microprocessor. It can do a 16N-bit by 8N-bit divide yielding a 8N-bit result plus and 8N-bit remainder. The multiply is an 8N-bit by 8N-bit operation with a 16N-bit result. The "N" represent the number of cascaded CDP1855's and can be 1, 2, 3 or 4. All operations require 8N + 1 shift pulses (See "DELAY NEEDED WITH AND WITHOUT PRESCALER").

The CDP1855 contains three registers, X, Y, and Z, which are loaded with the operands prior to an operation and contain the results at the completion. In addition, the control register must be loaded to initiate a multiply or divide. There is also a status register which contains an overflow flag as shown in the "CONTROL REGISTER BIT ASSIGNMENT TABLE". The register address lines (RA0-RA1) are used to select the appropriate register for loading or reading. The RD/$\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (See "CONTROL TRUTH TABLE").

When multiple MDU's are cascaded, the loading of each register is done sequentially. For example, the first selection of register X for loading loads the most significant CDP1855, the second loads the next significant, and so on. Registers are also read out sequentially. This is accomplished by internal counters on each MDU which are decremented by STB during each register selection. When the counter matches the chip number (CN1, CN0 lines), the device is selected. These counters must be cleared with a clear on pin 2 or with bit 6 in the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE") in order to start each sequence of accesses with the most significant device.

The CDP1855 has a built in clock prescaler which can be selected via bit 7 in the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable clock frequency is not readily available. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDU's as defined by bits 4 and 5 of the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

1. For one MDU, the clock frequency is divided by 2.
2. For two MDU's the clock frequency is divided by 4.
3. For 3 or 4 MDU's, the clock frequency is divided by 8.

## Operation

### 1. Initialization and Controls

The CDP1855 must be cleared by a low on pin 2 during power-on which prevents bus contention problems at the $Y_L$, $Y_R$ and $Z_L$, $Z_R$ terminals and also resets the sequence counters and the shift pulse generator.

Prior to loading any other registers the control register must be loaded to specify the number of MDU's being used (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

Once the number of devices has been specified and the sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y, and Z registers can be loaded as defined in the "CONTROL TRUTH TABLE". All bytes of the X register can be loaded, then all bytes of the Y, and then all bytes of the Z, or they can be loaded randomly. Successive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte, as previously described. Resetting the sequence counters select the most significant MDU. In a four MDU system, loading all MDU's results in the sequence counter pointing to the first MDU again. In all other configurations (1, 2, or 3 MDU's), the sequence counter must be reset prior to each series of register reads or writes.

### 2. Divide Operation

For the divide operation, the divisor is loaded in the X register. The dividend is loaded in the Y and Z registers with the more significant half in the Y register and the less significant half in the Z register. These registers may be loaded in any order, and after loading is completed, a control word is loaded to specify a divide operation and the number of MDU's and also to reset the sequence counters and Y or Z register and select the clock option if desired. Clearing the sequence counters with bit 6 will set the MDU's up for reading the results.

The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{C.O./O.F.}$ of the most significant MDU and can also be determined by reading the status byte.

While the CDP1855 is specified to perform 16 by 8-bit divides, if the quotient of a divide operation exceeds the size of the Z register(s) (8N-bits - where N is the number of cascaded CDP1855's) the overflow bit in the Status Register will be set. Neither the quotient in Z nor the remainder in Y will represent a valid answer. This will always be the result of a division performed when the divisor (X) is equal to or less than the most significant 8N-bits of the dividend (Y).

The MDU can still be used for such computations if the divide is done in two steps. The dividend is split into two parts-the more significant 8N-bits and the less significant 8N-bits-and a divide done on each part. Each step yields an 8N-bit result for a total quotient of 16N-bits.

The first step consists of dividing the more significant 8N-bits by the divisor. This is done by clearing the Y register(s), loading the Z register(s) with the more significant 8N-bits of the dividend, and loading the X register(s) with the divisor. A division is performed and the resultant value in Z represents the more significant 8N-bits of the final quotient. The Z register(s) value must be unloaded and saved by the processor.

A second division is performed using the remainder from the first division (in Y) as the more significant 8N-bits of the dividend and the less significant half of the original dividend loaded into the Z register. The divisor in X remains unaltered and is, by definition, larger than the remainder from the first division which is in Y. The resulting value in Z becomes the less significant 8N-bits of the final quotient and the value in Y is, as usual, the remainder.

Extending this technique to more steps allows division of any size number by an 8N-bit divisor.

Note that division by zero is never permitted and must be tested for and handled in software.

The following example illustrates the use of this algorithm.

**Example:**

Assume three MDU's capable of a by 24-bit division. The problem is to divide 00F273, 491C06H by 0003B4H.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Step 1: | 000000 | , | 00F273 | / | 0003B4 | = | 000041 | R=0001BF |
| | Y | | Z(MS) | | X | | Z1 | Y1 |
| Step 2: | 0001BF | , | 491C06 | / | 0003B4 | = | 78C936 | R=00000E |
| | Y1 | | Z(LS) | | X | | Z2 | Y2 |
| Result: | 000041 | , | 78C936 | | R=00000E | | | |
| | Z1 | | Z2 | | Y2 | | | |

The Z register can simply be reset using bit 2 of the control word and another divide can be done in order to further divide the remainder.

**3. Multiply Operation**

For a multiply operation the two numbers to be multiplied are loaded in the X and Z registers. The result is in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed.

The original contents of the Y register are added to the product of X and Z. Bit 3 of the control word will reset register Y to 0 if desired.

## *Functional Description of CDP1855 Terminals*

**CE - Chip Enable (Input):**

A high on this pin enables the CDP1855 MDU to respond to the select lines. All cascaded MDU's must be enabled together. CE also controls the three-state $\overline{C.O./O.F.}$, output of the most significant MDU.

**$\overline{Clear}$ (Input):**

The CDP1855 MDU(s) must be cleared upon power-on with a low-on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

**CTL - Control (Input):**

This is an input pin. All CTL pins must be wired together and to the $Y_L$ of the most significant CDP1855 MDU and to the $Z_R$ of the least significant CDP1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

**$\overline{C.O./O.F.}$ - $\overline{Carry\ Out/Over\ Flow}$ (Output):**

This is a three-state output pin. It is the CDP1855 $\overline{Carry\ Out}$ signal and is connected to $\overline{CI}$ ($\overline{CARRY\text{-}IN}$) of the next more significant CDP1855 MDU, except for on the most significant MDU. On that MDU it is an overflow indicator and is enabled when chip enables is true. A low on this pin indicates that an overflow has occurred. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

**$Y_L$, $Y_R$ - Y-Left, Y-Right:**

These are three-state bi-directional pins for data transfer between the Y registers of cascaded CDP1855 MDU's. The $Y_R$ pin is an output and $Y_L$ is an input during a multiply and the reverse is true at all other times. The $Y_L$ pin must be connected to the $Y_R$ pin of the next more significant MDU. An exception is that the $Y_L$ pin of the most significant CDP1855 MDU must be connected to the $Z_R$ pin of the least significant MDU and to the CTL pins of all MDU's. Also the $Y_R$ pin of the least significant MDU is tied to the $Z_L$ pin of the most significant MDU.

**$Z_L$, $Z_R$ - Z-Left, Z-Right:**

These are three-state bi-directional pins for data transfers between the “Z” registers of cascaded MDU's. The $Z_R$ pin is an output and $Z_L$ is an input during a multiply and the reverse is true at all other times. The $Z_L$ pin must be tied to the $Y_R$ pin of the next more significant MDU. An exception is that the $Z_L$ in of the most significant MDU must be connected to the $Y_R$ pin of the least significant MDU. Also, the $Z_R$ pin of the least significant MDU is tied to the $Y_L$ of the most significant MDU.

**$\overline{Shift}$ - $\overline{Shift\ Clock}$:**

This is a three-state bi-directional pin. It is an output on the most significant MDU. And an input on all other MDU's. It provides the MDU system timing pulses. All $\overline{SHIFT}$ pins must be connected together for cascaded operation. A maximum of the 8N +1 shifts are required for an operation where "N" equals the number of MDU devices that are cascaded.

**CLK - Clock (Input):**

This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin if so desired, controlled by bit 7 of the control byte.

**STB - Strobe (Input):**

When RD/WE is low, data is latched from bus lines on the falling edge of this signal. It may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in CDP1800 systems.

**RD/$\overline{WE}$ - Read/$\overline{Write\ Enable}$ (Input):**

This signal defines whether the selected register is to be read from or written to. In 1800 systems use $\overline{MRD}$ if MDU's are addressed as I/O devices, $\overline{MWR}$ is used if MDU's are addressed as memory devices.

**RA2, RA1, RA0 - Register Address (Input):**

These input signals define which register is to be read from or written to. It can be seen in the "CONTROL TRUTH TABLE" that RA2 can be used as a chip enable. It is identical to the CE pin, except only CE controls the three-state $\overline{C.O./O.F.}$ on the most significant MDU. In 1800 systems use N lines if MDU's are used as I/O devices, use address lines or function of address lines if MDU's are used as memory devices.

**Bus 0 - Bus 7 - Bus Lines:**

Three-state bi-directional bus for direct interface with CDP1800 series and other 8-bit microprocessors.

**$Z_R$ - Z-Right:**

See Pin 6.

**$Y_R$ - Y-Right:**

See Pin 5.

**$\overline{CI}$- $\overline{Carry\ In}$ (Input):**

This is an input for the carry from the next less significant MDU. On the least significant MDU it must be high ($V_{DD}$) on all others it must be connected to the $\overline{CO}$ pin of the next less significant MDU.

**CN1, CN0 - Chip Number (Input):**

These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many CDP1855 MDU's are used. Then CN1 = high and CN0 = low for the next MDU and so forth.

**$V_{SS}$ - Ground:**

Power supply line.

**$V_{DD}$ - V+:**

Power supply line.

**CONTROL TRUTH TABLE**

| **INPUTS** (NOTE 1) | | | | | | |
|---|---|---|---|---|---|---|
| **CE** | **RA2 (N2)** | **RA1 (N1)** | **RA0 (N0)** | **RD/$\overline{WE}$ (MRD)** | **STB (TPB)** | **RESPONSE** |
| 0 | X | X | X | X | X | No Action (Bus Floats) |
| X | 0 | X | X | X | X | No Action (Bus Floats) |
| 1 | 1 | 0 | 0 | 1 | X | X to Bus |
| 1 | 1 | 0 | 1 | 1 | X | Z to Bus |
| 1 | 1 | 1 | 0 | 1 | X | Y to Bus |
| | | | | | | Increment Sequence Counter When STB and RD = 1 |
| 1 | 1 | 1 | 1 | 1 | X | Status to Bus |
| 1 | 1 | 0 | 0 | 0 | 1 | Load X from Bus |
| 1 | 1 | 0 | 1 | 0 | 1 | Load Z from Bus |
| 1 | 1 | 1 | 0 | 0 | 1 | Load Y from Bus |
| | | | | | | Increment Sequence Counter |
| 1 | 1 | 1 | 1 | 0 | 1 | Load Control Register |
| 1 | 1 | X | X | 0 | 0 | No Action (Bus Floats) |

NOTE:

1. ( ) = 1800 System Signals. 1 = High Level, 0 = Low Level, X = High or Low Level.

**CONTROL REGISTER BIT ASSIGNMENT TABLE**

| BUS 7 | BUS 6 | BUS 5 | BUS 4 | BUS 3 | BUS 2 | BUS 1 | BUS 0 |
|---|---|---|---|---|---|---|---|

REGISTER RESET

| B1 | B0 | OPERATION SELECT |
|---|---|---|
| 0 | 0 | No Operation |
| 0 | 1 | Multiply |
| 1 | 0 | Divide |
| 1 | 1 | Illegal State |

B2 = 1, RESET Z REGISTER
B3 = 1, RESET Y REGISTER

| B5 | B4 | NO. OF MDU's |
|---|---|---|
| 1 | 1 | One MDU |
| 1 | 0 | Two MDU's |
| 0 | 1 | Three MDU's |
| 0 | 0 | Four MDU's |

| NO. OF MDU's | SHIFT RATE |
|---|---|
| 1 | Clock ÷ 2 |
| 2 | Clock ÷ 4 |
| 3 | Clock ÷ 8 |
| 4 | Clock ÷ 8 |

B6 = 1, RESET SEQUENCE COUNTER

B7 = 1, SELECT SHIFT RATE OPTIONS: ⟶
B7 = 0, SHIFT = CLOCK FREQUENCY RATE

**STATUS REGISTER**

| | STATUS BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **OUTPUT** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | O.F. |

NOTES:

1. O.F. = 1 if overflow (only valid after a divide has been done)
2. Bits 1 - 7 are read as 0 always.

**DELAY NEEDED WITH AND WITHOUT PRESCALER**

8N + 1 Shifts/Operation at 1 Clock Cycle/Shift
N = Number of MDU's, S = Shift Rate

| | WITHOUT PRESCALER | | WITH PRESCALER | | |
|---|---|---|---|---|---|
| **NO. OF MDU's** | **SHIFTS = 8N +1 NEEDED** | (NOTE 1) **MACHINE CYCLES NEEDED** | **SHIFTS = S (8N +1) NEEDED** | (NOTE 1) **MACHINE CYCLES NEEDED** | **SHIFT RATE** |
| 1 | 9 | 2 (1 NOP) | 18 | 3 (1 NOP) | 2 |
| 2 | 17 | 2 (1 NOP) | 68 | 9 (3 NOPs) | 4 |
| 3 | 25 | 3 (1 NOP) | 200 | 25 (9 NOPs) | 8 |
| 4 | 33 | 4 (2 NOPs) | 264 | 33 (11 NOPs) | 8 |

NOTE:

1. NOP instruction is shown for machine cycles needed (3/NOP). Other instructions may be used.

## CDP1855 Interfacing Schemes

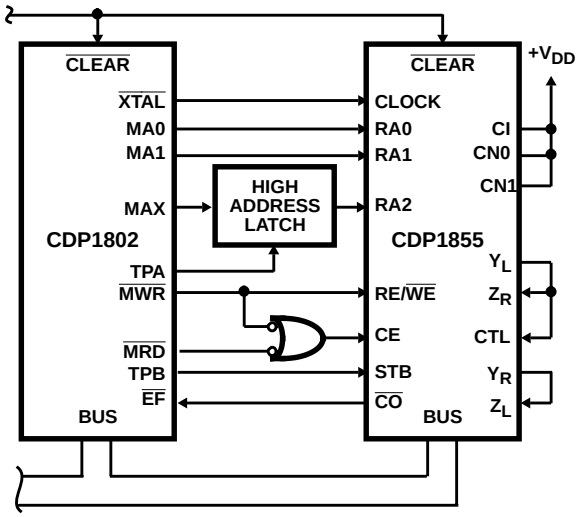



FIGURE 3. REQUIRED CONNECTION FOR MEMORY MAPPED ADDRESSING OF THE MDU

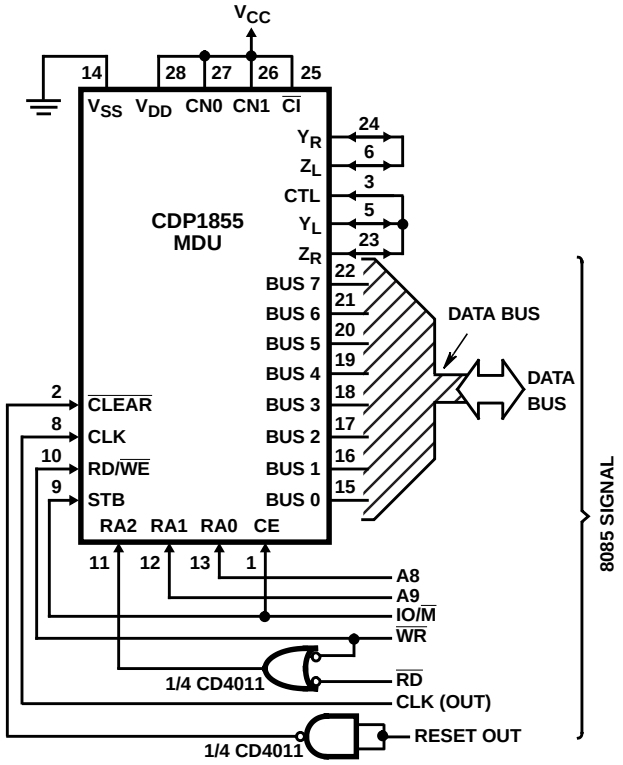



FIGURE 4. INTERFACING THE CDP1855 TO AN 8085 MICROPROCESSOR AS AN I/O DEVICE

## Programming Example for Multiplication

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$:

| MEMORY LOCATION | OP CODE | LINE NO. | ASSEMBLY LANGUAGE |
|---|---|---|---|
| 0000 | F830; | 0001 | LDI 030H |
| 0002 | A2; | 0002 | PLO R2 . . LOAD 30 INTO R2.0 |
| 0003 | F800; | 0003 | LDI 00H |
| 0005 | B2; | 0004 | PHI R2 . . LOAD 00 INTO R2.1 (R2=0030) |
| 0006 | 6758; | 0005 | OUT 7; DC 058H . . LOAD CONTROL REGISTERS |
| 0008 | ; | 0006 | . . SPECIFYING THREE MDU's |
| 0008 | ; | 0007 | . . RESET THE Y REGISTER AND |
| 0008 | ; | 0008 | . . SEQUENCE COUNTER |
| 0008 | 6420; | 0009 | OUT 4; DC 020H . . LOAD MSB OF X REGISTER |
| 000A | ; | 0010 | . . WITH 20 |
| 000A | 641F; | 0011 | OUT 4; DC 01FH . . LOAD NEXT MSB OF X REG |
| 000C | ; | 0012 | . . WITH 1F |
| 000C | 647C; | 0013 | OUT 4; DC 07CH . . LOAD LSB OF X REGISTER |
| 000E | ; | 0014 | . . WITH 7C |
| 000E | 6572; | 0015 | OUT 5; DC 072H . . LOAD MSB OF Z REGISTER |
| 0010 | ; | 0016 | . . WITH 72 |

## Programming Example for Multiplication

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$: **(Continued)**

| MEMORY LOCATION | OP CODE | LINE NO. | ASSEMBLY LANGUAGE |
|---|---|---|---|
| 0010 | 653C; | 0017 | OUT 5; DC 030H . . LOAD NEXT MSB OF Z REG |
| 0012 | ; | 0018 | . . WITH 3C |
| 0012 | 6509; | 0019 | OUT 5; DC 09H . . LOAD LSB OF Z REGISTER |
| 0014 | ; | 0020 | . . WITH 09 |
| 0014 | 6759; | 0021 | OUT 7; DC 059H . . LOAD CONTROL REGISTERS |
| 0016 | ; | 0022 | . . RESETTING Y REGISTERS |
| 0016 | ; | 0023 | . . AND SEQUENCE COUNTERS |
| 0016 | ; | 0024 | . . AND STARTING MULTIPLY |
| 0016 | ; | 0025 | . . OPERATION |
| DELAY FOR MULTIPLY TO FINISH | | | |
| 0016 | E2; | 0026 | SEX R2 |
| 0017 | 6E60; | 0027 | INP 6; IRX . . MSB OF RESULTS IS STORED |
| 0019 | ; | 0028 | . . AT LOCATION 0030 |
| 0019 | 6E60; | 0029 | INP 6; IRX |
| 001B | 6E60; | 0030 | INP 6; IRX |
| 001D | 6D60; | 0031 | INP 5; IRX |
| 001F | 6D60; | 0032 | INP 5; IRX |
| 0021 | 6D; | 0033 | INP 5 . . COMPLETE LOADING RESULT |
| 0022 | ; | 0034 | . . INTO MEMORY LOCATIONS |
| 0022 | ; | 0035 | . . 0030 TO 0035 |
| 0022 | ; | 0036 | . . RESULTS = 0E558DBA2B5C |
| 0022 | 3022; | 0037 STOP | BR STOP |
| 0024 | ; | 0038 | END |
| 0000 | | | |

The result of $201F7C_{16}$ x $723C09_{16}$ is 0E558DBA2B5C = $15760612797276_{10}$. It will be stored in memory as follows:

| LOC | BYTE |
|---|---|
| 0030 | 0E |
| 31 | 55 |
| 32 | 8D |
| 33 | BA |
| 34 | 2B |
| 35 | 5C |

**BEFORE MULTIPLY**

| | MDU1 | MDU2 | MDU3 |
|---|---|---|---|
| REGISTER X | 20 | 1F | 7C |
| REGISTER Y | 00 | 00 | 00 |
| REGISTER Z | 72 | 3C | 09 |

**AFTER MULTIPLY**

| | MDU1 | MDU2 | MDU3 |
|---|---|---|---|
| REGISTER X | 20 | 1F | 7C |
| REGISTER Y | 0E | 55 | 8D |
| REGISTER Z | BA | 2B | 5C |

## Programming Example for Division

| MEMORY LOCATION | OP CODE | LINE NO. | ASSEMBLY LANGUAGE | |
|---|---|---|---|---|
| 0000 | ; | 0001 | . . Program example for a 16-bit by 8-bit divide using 1 CDP1855 MDU | |
| 0000 | ; | 0002 | . . Gives a 16-bit answer with 8-bit remainder | |
| 0000 | ; | 0003 | | |
| 0000 | 68C22000; | 0004 | RLDI R2, 2000H | . . Answer is stored at 2000 hex |
| 0004 | ; | 0005 | | . . Register 2 points to it |
| 0004 | 68C33000; | 0006 | RLDI R3, 3000H | . . Dividend is stored at 3000 hex |
| 0008 | ; | 0007 | | . . Register 3 points to it |
| 0008 | 68C44000; | 0008 | RLDI R4, 4000H | . . Divisor is stored at 4000 hex |
| 000C | ; | 0009 | | . . Register 4 points to it |
| 000C | ; | 0010 | | |
| 000C | E067F0; | 0011 | SEX R4; OUT 7; DC OF0H | . . Write to the control register to use |
| 000F | ; | 0012 | | . . clock/2; 1MDU; reset sequence |
| 000F | ; | 0013 | | . . counter; and no operation |
| 000F | ; | 0014 | | |
| 000F | E464; | 0015 | SEX R4; OUT 4 | . . Load the divisor into the X register |
| 0011 | ; | 0016 | | |
| 0011 | E06600; | 0017 | SEX R0; OUT 6; DC 0 | . . Load 0 into the Y register |
| 0014 | E365; | 0018 | SEX R3; OUT 5 | . . Load the most significant 8 bits of |
| 0016 | ; | 0019 | | . . the dividend into the Z register |
| 0016 | ; | 0020 | | |
| 0016 | E067F2; | 0021 | SEX R0; OUT 7; DC 0F2H | . . Do the first divide, also resets the |
| 0019 | ; | 0022 | | . . sequence counter |
| 0019 | ; | 0023 | | |
| 0019 | E26D60; | 0024 | SEX R2; INP 5; IRX | . . Read and store the most significant |
| 001C | ; | 0025 | | . . 8 bits of the answer at 2000 hex |
| 001C | ; | 0026 | | |
| 001C | E067F0; | 0027 | SEX R0; OUT 7; DC 0F0H | . . Reset the sequence counter |
| 001F | ; | 0028 | | |
| 001F | E365; | 0029 | SEX R3; OUT 5 | . . Load the 8 least significant 8 bits |
| 0021 | ; | 0030 | | . . of the original dividend into the Z |
| 0021 | ; | 0031 | | . . register |
| 0021 | ; | 0032 | | |
| 0021 | E067F2; | 0033 | SEX R0; OUT 7; DC 0F2H | . . Do the second division |
| 0024 | ; | 0034 | | |
| 0024 | E26D60; | 0035 | SEX R2; INP 5; IRX | . . Read and store the least significant |
| 0027 | ; | 0036 | | . . 8 bits of the answer at 2001 hex |
| 0027 | 6E; | 0037 | INP 6 | . . Read and store the remainder at 2002 |
| 0028 | ; | 0038 | | . . hex |
| 0000 | | | | |

For the divide operation (Figure 5), the formula is:

$$\frac{Y_3Y_2Y_1Z_3Z_2Z_1}{X_3X_2X_1} = Z_3Z_2Z_1 + \frac{Y_3Y_2Y_1}{X_3X_2X_1}$$

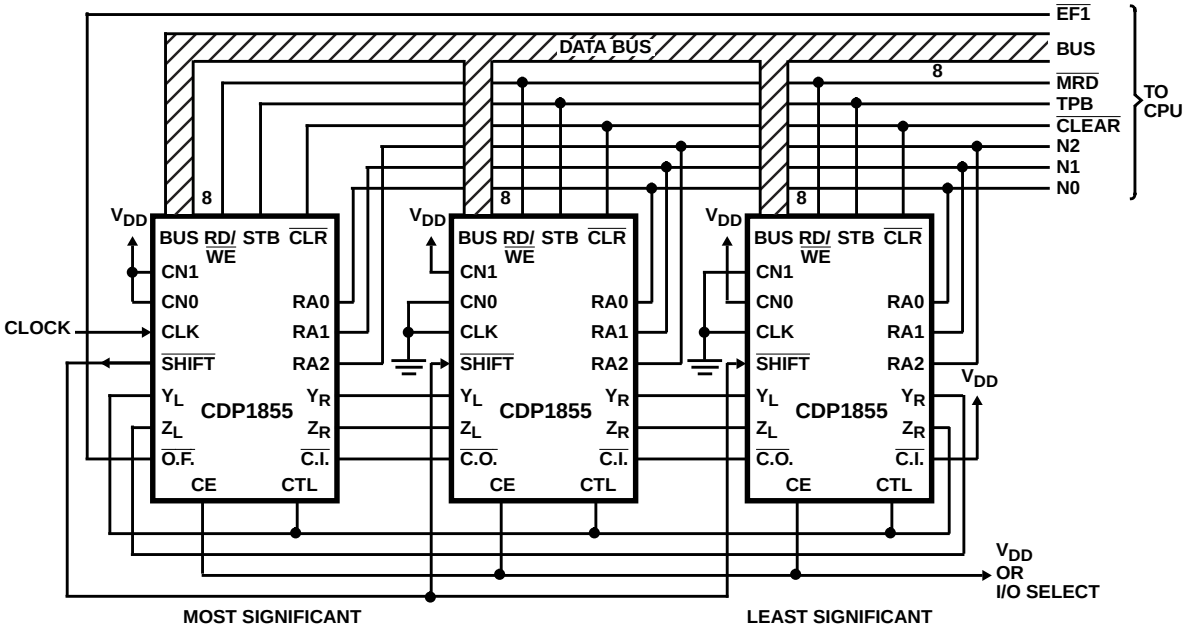



**FIGURE 5. CASCADING THREE MDU's (CDP1855) IN AN 1800 SYSTEM WITH MDU's BEING ACCESSED AS I/O PORTS IN PROGRAMMING EXAMPLE**

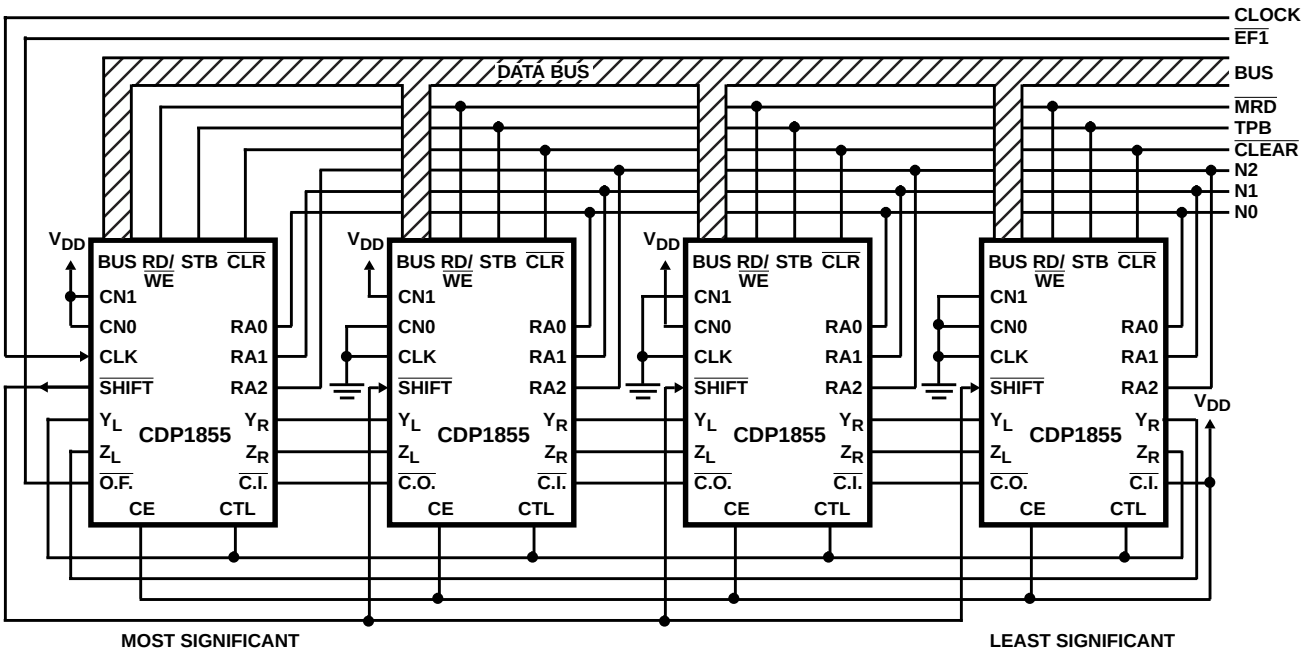



**FIGURE 6. CASCADING FOUR MDU's (CDP1855)**

**Dynamic Electrical Specifications** At $T_A$ = -40 to +85$^o$C, $V_{DD}$ ±5%, $t_R$, $t_F$ = 20ns, $V_{IH}$ = 0.7$V_{DD}$, $V_{IL}$ = 0.3$V_{DD}$, $C_L$ = 100pF (See Figure 7)

| (NOTE 1) PARAMETER | | $V_{DD}$ (V) | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | CDP1855 | | | CDP1855C | | | |
| | | | MIN | (NOTE 2) TYP | MAX | MIN | (NOTE 2) TYP | MAX | |
| **OPERATION TIMING** | | | | | | | | | |
| Maximum Clock Frequency (Note 3) | | 5 | 3.2 | 4 | - | 3.2 | 4 | - | MHz |
| | | 10 | 6.4 | 8 | - | - | - | - | MHz |
| Maximum Shift Frequency (1 Device) (Note 4) | | 5 | 1.6 | 2 | - | 1.6 | 2 | - | MHz |
| | | 10 | 3.2 | 4 | - | - | - | - | MHz |
| Minimum Clock Width | $t_{CLK0}$ $t_{CLK1}$ | 5 | - | 100 | 150 | - | 100 | 150 | ns |
| | | 10 | - | 50 | 75 | - | - | - | ns |
| Minimum Clock Period | $t_{CLK}$ | 5 | - | 250 | 312 | - | 250 | 312 | ns |
| | | 10 | - | 125 | 156 | - | - | - | ns |
| Clock to Shift Propagation Delay | $t_{CSH}$ | 5 | - | 200 | 300 | - | 200 | 300 | ns |
| | | 10 | - | 100 | 150 | - | - | - | ns |
| Minimum C.I. to Shift Setup | $t_{SU}$ | 5 | - | 50 | 67 | - | 50 | 67 | ns |
| | | 10 | - | 25 | 33 | - | - | - | ns |
| C.O. from Shift Propagation Delay | $t_{PLH}$ $t_{PHL}$ | 5 | - | 450 | 600 | - | 450 | 600 | ns |
| | | 10 | - | 225 | 300 | - | - | - | ns |
| Minimum C.I. from Shift Hold | $t_H$ | 5 | - | 50 | 75 | - | 50 | 75 | ns |
| | | 10 | - | 25 | 40 | - | - | - | ns |
| Minimum Register Input Setup | $t_{SU}$ | 5 | - | -20 | 10 | - | -20 | 10 | ns |
| | | 10 | - | -10 | 10 | - | - | - | ns |
| Register after Shift Delay | $t_{PLH}$ $t_{PHL}$ | 5 | - | 400 | 600 | - | 400 | 600 | ns |
| | | 10 | - | 200 | 300 | - | - | - | ns |
| Minimum Register after Shift Hold | $t_H$ | 5 | - | 50 | 100 | - | 50 | 100 | ns |
| | | 10 | - | 25 | 50 | - | - | - | ns |
| C.O. from C.I. Propagation Delay | $t_{PLH}$ $t_{PHL}$ | 5 | - | 100 | 150 | - | 100 | 150 | ns |
| | | 10 | - | 50 | 75 | - | - | - | ns |
| Register from C.I. Propagation Delay | $t_{PLH}$ $t_{PHL}$ | 5 | - | 80 | 120 | - | 80 | 120 | ns |
| | | 10 | - | 40 | 60 | - | - | - | ns |

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for $T_A$ = 25$^o$C and nominal voltages.
3. Clock frequency and pulse width are given for systems using the internal clock option of the CDP1855. Clock frequency equals shift frequency for systems not using the internal clock option.
4. Shift period for cascading of devices is increased by an amount equal to the $\overline{C.I.}$ to $\overline{C.O.}$ Propagation Delay for each device added.

**Dynamic Electrical Specifications** At $T_A$ = -40 to +85°C, $V_{DD}$ ±5%, $t_R$, $t_F$ = 20ns, $V_{IH}$ = 0.7$V_{DD}$, $V_{IL}$ = 0.3$V_{DD}$, $C_L$ = 100pF (See Figure 8)

| (NOTE 1) PARAMETER | | $V_{DD}$ (V) | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | CDP1855 | | | CDP1855C | | | |
| | | | MIN | (NOTE 2) TYP | MAX | MIN | (NOTE 2) TYP | MAX | |
| **WRITE CYCLE** | | | | | | | | | |
| Minimum Clear Pulse Width | $t_{\overline{CLR}}$ | 5 | - | 50 | 75 | - | 50 | 75 | ns |
| | | 10 | - | 25 | 40 | - | - | - | ns |
| Minimum Write Pulse Width | $t_{WW}$ | 5 | - | 150 | 225 | - | 150 | 225 | ns |
| | | 10 | - | 75 | 115 | - | - | - | ns |
| Minimum Data-In-Setup | $t_{DSU}$ | 5 | - | -75 | 0 | - | -75 | 0 | ns |
| | | 10 | - | -40 | 0 | - | - | - | ns |
| Minimum Data-In-Hold | $t_{DH}$ | 5 | - | 50 | 75 | - | 50 | 75 | ns |
| | | 10 | - | 25 | 40 | - | - | - | ns |
| Minimum Address to Write Setup | $t_{ASU}$ | 5 | - | 50 | 75 | - | 50 | 75 | ns |
| | | 10 | - | 25 | 40 | - | - | - | ns |
| Minimum Address after Write Hold | $t_{AH}$ | 5 | - | 50 | 75 | - | 50 | 75 | ns |
| | | 10 | - | 25 | 40 | - | - | - | ns |

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for $T_A$ = 25°C and nominal voltages.

**Dynamic Electrical Specifications** At $T_A$ = -40 to +85°C, $V_{DD}$ ±5%, $t_R$, $t_F$ = 20ns, $V_{IH}$ = 0.7$V_{DD}$, $V_{IL}$ = 0.3$V_{DD}$, $C_L$ = 100pF (See Figure 9)

| (NOTE 1) PARAMETER | | $V_{DD}$ (V) | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | CDP1855 | | | CDP1855C | | | |
| | | | MIN | (NOTE 2) TYP | MAX | MIN | (NOTE 2) TYP | MAX | |
| **READ CYCLE** | | | | | | | | | |
| CE to Data Out Active | $t_{CDO}$ | 5 | - | 200 | 300 | - | 200 | 300 | ns |
| | | 10 | - | 100 | 150 | - | - | - | ns |
| CE to Data Access | $t_{CA}$ | 5 | - | 300 | 450 | - | 300 | 450 | ns |
| | | 10 | - | 150 | 225 | - | - | - | ns |
| Address to Data Access | $t_{AA}$ | 5 | - | 300 | 450 | - | 300 | 450 | ns |
| | | 10 | - | 150 | 225 | - | - | - | ns |
| Data Out Hold after CE | $t_{DOH}$ | 5 | 50 | 150 | 225 | 50 | 150 | 225 | ns |
| | | 10 | 25 | 75 | 115 | - | - | - | ns |
| Data Out Hold after Read | $t_{DOH}$ | 5 | 50 | 150 | 225 | 50 | 150 | 225 | ns |
| | | 10 | 25 | 75 | 115 | - | - | - | ns |
| Read to Data Out Active | $t_{RDO}$ | 5 | - | 200 | 300 | - | 200 | 300 | ns |
| | | 10 | - | 100 | 150 | - | - | - | ns |
| Read to Data Access | $t_{RA}$ | 5 | - | 200 | 300 | - | 200 | 300 | ns |
| | | 10 | - | 100 | 150 | - | - | - | ns |

**Dynamic Electrical Specifications** At $T_A$ = -40 to +85°C, $V_{DD}$ ±5%, $t_R$, $t_F$ = 20ns, $V_{IH}$ = 0.7$V_{DD}$, $V_{IL}$ = 0.3$V_{DD}$, $C_L$ = 100pF (See Figure 9) **(Continued)**

| (NOTE 1) PARAMETER | | $V_{DD}$ (V) | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | CDP1855 | | | CDP1855C | | | |
| | | | MIN | (NOTE 2) TYP | MAX | MIN | (NOTE 2) TYP | MAX | |
| Strobe to Data Access | $t_{SA}$ | 5 | 50 | 200 | 300 | 50 | 200 | 300 | ns |
| | | 10 | 25 | 100 | 150 | - | - | - | ns |
| Minimum Strobe Width | $t_{SW}$ | 5 | - | 150 | 225 | - | 150 | 225 | ns |
| | | 10 | - | 75 | 115 | - | - | - | ns |

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for $T_A$ = 25°C and nominal voltages.

## Timing Diagrams

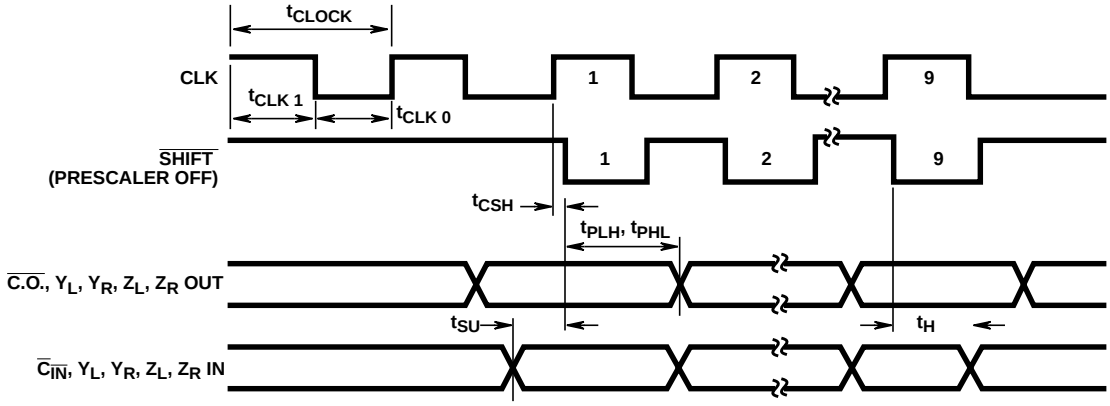



**FIGURE 7. OPERATION TIMING DIAGRAM**

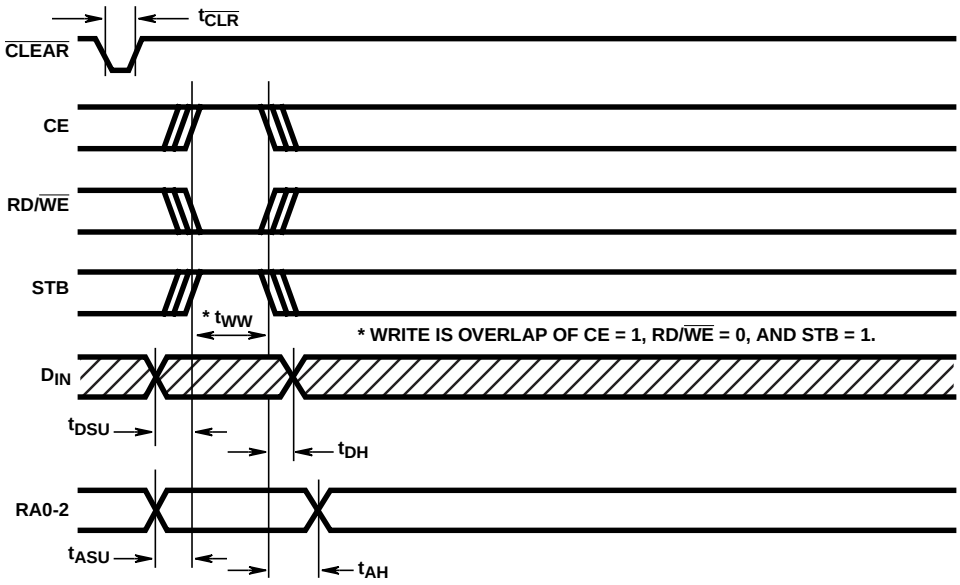



**FIGURE 8. WRITE TIMING DIAGRAM**

## Timing Diagrams (Continued)

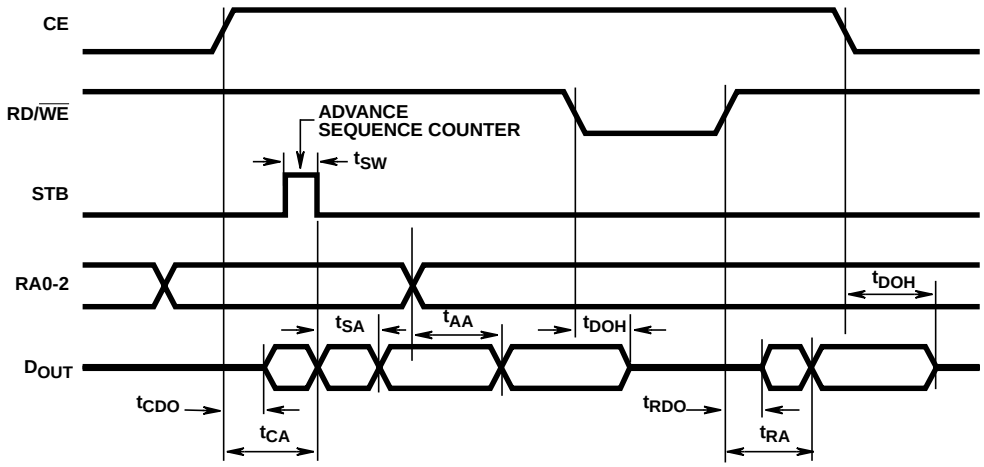



**FIGURE 9. READ TIMING DIAGRAM**

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