Data Sheet

CADEKA
Amplify the Human Experience

CDK3400/CDK3401

10-bit, 100/150MSPS, Triple Video DACs

FEATURES

- 10-bit resolution
- 150 megapixels per second
- ±0.1% linearity error
- Sync and blank controls
- 1.0V_{pp} video into 37.5Ω or 75Ω load
- Internal bandgap voltage reference
- Double-buffered data for low distortion
- TTL-compatible inputs
- Low glitch energy
- Single +5V power supply

APPLICATIONS

- Video signal conversion
  - RGB
  - YC_BC_R
  - Composite, Y, C
- Multimedia systems
- Image processing
- True-color graphics systems (1 billion colors)
- Broadcast television equipment
- High-Definition Television (HDTV) equipment
- Direct digital synthesis

General Description

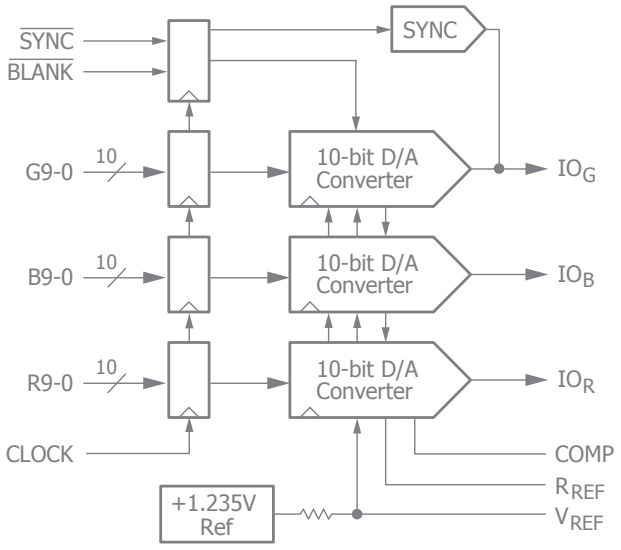
CDK3400/3401 products are low-cost triple D/A converters that are tailored to fit graphics and video applications where speed is critical. Two speed grades are available: CDK3400 at 100MSPS and CDK3401 at 150MSPS.

TTL-level inputs are converted to analog current outputs that can drive 25-37.5Ω loads corresponding to doubly-terminated 50-75Ω loads. A sync current following $\overline{SYNC}$ input timing is added to the IO_G output. $\overline{BLANK}$ will override RGB inputs, setting IO_G, IO_B and IO_R currents to zero when $\overline{BLANK}$ = L. Although appropriate for many applications, the internal 1.235V reference voltage can be overridden by the V_{REF} input.

Few external components are required, just the current reference resistor, current output load resistors, and decoupling capacitors.

Package is a 48-lead TQFP. Fabrication technology is CMOS. Performance is guaranteed from 0 to 70°C.

Block Diagram



Ordering Information

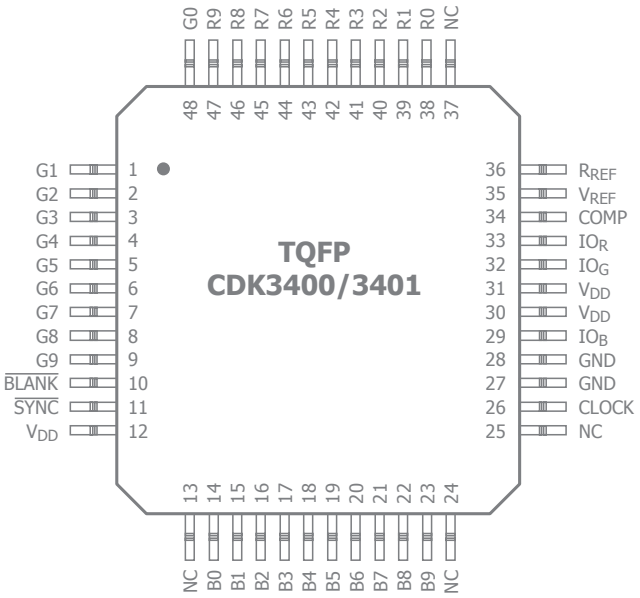
Part Number	Package	Pb-Free	RoHS Compliant	Operating Temp Range	Packaging Method	Package Quantity
CDK3400CTQ48	TQFP-48	Yes	Yes	0°C to +70°C	Tray	250
CDK3400CTQ48Y	TQFP-48	Yes	Yes	0°C to +70°C	Tray	1,250
CDK3401CTQ48	TQFP-48	Yes	Yes	0°C to +70°C	Tray	250
CDK3401CTQ48Y	TQFP-48	Yes	Yes	0°C to +70°C	Tray	1,250

Moisture sensitivity level for all parts is MSL-3.

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Pin Configuration

TQFP-48



Pin Assignments

Pin No.	Pin Name	Description
Clock and Pixel I/O		
26	CLK	Clock Input
47-37	R9-0	Red Pixel Data Inputs
48, 9–1	G9-0	Green Pixel Data Inputs
23–14	B9-0	Blue Pixel Data Inputs
Controls		
11	$\overline{\text{SYNC}}$	Sync Pulse Input
10	$\overline{\text{BLANK}}$	Blanking Input
Video Outputs		
33	IOR	Red Current Output
32	IOG	Green Current Output
29	IOB	Blue Current Output
Voltage Reference		
35	V_{REF}	Voltage Reference Output/Input
36	R_{REF}	Current-Setting Resistor
34	COMP	Compensation Capacitor
Power and Ground		
12, 30, 31	V_{DD}	Power Supply
27, 28	GND	Ground

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Power Supply Voltage			
V_{DD} (Measured to GND)	-0.5	7.0	V
Inputs			
Applied Voltage (measured to GND)(2)	-0.5	V_{DD} + 0.5	V
Forced Current(3,4)	-10.0	10.0	mA
Outputs			
Applied Voltage (measured to GND)(2)	-0.5	V_{DD} + 0.5	V
Forced Current(3,4)	-60.0	60.0	mA
Short Circuit Duration (single output in HIGH state to GND)		Infinite	sec
Temperature			
Operating, Ambient	-20	110	°C
Junction		150	°C
Lead Soldering (10 seconds)		300	°C
Vapor Phase Soldering (1 minute)		220	°C
Storage	-65	150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_S	Conversion Rate	CDK3400			100	MSPS
		CDK3401			150	MSPS
t_{PWH}	CLK Pulsewidth, HIGH	CDK3400	3.1			ns
		CDK3401	2.5			ns
t_{PWL}	CLK Pulsewidth, LOW	CDK3400	3.1			ns
		CDK3401	2.5			ns
t_W	CLK Pulsewidth	CDK3400	10			ns
		CDK3401	6.6			ns
t_S	Input Data Setup Time		1.7			ns
t_h	Input Date Hold Time		0			ns
V_{REF}	Reference Voltage, External		1.0	1.235	1.5	V
C_C	Compensation Capacitor			0.1		µF
R_L	Output Load			37.5		Ω
V_{IH}	Input Voltage, Logic HIGH		2.0		VDD	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
T_A	Ambient Temperature, Still Air		0		70	°C

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Electrical Characteristics

(T_A = 25°C, V_{DD} = +5V, V_{REF} = 1.235V, R_L = 37.5Ω, R_{REF} = 540Ω; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current(1)	V_{DD} = 5.25V, T_A = 0°C			125	mA
PD	Total Power Dissipation(1)	V_{DD} = 5.25V, T_A = 0°C			655	mW
R_O	Output Resistance			100		kΩ
C_O	Output Capacitance	I_{OUT} = 0mA			30	pF
I_{IH}	Input Current, HIGH	V_{DD} = 5.25V, V_{IN} = 2.4V			-5	µA
I_{IL}	Input Current, LOW	V_{DD} = 5.25V, V_{IN} = 0.4V			5	µA
I_{REF}	V_{REF} Input Bias Current			0	±100	µA
V_{REF}	Reference Voltage Output			1.235		V
V_{OC}	Output Compliance	Referred to V_{DD}	-0.4	0	+1.5	V
C_{DI}	Digital Input Capacitance			4	10	pF

Notes:
1. 100% tested at 25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

Switching Characteristics

(T_A = 25°C, V_{DD} = +5V, V_{REF} = 1.235V, R_L = 37.5Ω, R_{REF} = 590Ω; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_D	Clock to Output Delay	V_{DD} = 4.75V, T_A = 0°C		10	15	ns
t_{SKEW}	Output Skew			1	2	ns
t_R	Output Risetime	10% to 90% of Full Scale			3	ns
t_F	Output Falltime	90% to 10% of Full Scale			3	ns

Notes:
1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

System Performance Characteristics

(T_A = 25°C, V_{DD} = +5V, V_{REF} = 1.235V, R_L = 37.5Ω, R_{REF} = 590Ω; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INL	Integral Linearity Error			±0.1	±0.25	%/FS
DNL	Differential Linearity Error			±0.1	±0.25	%/FS
E_{DM}	DAC to DAC Matching			3	10	%
PSRR	Power Supply Rejection Ratio				0.05	%/%

Notes:
1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

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Table 1. Output Voltage vs. Input Code, $\overline{SYNC}$ and $\overline{BLANK}$, V_{REF} = 1.235V, R_{REF} = 590Ω, R_L = 37.5Ω

RGB9-0 (MSB...LSB)	BLUE AND RED D/AS			GREEN D/A		
	$\overline{SYNC}$	$\overline{BLANK}$	VOUT	$\overline{SYNC}$	$\overline{BLANK}$	VOUT
11 1111 1111	X	1	0.7140	1	1	1.0000
11 1111 1111	X	1	0.7140	0	1	0.7140
11 1111 1110	X	1	0.7134	1	1	0.9994
11 1111 1101	X	1	0.7127	1	1	0.9987
•	•	•	•	•	•	•
•	•	•	•	•	•	•
10 0000 0000	X	1	0.3843	1	1	0.6703
01 1111 1111	X	1	0.3837	1	1	0.6697
•	•	•	•	•	•	•
•	•	•	•	•	•	•
00 0000 0010	X	1	0.0553	1	1	0.3413
00 0000 0001	X	1	0.0546	1	1	0.3406
00 0000 0000	X	1	0.0540	1	1	0.3400
XX XXXX XXXX	X	0	0.0000	1	0	0.2860
XX XXXX XXXX	X	0	0.0000	0	0	0.0000

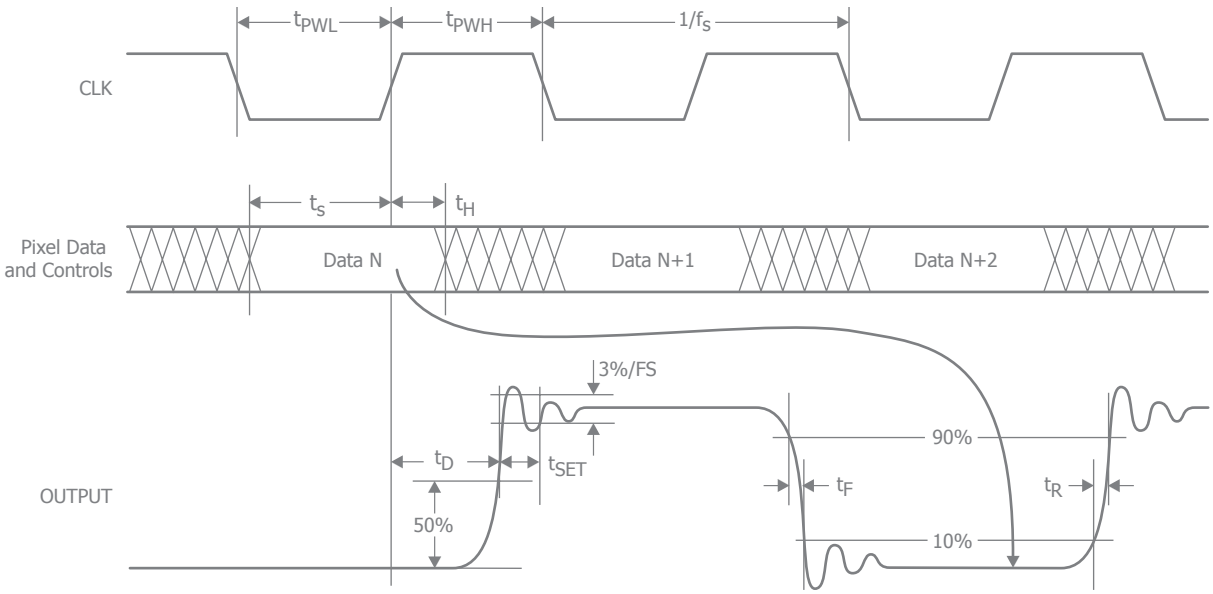


Figure 1. CDK3400/3401 Timing Diagram

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Functional Description

Within the CDK3400/3401 are three identical 10-bit D/A converters, each with a current source output. External loads are required to convert the current to voltage outputs. Data inputs RGB7-0 are overridden by the $\overline{BLANK}$ input. $\overline{SYNC}$ = H activates, sync current from I_{OS} for sync-on-green video signals.

Digital Inputs

All digital inputs are TTL-compatible. Data is registered on the rising edge of the CLK signal. Following one stage of pipeline delay, the analog output changes t_{DO} after the rising edge of CLK.

Clock Input - CLK

The clock input is TTL-compatible and all pixel data is registered on the rising edge of CLK. It is recommended that CLK be driven by a dedicated TTL buffer to avoid reflection induced jitter, overshoot, and undershoot.

Pixel Data Inputs - R9-0, B9-0, G9-0

TTL-compatible Red, Green and Blue Data Inputs are registered on the rising edge of CLK.

$\overline{SYNC}$ and $\overline{BLANK}$

$\overline{SYNC}$ and $\overline{BLANK}$ inputs control the output level (Figure 2 and Table 1, on the previous page) of the D/A converters during CRT retrace intervals. $\overline{BLANK}$ forces the D/A outputs to the blanking level while $\overline{SYNC}$ = L turns off a current source that is connected to the green D/A converter. $\overline{SYNC}$ = H adds a 40 I_{RE} sync pulse to the green output, $\overline{SYNC}$ = L sets the green output to 0.0V during the sync tip. $\overline{SYNC}$ and $\overline{BLANK}$ are registered on the rising edge of CLK.

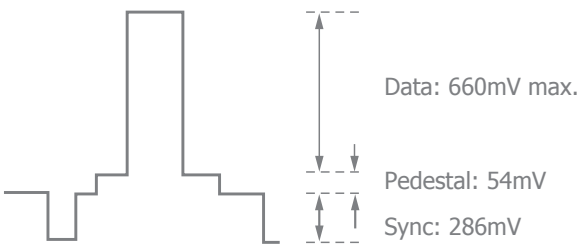


Figure 2. Normal Output Levels

$\overline{BLANK}$ gates the D/A inputs and sets the pedestal voltage. If $\overline{BLANK}$ = HIGH, the D/A inputs are added to a pedestal which offsets the current output. If $\overline{BLANK}$ = Low, data inputs and the pedestal are disabled.

Sync Pulse Input - $\overline{SYNC}$

Bringing $\overline{SYNC}$ LOW, turns off a 40 I_{RE} (7.62mA) current source which forms a sync pulse on the Green D/A converter output. $\overline{SYNC}$ is registered on the rising edge of CLK with the same pipeline latency as $\overline{BLANK}$ and pixel data. SYNC does not override any other data and should be used only during the blanking interval.

Since this is a single-supply D/A and all signals are positive-going, sync is added to the bottom of the Green D/A range. So turning $\overline{SYNC}$ OFF means turning the current source ON. When a sync pulse is desired, the current source is turned OFF. If the system does not require sync pulses from the Green D/A converter, $\overline{SYNC}$ should connected to GND.

Blanking Input - $\overline{BLANK}$

When $\overline{BLANK}$ is LOW, pixel inputs are ignored and the D/A converter outputs fall to the blanking level. $\overline{BLANK}$ is registered on the rising edge of CLK and has the same pipeline latency as $\overline{SYNC}$.

D/A Outputs

Each D/A output is a current source. To obtain a voltage output, a resistor must be connected to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

Normally, a source termination resistor of 75Ω is connected between the D/A current output pin and GND near the D/A converter. A 75Ω line may then be connected with another 75Ω termination resistor at the far end of the cable. This "double termination" presents the D/A converter with a net resistive load of 37.5Ω.

The CDK3400/3401 may also be operated with a single 75Ω terminating resistor. To lower the output voltage swing to the desired range, the nominal value of the resistor on R_{REF} should be doubled.

R, G, and B Current Outputs - IO_R, IO_G, IO_B

The R, G, and B current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M compatible levels into doubly-terminated 75Ω lines. Sync pulses may be added to the Green D/A output.

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Current-Setting Resistor - R_{REF}

Full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. Nominal value of R_{REF} is found from:

$$R_{REF} = 9.1 (V_{REF}/I_{FS})$$

where I_{FS} is the full-scale (white) output current (in amps) from the D/A converter (without sync). Sync is 0.4 * I_{FS}.

D/A full-scale (white) current may also be calculated from:

$$I_{FS} = V_{FS}/R_L$$

Where V_{FS} is the white voltage level and R_L is the total resistive load (Ω) on each D/A converter. V_{FS} is the blank to full-scale voltage.

Voltage Reference

All three D/A converters are supplied with a common voltage reference. Internal bandgap voltage reference voltage is +1.235V with a 3kΩ source resistance. An external voltage reference may be connected to the V_{REF} pin, overriding the internal voltage reference.

A 0.1µF capacitor must be connected between the COMP pin and V_{DD} to stabilize internal bias circuitry and ensure low-noise operation.

Voltage Reference Output/Input - V_{REF}

An internal voltage source of +1.235V is output on the V_{REF} pin. An external +1.235V reference may be applied here which overrides the internal reference. Decoupling V_{REF} to GND with a 0.1µF ceramic capacitor is required.

Power and Ground

Required power is a single +5.0V supply. To minimize power supply induced noise, analog +5V should be connected to V_{DD} pins with 0.1µF and 0.01µF decoupling capacitors placed adjacent to each V_{DD} pin or pin pair.

The high slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

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Equivalent Circuits

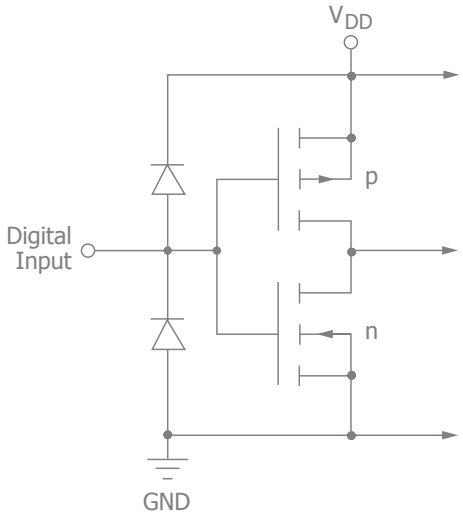


Figure 3. Equivalent Digital Input Circuit

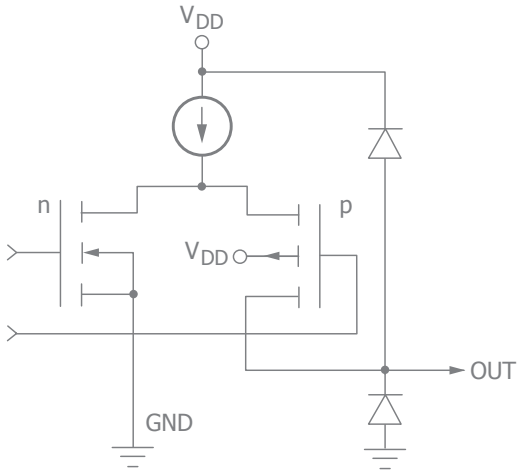


Figure 4. Equivalent Analog Output Circuit

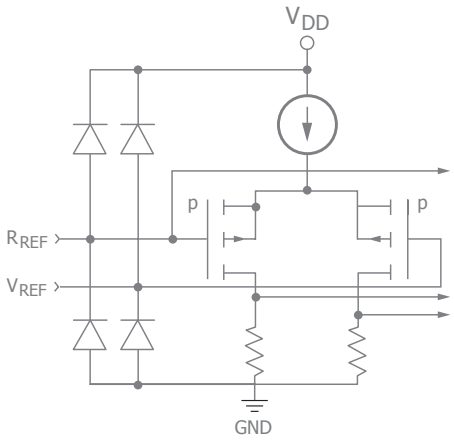


Figure 5. Equivalent Analog Input Circuit

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Typical Application Diagrams

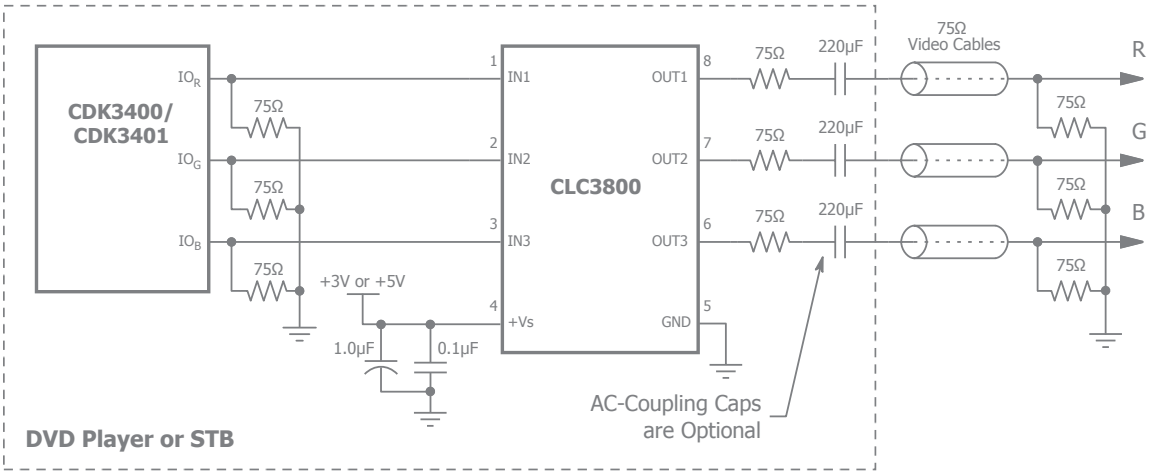


Figure 6. Standard Definition Video Output Circuit Diagram

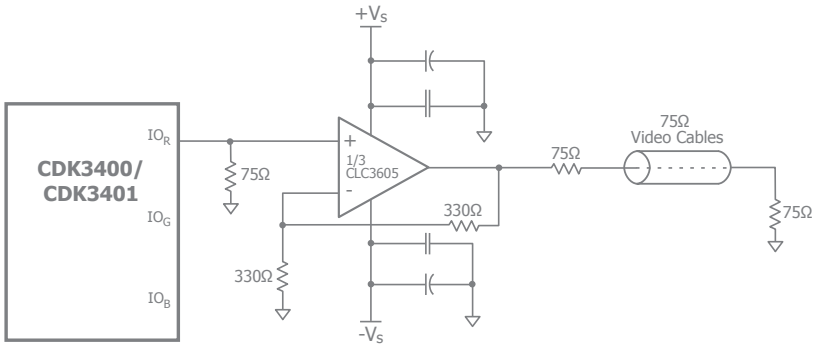


Figure 7. Graphics Output Driver Circuit Diagram

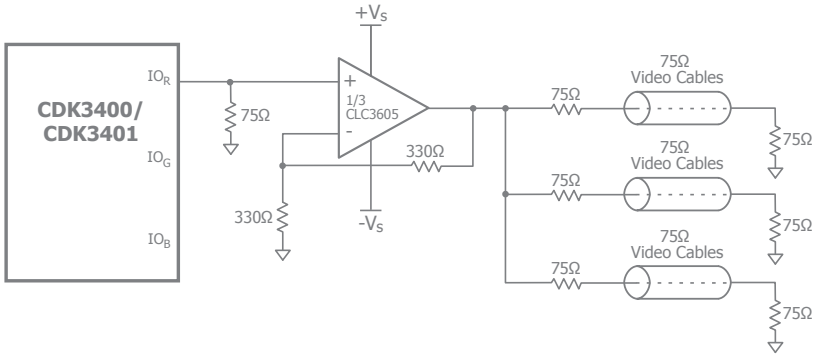


Figure 8. Standard Definition Video Distribution Circuit Diagram

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Applications Dicussion

Figure 9 below illustrates a typical CDK3400/3401 interface circuit. In this example, an optional 1.2V bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the CDK3400/3401 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The CDK3400/3401 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DD}) come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

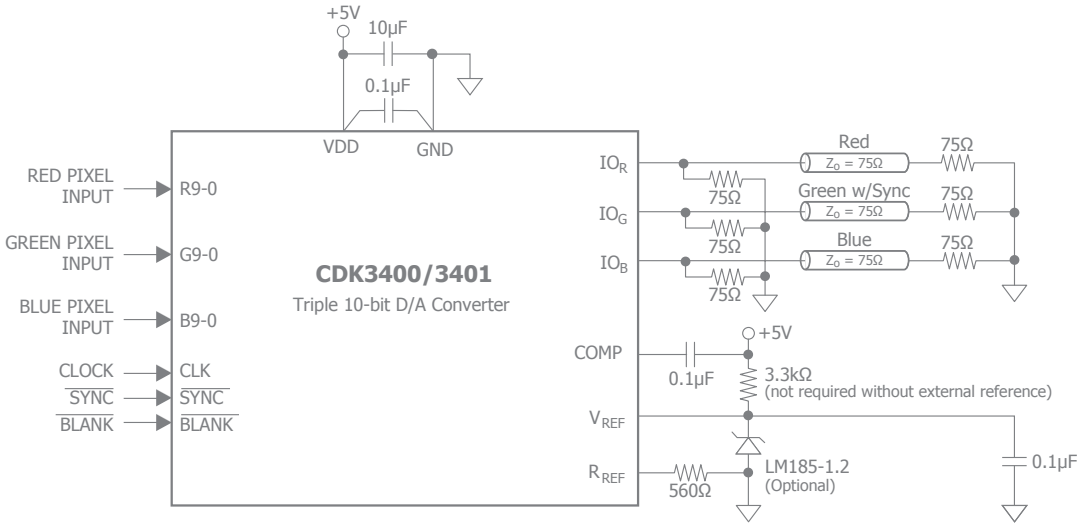


Figure 9. Typical Interface Circuit Diagram

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_S, IO_R, IO_G) as short as possible and as far as possible from all digital signals. The CDK3400/3401 should be located near the board edge, close to the analog out-put connectors.
2. Power plane for the CDK3400/3401 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the CDK3400/3401 is the same as that of the system's digital circuitry, power to the CDK3400/3401 should be decoupled with 0.1µF and 0.01µF capacitors and iso-lated with a ferrite bead.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.
4. If the digital power supply has a dedicated power plane layer, it should not be placed under the CDK3400/3401, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the CDK3400/3401 and its related analog circuitry can have an adverse effect on performance.
5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Evaluation boards are available (CEB3400 and CEB3401), contact CADEKA for more information.

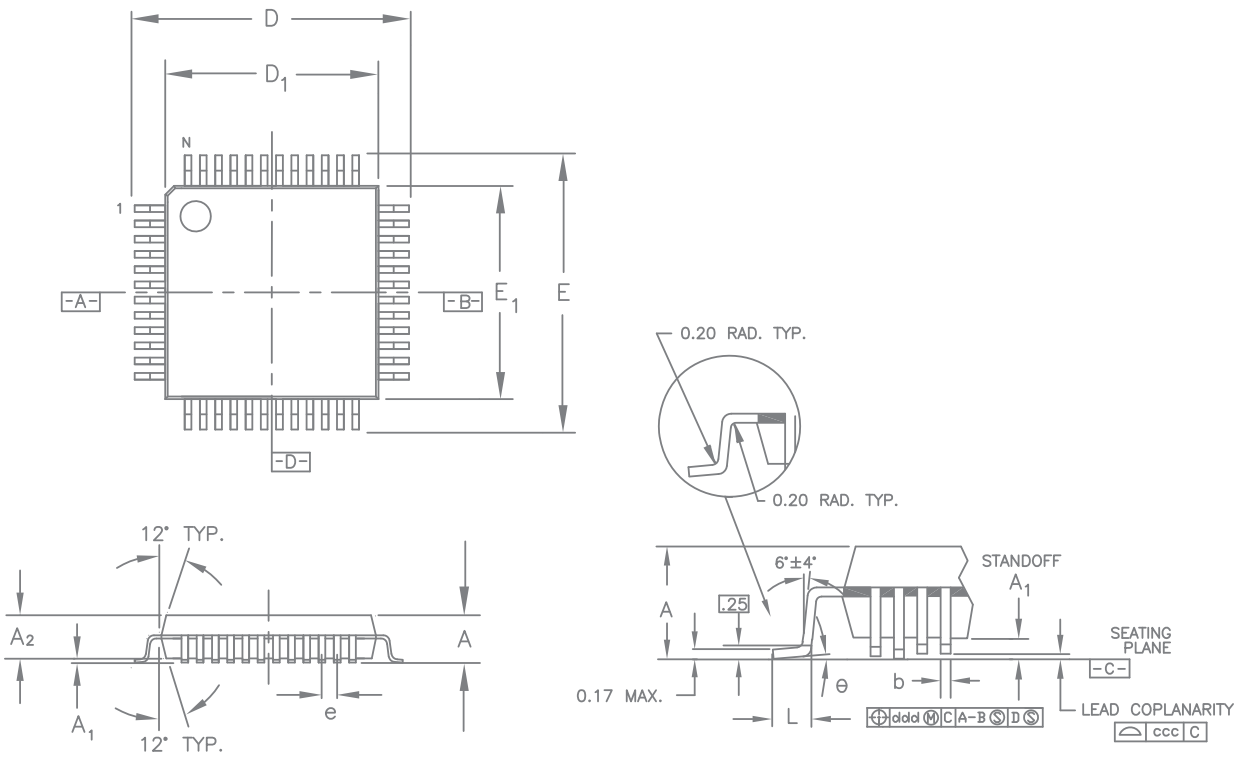
Related Products

- CDK3402/3403 Triple 8-bit 100/150MSPS DACs
- CDK3404 Triple 8-bit 180MSPS DAC

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Mechanical Dimensions

TQFP-48 Package



LEAD COUNT		48L	
DIMS.	TOL.		
A	MAX.	1.20	1.60
A_1		.05 MIN.	.15 MAX.
A_2	±.05	1.00	1.40
D	±.20	9.00	
D_1	±.10	7.00	
E	±.20	9.00	
E_1	±.10	7.00	
L	+.15/−.10	.60	
e	BASIC	.50	
ϕ	±.05	.22	
θ		0°−7°	
ddd	MAX.	.08	
ccc	MAX.	.08	
JEDEC REFERENCE DRAWING VARIATION DESIGNATOR		MS−026 ABC	MS−026 BBC

NOTES.

1. All dimensions in mm.
2. Dimension shown are nominal with tolerances indicated.
3. Foot length 'L' is measured at gage plane 0.25mm above seating plane.
4. L/F: Eftec 64T Cu or equivalent, 0.127mm (0.005") thick

For additional information regarding our products, please visit CADEKA at: cadeka.com

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