User's Guide
SCAU033–July 2009

Low Additive Phase Noise Clock Buffer Evaluation Board

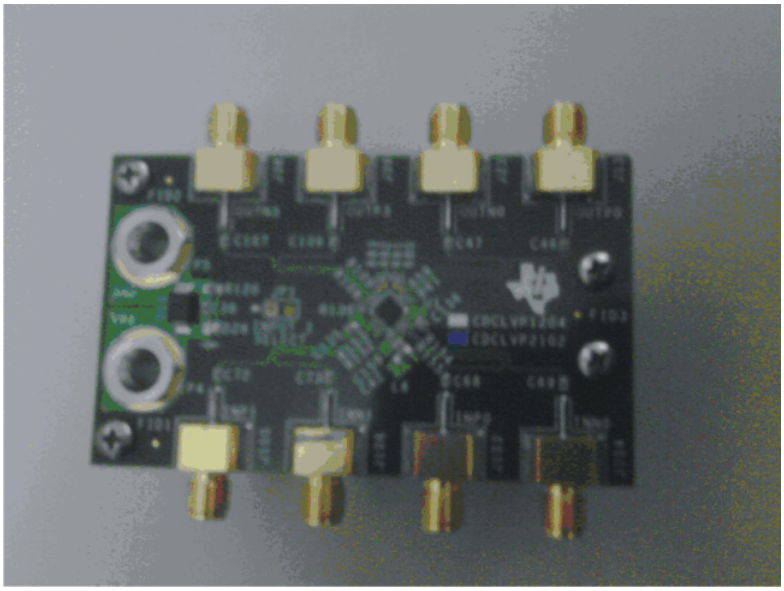


Figure 1. CDCLVP2102 Evaluation Board

Features:

- Easy-to-use evaluation board to fan out low phase noise clocks
- Easy device setup
- Fast configuration
- Control pins configurable through jumpers
- Board powered at +2.5-/+3.3-V
- Single-ended or differential input clocks
- CDCLVP2102 supports four LVPECL outputs; CDCLVP2102EVM supports two LVPECL outputs

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1 General Description

The CDCLVP2102 is a high-performance, low additive phase noise clock buffer. It has two universal input buffers that support either single-ended or differential clock inputs, and each input feeds a bank of two LVPECL outputs. The device also features on-chip bias generators that can provide the LVPECL common-mode voltage to the device inputs.

This evaluation module (EVM) is designed to demonstrate the electrical performance of the CDCLVP2102. This fully assembled and factory-tested evaluation board allows complete validation of the CDCLVP2102 device functionalities. Throughout this document, the acronym *EVM* and the phrases *evaluation module* and *evaluation board* are synonymous with the CDCLVP2102EVM. Figure 1 illustrates the CDCLVP2102EVM.

For optimum performance, the board is equipped with 50-Ω SMA connectors and well-controlled, 50-Ω impedance microstrip transmission lines.

2 Signal Path and Control Circuitry

The CDCLVP2102 supports single-ended inputs up to 200 MHz and differential inputs up to 2 GHz. The device provides up to four LVPECL outputs operating at the input frequency. For more information about the CDCLVP2102, see the CDCLVP2102 product data sheet available for download from the TI web site (www.ti.com).

3 Getting Started

The CDCLVP2102EVM has self-explanatory labeling and uses similar naming conventions as the CDCLVP2102 product data sheet. In this user's guide, all words in ***boldface and italic print*** reflect the actual labeling on the EVM. The CDCLVP2102EVM can be used with either single-ended or differential inputs.

3.1 Power-Supply Connections

Connect the power-supply source to the banana plug labeled ***VDD (P4)***, and connect the ground of the power-supply source to ***GND (P5)***. There are decoupling capacitors and a ferrite bead to isolate the EVM power from the CDCLVP2102 device power pins.

The CDCLVP2102EVM can use a supply voltage of 2.375 V to 3.6 V.

4 Input Clock Selection

The CDCLVP2102EVM offers users the option of receiving either a differential or single-ended clock as the clock input. The default option is for the differential signal at both device inputs. The inputs can be applied through the SMAs (J103, J104 or J105, J106). These inputs are ac-coupled to the device inputs. The common-mode voltage for these inputs after the ac-coupling capacitors are provided by 50 Ω (R152, R153 and R154, R155) to the device on-chip bias generator (V_{AC_REF}) pins. Either of the two input clocks can be selected using jumper JP1. When JP1 is shorted, IN0 is selected. When JP1 is open, IN1 is selected.

4.1 Configuring Single-ended Input

For a single-ended clock applied to IN0, remove capacitors C68 and C69 and replace them with 0-Ω resistors of the same footprint. The single-ended signal should be applied to INP0 (J103) and the dc bias voltage should be applied to INN0 (J104).

For a single-ended clock applied to IN1, remove capacitors C72 and C73 and replace them with 0-Ω resistors of the same footprint. The single-ended signal should be applied to INP1 (J105) and the dc bias voltage should be applied to INN1 (J106).

5 Output Clock

The CDCLVP2102 generates up to four LVPECL outputs. Two outputs are available on the CDCLVP2102EVM (outputs 0 and 3) through the following SMAs:

- J13, J23 for OUT0
- J39, J38 for OUT3

The LVPECL outputs are terminated with 150 Ω to ground and ac-coupled to the respective SMAs.

6 Schematics and Layout

Figure 2 and Figure 3 show the printed circuit board (PCB) schematics.

Note: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing CDCLVP2102EVM PCBs.

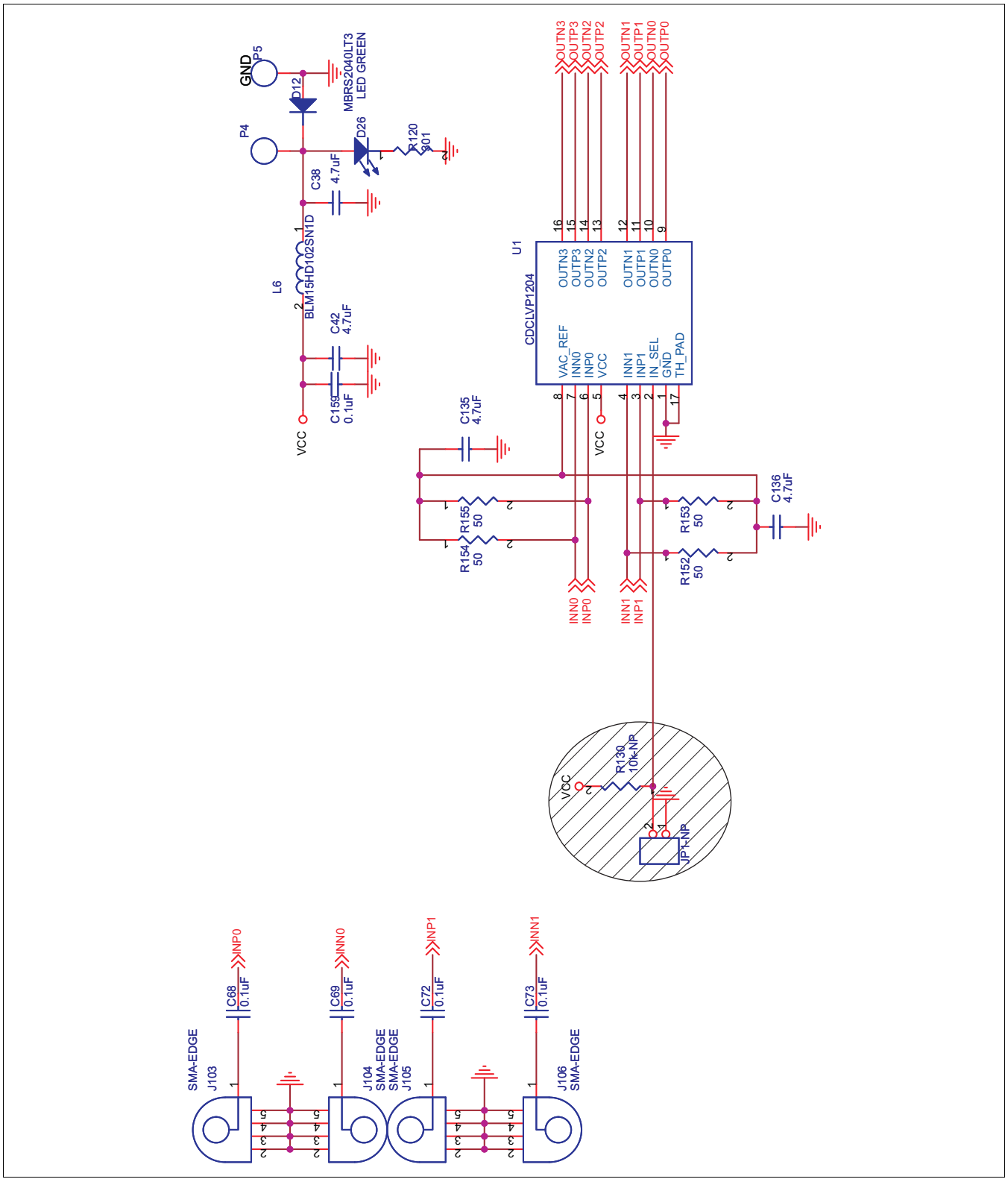


Figure 2. CDCLVP2102EVM—Schematic

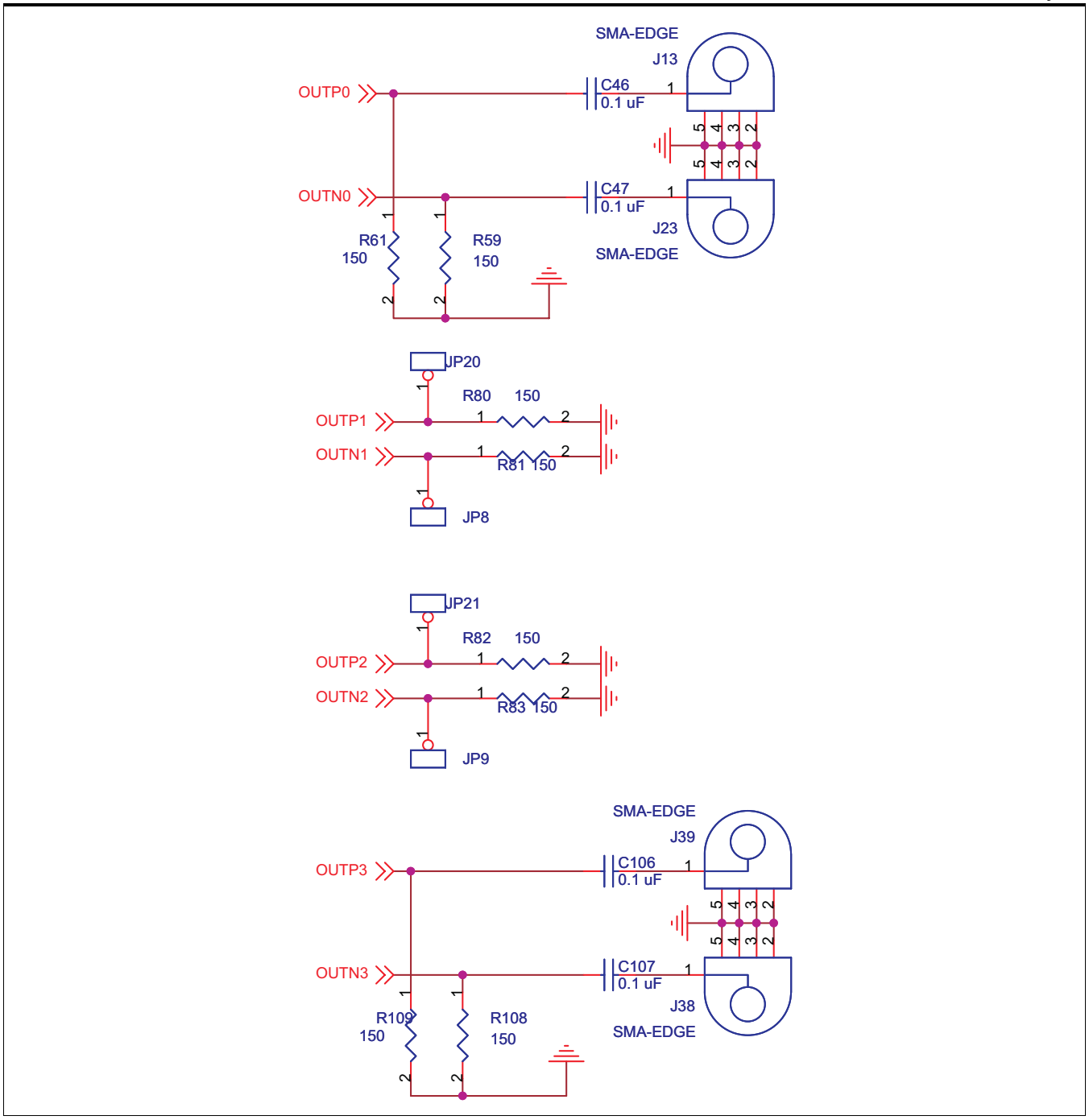


Figure 3. CDCLVP2102EVM—Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of –0.5 V to +4.0 V and the output voltage range of 0 V to +3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +120°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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