CDB53L21

Evaluation Board for CS53L21

Features

- Selectable Analog Inputs
  - Stereo Line-Level RCA Jacks
  - Stereo Microphone 1/8" Jacks
- Stereo Microphone Input Jacks
- 8- to 96-kHz S/PDIF Output
  - CS8406 Digital Audio Transmitter
- I/O Stake Headers
  - External Control Port Accessibility
  - External DSP Serial Audio I/O Accessibility
- Independent, Regulated Supplies
- 1.8 V to 3.3 V Logic Interface
- Hardware Control
  - 4 Pre-Defined Switch Settings
- FlexGUI S/W Control - Windows® Compatible
  - Pre-Defined & User-Configurable Scripts
- Layout and Grounding Recommendations

Description

The CDB53L21 evaluation board is an excellent means for evaluating the CS53L21 ADC. Evaluation requires an analog audio source, an analog/digital analyzer and power supplies. Optionally, a Windows PC-compatible computer may be used to evaluate the CS53L21 in Software Mode.

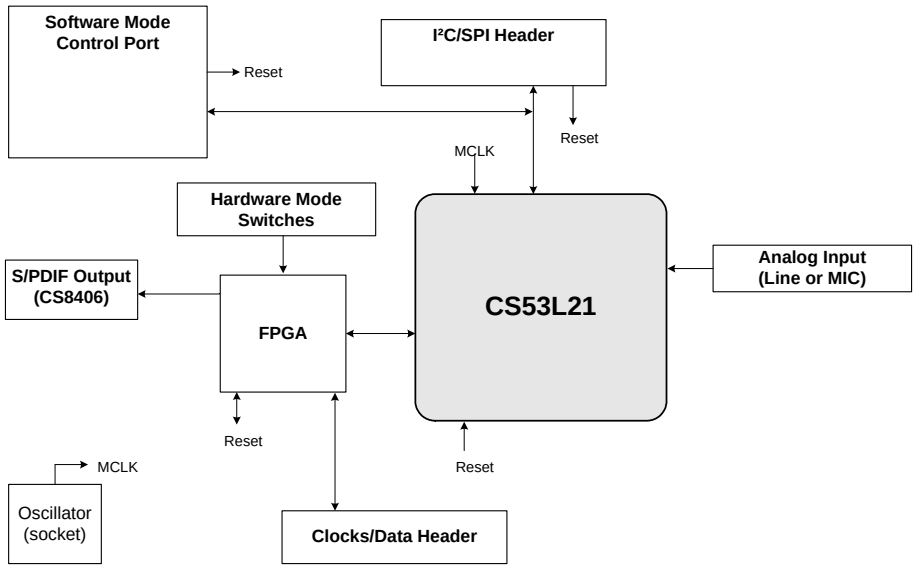
System timing can be provided by the CS53L21 with supplied master clock, or by using an I/O stake header with a DSP connected.

RCA phono jacks are provided for the CS53L21 analog inputs. 1/8" jacks are also available for microphone inputs. A digital data output is available from the CS8406 via RCA phono or optical connectors.

The Windows software provides a GUI to make configuration of the CDB53L21 easy. The software communicates through the PC's serial port or USB port to configure the control port registers so that all features of the CS53L21 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB53L21	Evaluation Board



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1. SYSTEM OVERVIEW

The CDB53L21 evaluation board is an excellent means for evaluating the CS53L21 ADC. Digital audio signal outputs are provided, and an FPGA is used for easily configuring the board. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 13 provide configuration details.

The CDB53L21 schematic set has been partitioned into seven pages and is shown in Figures 27 through 33. “System Connections and Jumpers” on page 20 provides a description of all stake headers and connectors, including the default factory settings for all jumpers.

1.1 Power

Power is supplied to the evaluation board through the +5.0 V binding posts. Jumpers connect the ADC’s supplies to a regulated voltage of +1.8 V, 2.5 V or +3.3 V for VL and +1.8 V or 2.5 V for VD and VA. All voltage inputs must be referenced to the black binding post ground connector.

For current measurement purposes only, a series resistor is connected to each supply. The current is easily calculated by measuring the voltage drop across this resistor. **NOTE:** The stake headers connected in parallel with these resistors must be shunted with the supplied jumper during normal operation.

WARNING: Please refer to the CS53L21 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS53L21 requires careful attention to power supply and grounding arrangements to optimize performance. The CDB53L21 demonstrates these optimal arrangements. Figure 26 on page 22 provides an overview of the connections to the CS53L21. Figure 34 on page 30 shows the component placement, Figure 35 on page 31 shows the top layout, and Figure 36 on page 32 shows the bottom layout. The decoupling capacitors are located as close to the CS53L21 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 FPGA

The FPGA provides digital signal routing between the CS53L21, CS8406 and the I/O stake header. It also configures the Hardware Mode options of the CS8406 and provides routing control of the system master clock from an on-board oscillator and the I/O stake header. The Cirrus FlexGUI software and “FPGA H/W Control” switches provide full control of the FPGA’s routing and configuration options. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 13 provide configuration details.

1.4 CS53L21 Audio A to D Converter

A complete description of the CS53L21 (Figure 27 on page 23) is included in the CS53L21 product data sheet.

The CS53L21 may be configured using either the Cirrus FlexGUI or the on-board “CS53L21 H/W Control” switches. The Software Mode control port registers are accessible through the “Register Maps” tab of the Cirrus FlexGUI software. This tab provides low-level control of each bit. For easier configuration, additional tabs provide high-level control. The Hardware Mode, stand-alone controls for the CS53L21 are accessible through the on-board, stand-alone switches, “CS53L21 H/W Control.”

Clock and data source selections are made in the control port of the FPGA, accessible through the “General Configurations” tab of the Cirrus FlexGUI software or through the on-board “FPGA H/W Control” switches. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 13 provide configuration details.

1.5 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter (Figure 29 on page 25) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS53L21 to the standard S/PDIF data stream and routes this signal to the optical and RCA connectors. The CS8406 operates in slave mode only, accepting either a 128xFs or 256xFs master clock, and can operate in either the Left-Justified or I²S interface format.

Selections are made in the control port of the FPGA, accessible through the "General Configurations" tab of the Cirrus FlexGUI software or through the on-board switches, "FPGA H/W Control." Section 2. "Software Mode Control" on page 7 and Section 3. "Hardware Mode Control" on page 13 provide configuration details.

1.6 Oscillator

The on-board oscillator provides one of the system master clocks. Selections are made in the control port of the FPGA, accessible through the "General Configurations" tab of the Cirrus FlexGUI software or through the on-board switches, "FPGA H/W Control." Section 2. "Software Mode Control" on page 7 and Section 3. "Hardware Mode Control" on page 13 provide configuration details.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. Additional sockets are also installed, allowing the optional use of a full- or half-can-sized oscillator.

1.7 I/O Stake Headers

The evaluation board has been designed to allow interfacing with external systems via a serial port header (reference designation J5) and a control port header, "CS53L21 S/W Control." The serial port header provides access to the serial audio signals required to interface with a DSP (Figure 31 on page 27). Selections are made in the control port of the FPGA, accessible through the "General Configurations" tab of the Cirrus FlexGUI software or through the on-board switches, "FPGA H/W Control." Section 2. "Software Mode Control" on page 7 and Section 3. "Hardware Mode Control" on page 13 provide configuration details.

The control port header provides bidirectional access to the SPI™/I²C® control port signals by simply removing all the shunt jumpers from the "PC" position. The user may then choose to connect a ribbon cable to the "CONTROL" position, allowing operation of the CS53L21 in a user-application for system development. A single "GND" row for the ribbon cable's ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I²C power rail.

1.8 Analog Input

RCA connectors supply the line-level analog inputs through an AC-coupled passive filter. The signal from these inputs may be driven to individual inputs or to all inputs of the CS53L21. A microphone may be connected to one or both of the 1/8" jacks, MIC1 and MIC2.

To accommodate the microphone bias output available on certain input pins of the CS53L21, additional stake headers are provided to MUX both the input audio signal and the output bias signal to or from the CS53L21. Figure 28 on page 24 in the schematic set illustrates how signals are routed. Table 4 on page 21 provides more details for how to connect the jumpers. The CS53L21 data sheet details the required single-ended signal amplitude that will drive the inputs to full scale.

1.9 Stand-Alone Switches

The “FPGA H/W Control” and “CS53L21 H/W Control” switches control all Hardware Mode options. Section 3. “Hardware Mode Control” on page 13 provides a description of each topology.

1.10 Control Port Connectors

A graphical user interface is available for the CDB53L21, allowing easy manipulation of each register. This GUI interfaces with the CDB via the RS-232 or USB connectors and controls all Software Mode options. Section 2. “Software Mode Control” on page 7 provides a description of the Graphical User Interface (GUI).

1.10.1 RS-232 and USB Connectors

Connecting a cable to the RS-232 connector or the USB 1.0/2.0 connector and launching the Cirrus FlexGUI software enables the CDB53L21 in Software Mode.

2. SOFTWARE MODE CONTROL

The CDB53L21 may be used with the Microsoft Windows-based FlexGUI graphical user interface, allowing software control of the CS53L21 and FPGA registers. The latest control software may be downloaded from **www.cirrus.com/msasoftware**. Step-by-step instructions for setting up the FlexGUI are provided as follows:

1. Download and install the FlexGUI software as instructed on the Website.
2. Connect and apply power to the +5.0 V binding post.
3. Connect the CDB to the host PC using either a 9-pin serial or USB cable.
4. Launch the Cirrus FlexGUI. *Once the GUI is launched successfully, all registers are set to their default reset state.*
5. Enable the CS53L21 by engaging the “Enable CS53L21” push button.
6. Refresh the GUI by clicking on the “Update” button. *The default state of all registers are now visible.*
7. Engage and then disengage the “Power Down” push button in the “ADC Basic Configurations” group. *This performs the necessary write sequence to the* CS53L21 *for Software Mode operation.*

For standard setup:

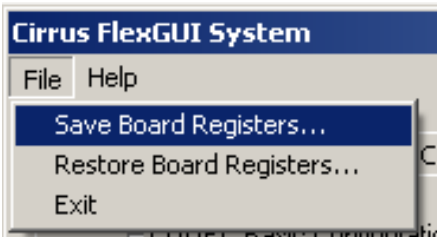
8. Set up the signal routing in the “General Configurations” tab as desired.
9. Set up the CS53L21 in the “ADC Configuration”, “ADC Volume Controls” or “Mix Volume Controls” tab as desired.
10. Begin evaluating the CS53L21.

For quick setup, the CDB53L21 may, alternatively, be configured by loading a predefined sample script file:



11. On the File menu, click "Restore Board Registers..."
12. Browse to Boards\CDB53L21\Scripts\.
13. Choose any one of the provided scripts to begin evaluation.

To create personal scripts files:



14. On the File menu, click "Save Board Registers..."
15. Enter any name that sufficiently describes the created setup.
16. Choose the desired location and save the script.
17. To load this script, follow the instructions from step 11 above.

2.1 General Configuration Tab

The “General Configuration” tab provides high-level control of signal routing on the CDB53L21. This tab also includes basic controls for the CS53L21 for quickly setting up the CDB53L21 in simple configurations. Status text detailing the ADC’s specific configuration is shown in parenthesis or appears directly below the associated control. This text may change depending on the setting of the associated control. A description of each control group is outlined below:

ADC Basic Configuration - Includes basic register controls in the CS53L21 used for setting up the interface format, clocking functions and internal analog input routing. See Section 2.2 through Section 2.4 for more CS53L21 controls.

S/PDIF Transmitter Control - Includes all available Hardware Mode controls for setting up the CS8406.

Clock/Data Routing and ADC Reset - Includes controls used for routing clocks and data between the CS53L21, oscillator and the I/O stake header. Also included is a reset control for the CS53L21.

Update - Reads all registers in the FPGA and CS53L21 and reflects the current values in the GUI.

Reset - Resets FPGA to default routing configuration.

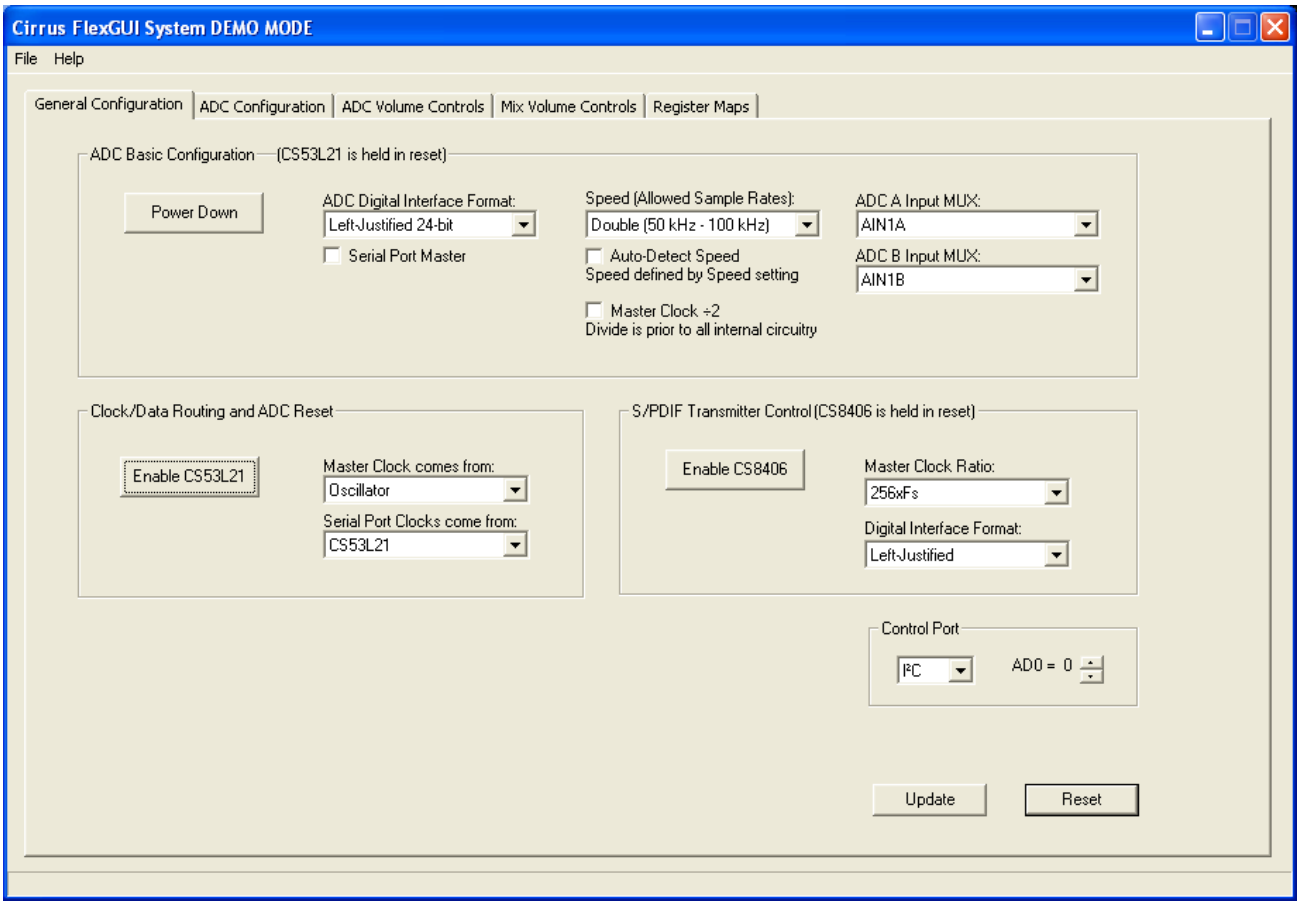


Figure 1. General Configuration Tab

2.2 ADC Configuration Tab

The “ADC Configuration” tab provides high-level control of all setup configurations for the CS53L21. Status text detailing the ADC’s specific configuration is shown in parenthesis or appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each control group is outlined below (a description of each register is included in the CS53L21 data sheet):

Power Control - Includes all register controls for powering down specific circuits within the CS53L21.

ADC input Configuration - Includes controls for the internal MUX, analog input, microphone bias output and channel mix.

Serial Port Configuration - Includes controls for all settings related to the transmission and relationship of data and clocks within the CS53L21.

Update - Reads all registers in the CS53L21 and reflects the current values in the GUI.

Reset - Resets the CS53L21.

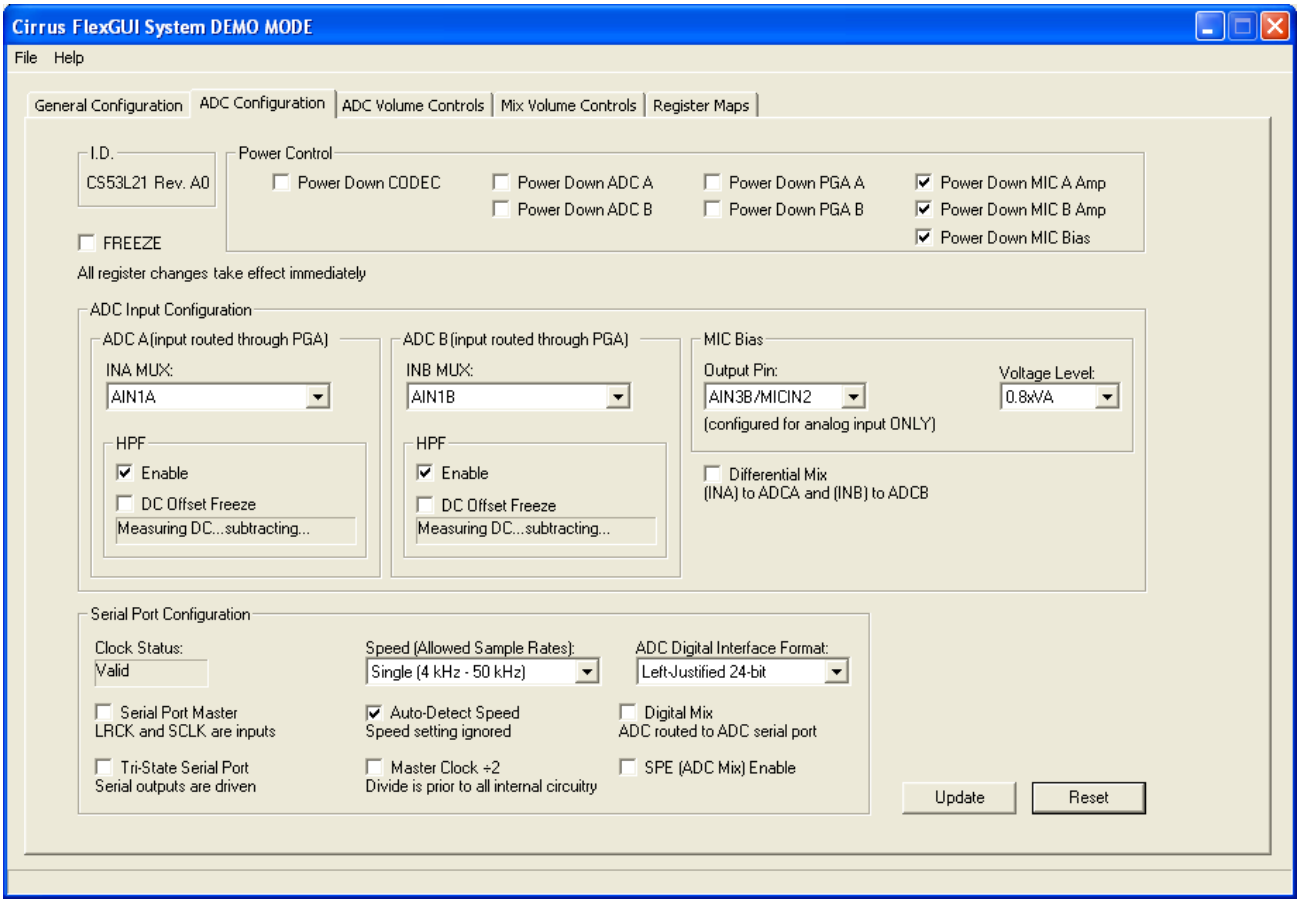


Figure 2. ADC Configuration Tab

2.3 ADC Volume Controls Tab

The “ADC Volume Controls” tab provides high-level control of all volume settings in the ADC of the CS53L21. Status text detailing the ADC’s specific configuration is shown in parenthesis or inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each control group is outlined below (a description of each register is included in the CS53L21 data sheet):

Digital Volume Control - Includes digital volume controls and adjustments for the ADC.

ALC Configuration - Includes all configuration settings for the Automatic Level Control (ALC).

Analog Volume Control - Includes all analog volume controls and adjustments for the ADC.

Noise Gate Configuration - Includes all configuration settings for the noise gate.

Update - Reads all registers in the CS53L21 and reflects the current values in the GUI.

Reset - Resets the CS53L21.

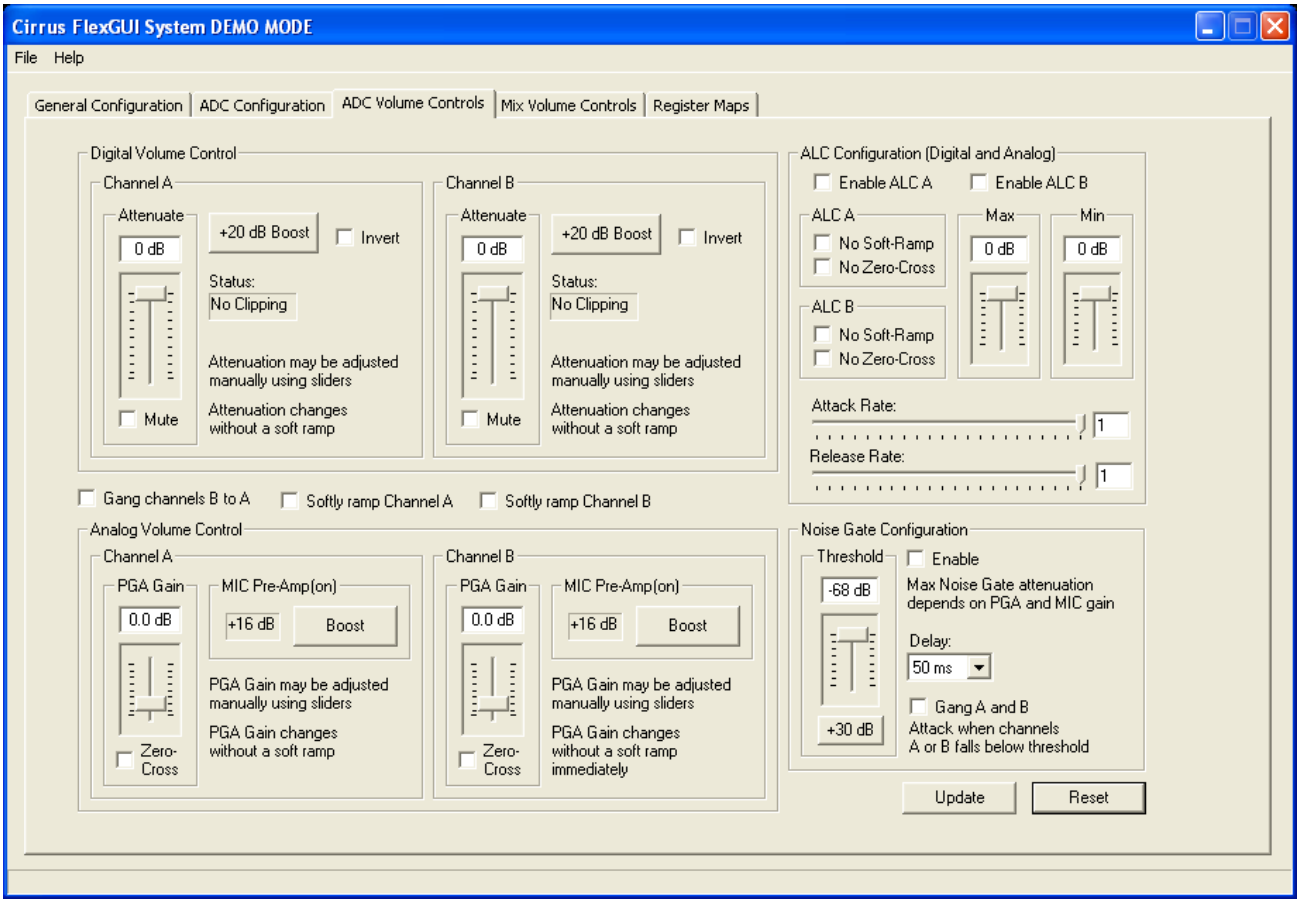


Figure 3. ADC Volume Controls Tab

2.4 Mix Volume Controls Tab

The “Mix Volume Controls” tab provides high-level control of the ADC channel mix functions. Status text detailing the ADC’s specific configuration is shown in read-only edit boxes or appears directly below the associated control. This text will change, depending on the setting of the associated control. A description of each control group is outlined below (a description of each register is included in the CS53L21 data sheet):

Digital Volume Control - ADC channel mix volume controls and adjustments.

Update - Reads all registers in the CS53L21 and reflects the current values in the GUI.

Reset - Resets the CS53L21.

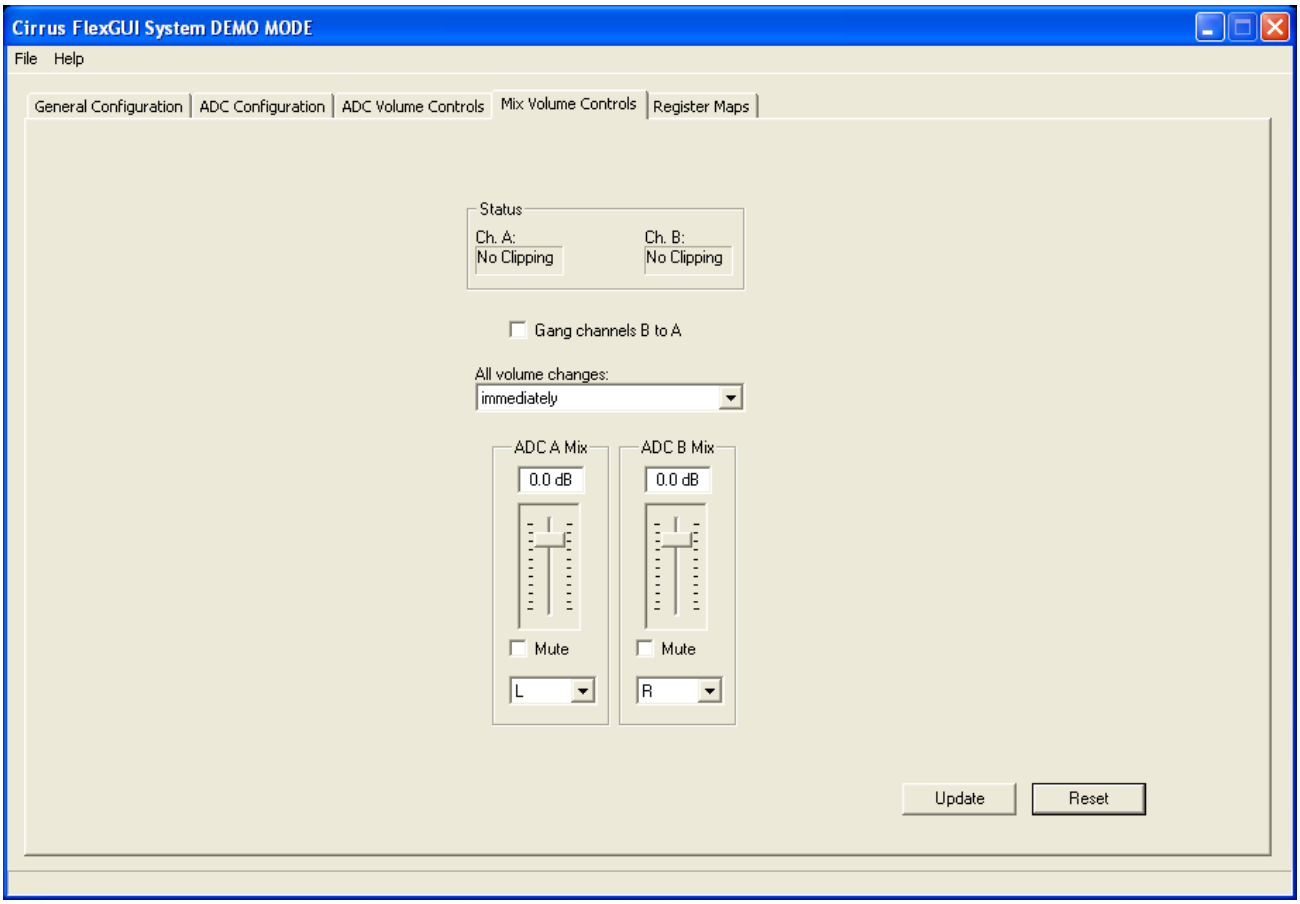


Figure 4. Mix Volume Controls Tab

2.5 Register Maps Tab

The Advanced Register Debug tab provides low-level control of the CS53L21 individual register settings. Register values can be modified bit-wise or byte-wise. For bit-wise, click the appropriate push-button for the desired bit. For byte-wise, the desired hex value can be typed directly into the register address box in the register map. The “FPGA” and “GPIO” tabs may be ignored.

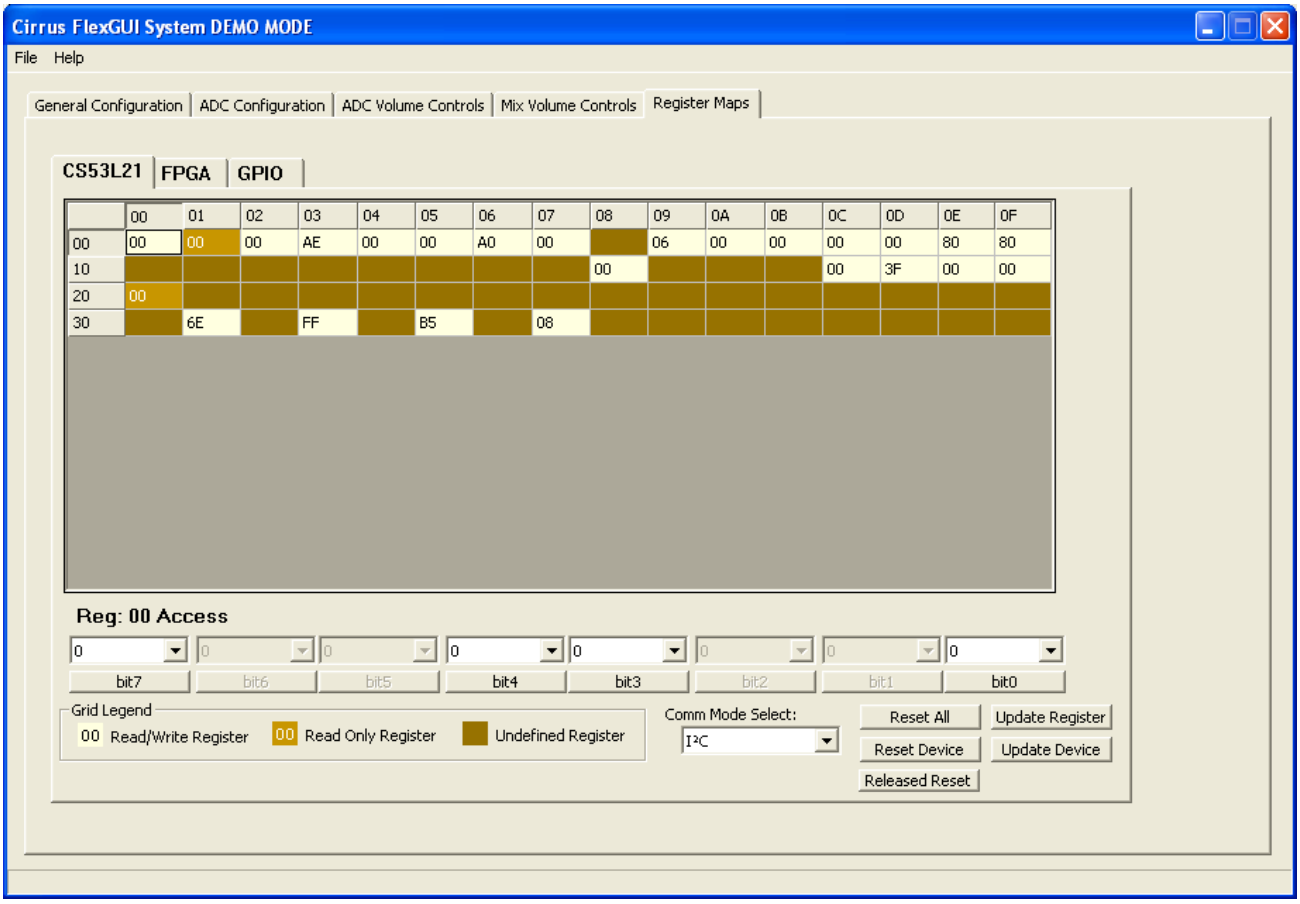


Figure 5. Register Maps Tab - CS53L21

3. HARDWARE MODE CONTROL

The CDB may be configured without the use of a software control port through the use of two switches, “FPGA H/W Control” and “CS53L21 H/W Control.” These switches are enabled in Hardware Mode only and ignored in Software Mode. The CDB53L21 automatically enters Hardware Mode upon initial power up, or when exiting Software Mode, by terminating the Cirrus FlexGUI software or by disconnecting the RS-232 serial cable or USB cable.

3.1 FPGA H/W Control

The “FPGA H/W Control” switch S3 sets up the CDB in 4 pre-defined routing topologies in Hardware Mode. The tables and figures below describe each switch setting. The At-A-Glance Controls table provides a quick reference for all presets.

At-A-Glance Controls		
S[3:2]	**S[1] (See Note 1.)**	**S[0]**
00 - Reserved **01** - I/O Header MCLK / I/O Header clocks/data route through FPGA **10** - Oscillator MCLK / I/O Header clocks/data route through FPGA **11** - Reserved	**0** - CS53L21 Slave Routing **1** - CS53L21 Master Routing	**0** - No Loopback Routing **1** - Reserved

Signal Routing	S[3:0]	General Description	Detailed Description
0	0000	Reserved	
1	0001	Reserved	
2	0010	Reserved	
3	0011	Reserved	
I/O MCLK			
4 Figure 6	0100	I/O Clocks/Data	1) I/O masters MCLK. 2) I/O masters PCM clocks. 3) SDOUT to CS8406 and I/O Header
5	0101	Reserved	
6 Figure 7	0110	CS53L21 Clocks, I/O Data	1) I/O masters MCLK. 2) CS53L21 masters PCM clocks. 3) SDOUT to CS8406 and I/O Header
7	0111	Reserved	
Oscillator MCLK			
8 Figure 8	1000	I/O Clocks/Data	1) Oscillator masters MCLK. 2) I/O masters PCM clocks. 3) SDOUT to CS8406 and I/O Header
9	1001	Reserved	
10 Figure 9	1010	CS53L21 Clocks, I/O Data	1) Oscillator masters MCLK. 2) CS53L21 masters PCM clocks. 3) SDOUT to CS8406 and I/O Header
11	1011	Reserved	
12-15 Reserved			

Table 1. MCLK and Clock/Data Routing Options

Notes:

1. The S[1] setting affects FPGA signal routing only and is independent of the M/$\overline{S}$ setting of the “CS53L21 H/W Control” switch S5. These settings must be made manually by the user and have to be consistent.

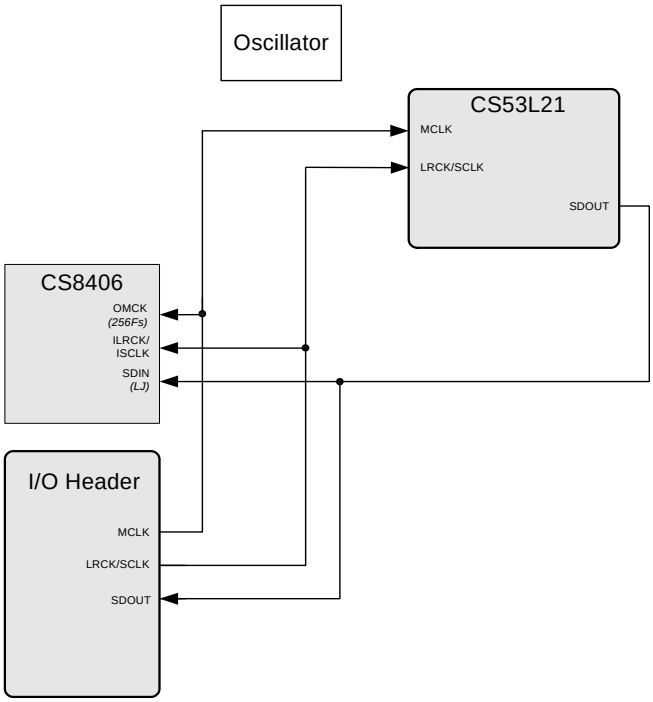


Figure 6. Routing 4

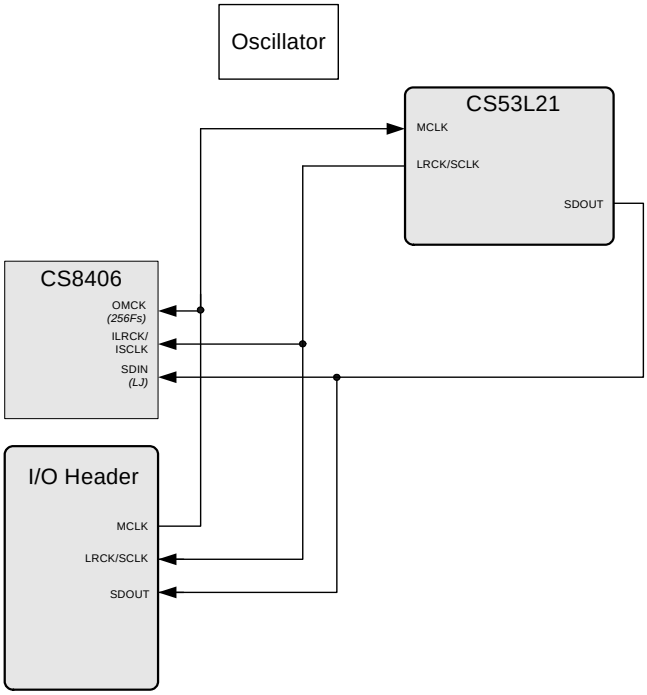


Figure 7. Routing 6

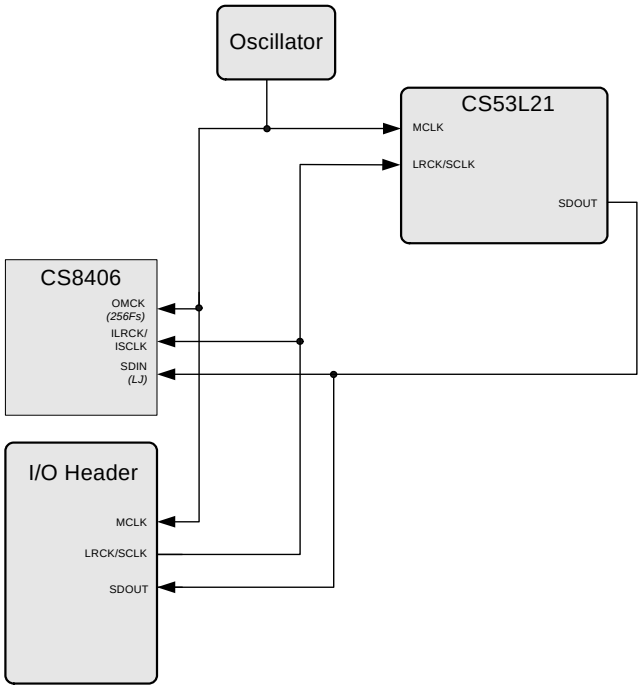


Figure 8. Routing 8

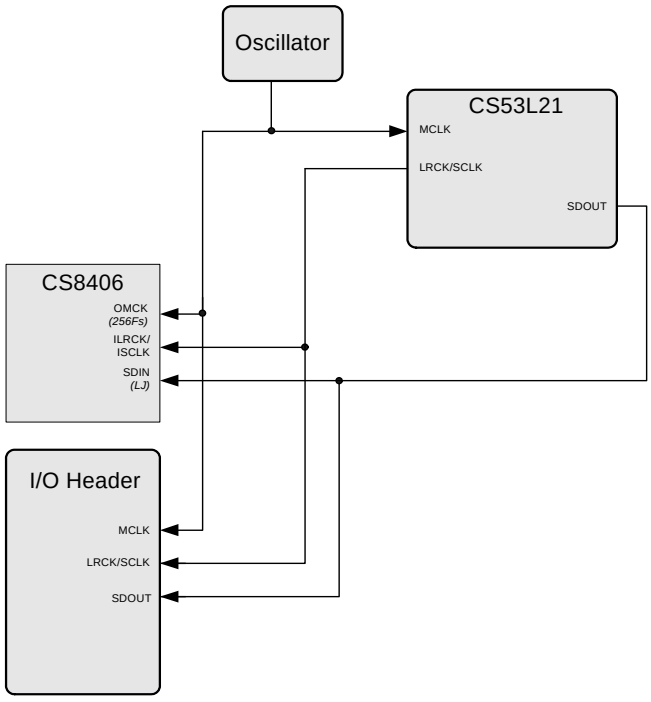


Figure 9. Routing 10

3.2 CS53L21 H/W Control

The stand-alone “CS53L21 H/W Control” switch S5 controls the Hardware Mode options of the CS53L21. A description of each switch is outlined in the following table. See the CS53L21 Data Sheet, Section 4.2 “Hardware M

ode” for further details on setting these switches.

Switch	Position	Function
M/$\overline{S}$ (Note 1.)	LO	LRCK and SCLK are inputs to CS53L21.
	HI	LRCK and SCLK are outputs to CS53L21.
MCLKDIV2	LO	Internal MCLK to CS53L21 not divided.
	HI	Internal MCLK to CS53L21 divided by 2.
I2S/$\overline{LJ}$ (Note 2.)	LO	CS53L21 Interface Format: Left-Justified.
	HI	CS53L21 Interface Format: I²S.

Table 2. CS53L21 H/W Mode Control

Notes: 1. The M/$\overline{S}$ setting affects the CS53L21 only and is independent of S[1] setting in the “FPGA H/W Control” switch S3. These settings must be made manually by the user and have to be consistent.

2. The I2S/$\overline{LJ}$ setting affects the CS53L21 only. The S/PDIF Transmitter input data format in HW Mode is always $\overline{LJ}$ and is independent of this setting. If the user desires I2S format PCM SDOUT data, the I/O Header will have to be used.

4. PERFORMANCE PLOTS

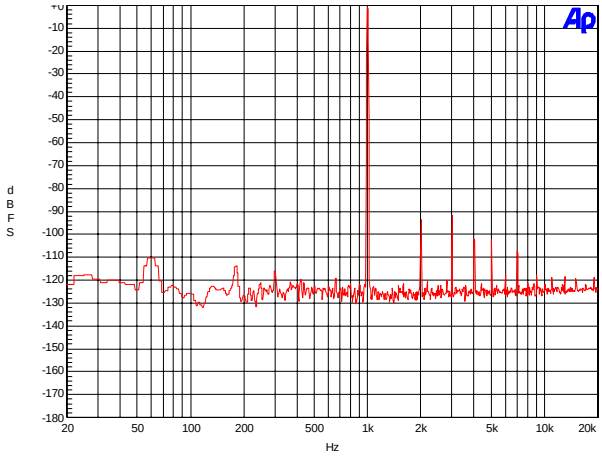


Figure 10. 0 dB FFT, Single-Speed Mode

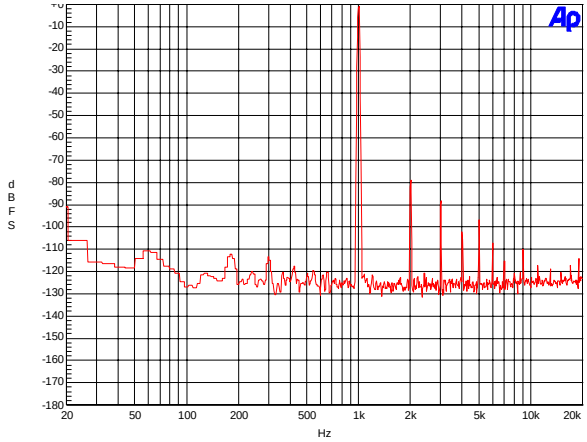


Figure 11. 0 dB FFT, Double-Speed Mode

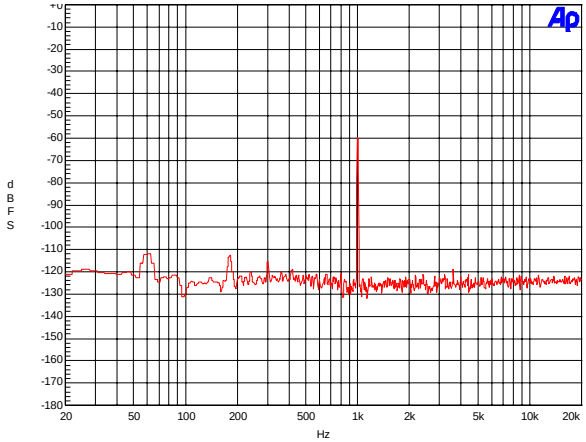


Figure 12. -60 dB FFT, Single-Speed Mode

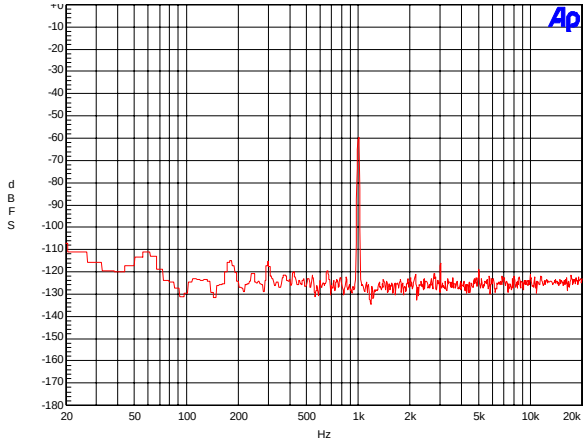


Figure 13. -60 dB FFT, Double-Speed Mode

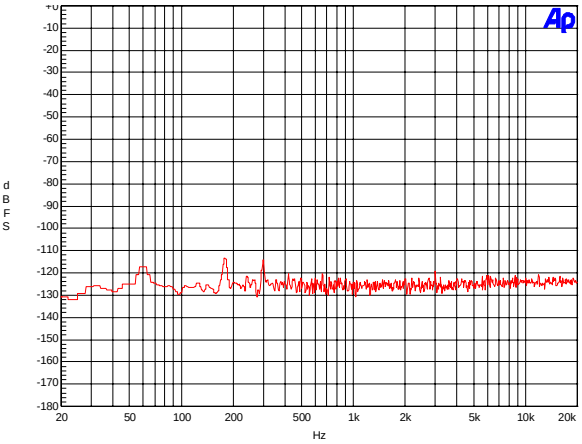


Figure 14. No Input FFT, Single-Speed Mode

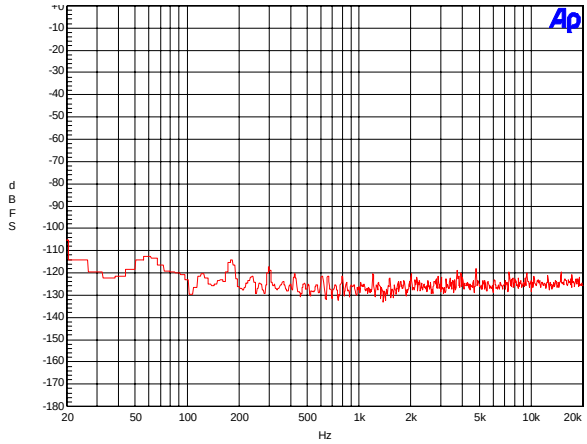


Figure 15. No Input FFT, Double-Speed Mode

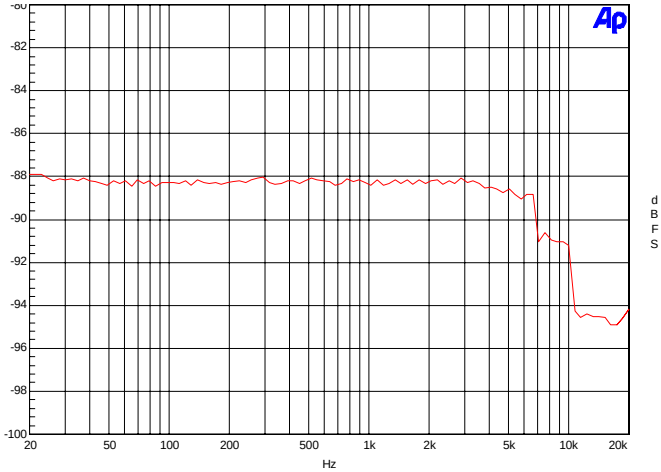


Figure 16. THD+N vs. Frequency, Single-Speed Mode

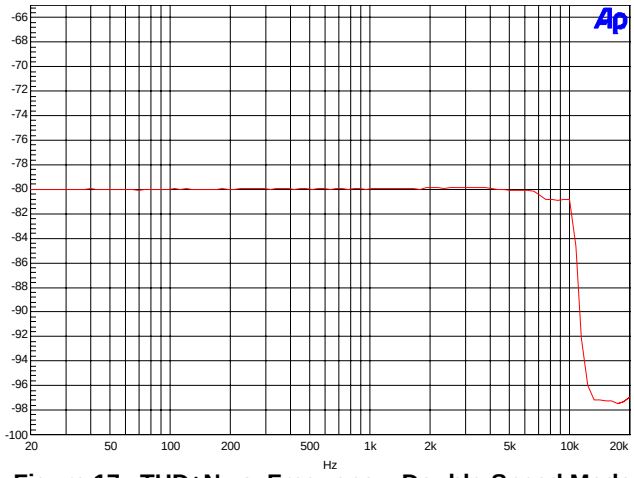


Figure 17. THD+N vs. Frequency, Double-Speed Mode

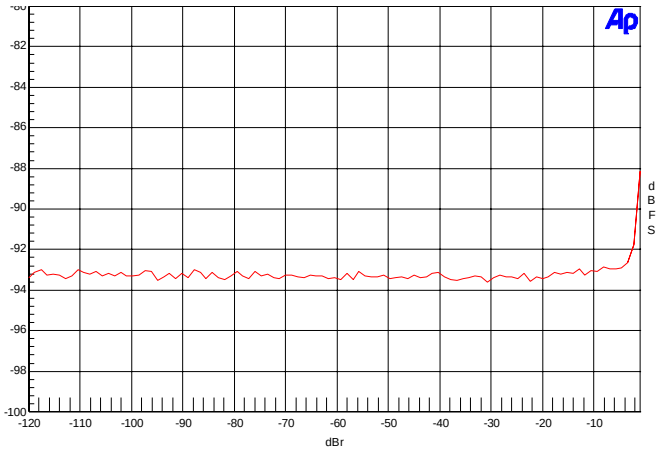


Figure 18. THD+N vs. Amplitude, Single-Speed Mode

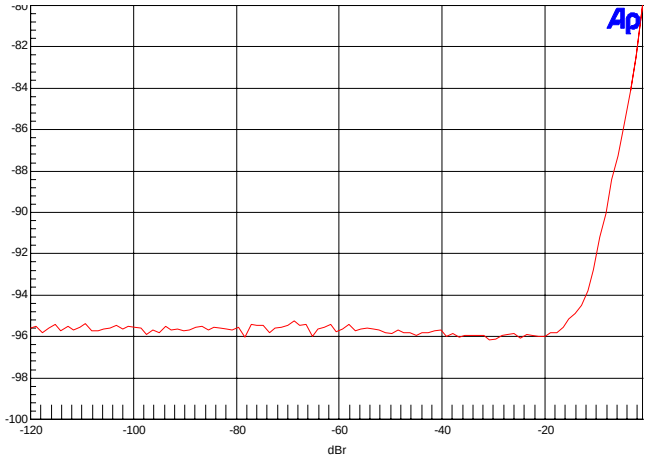


Figure 19. THD+N vs. Amplitude, Double-Speed Mode

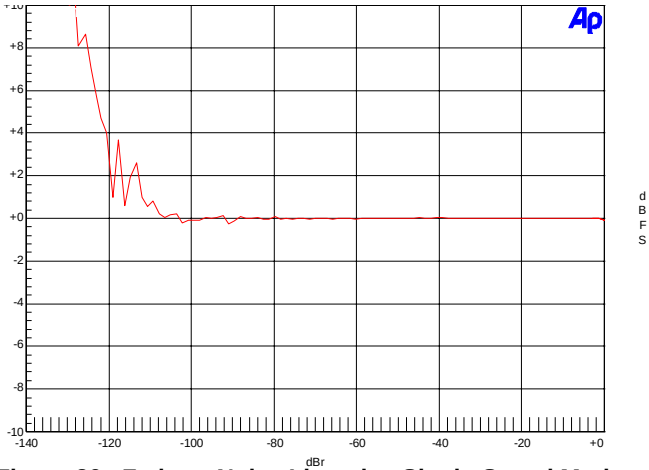


Figure 20. Fade-to-Noise Linearity, Single-Speed Mode

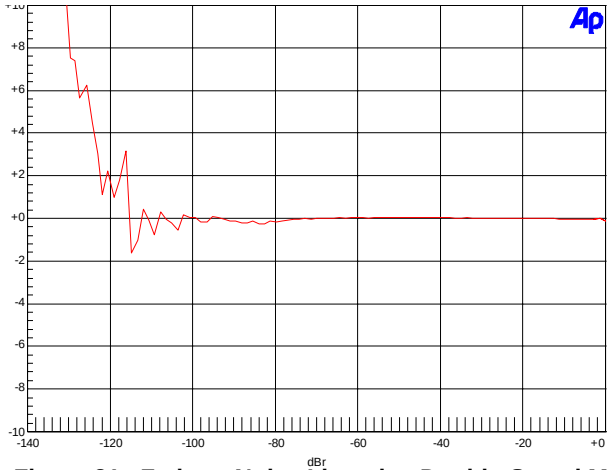


Figure 21. Fade-to-Noise Linearity, Double-Speed Mode

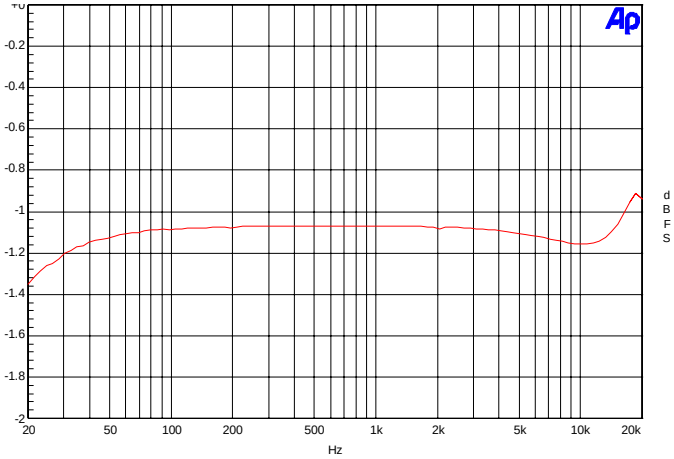


Figure 22. Frequency Response, Single-Speed Mode

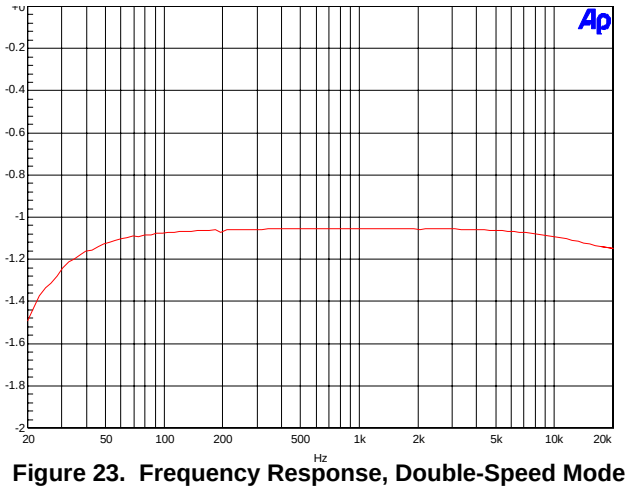


Figure 23. Frequency Response, Double-Speed Mode

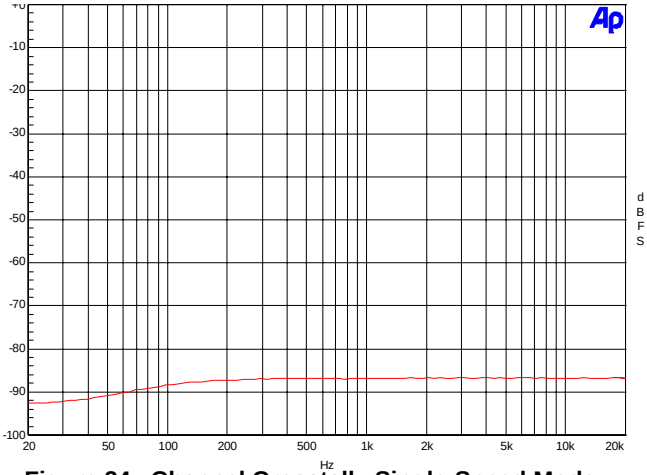


Figure 24. Channel Crosstalk, Single-Speed Mode

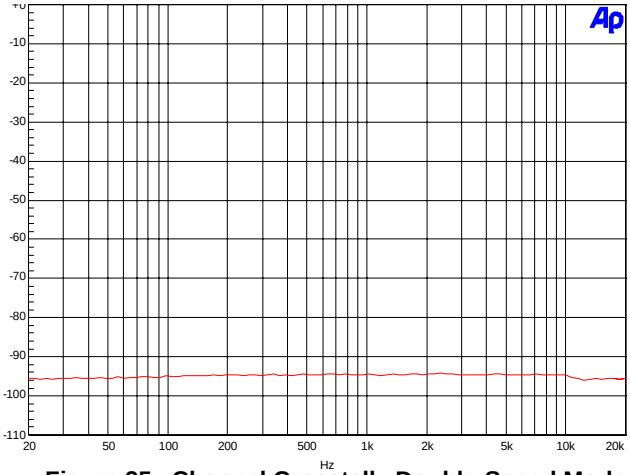


Figure 25. Channel Crosstalk, Double-Speed Mode

5. SYSTEM CONNECTIONS AND JUMPERS

CONNECTOR	REF	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J26	Input	+5.0 V Power Supply.
GND	J27	Input	Ground Reference .
RS232	J95	Input/Output	Serial connection to PC for SPI / I²C control port signals.
USB	J94	Input/Output	USB connection to PC for SPI / I²C control port signal.
S/PDIF OPTICAL OUT	OPT2	Output	CS8406 digital audio output via optical cable.
S/PDIF COAX OUT	J68	Output	CS8406 digital audio output via coaxial cable.
I/O Header	J5	Input/Output	I/O for Clocks & Data.
S/W CONTROL	J109	Input/Output	I/O for external SPI / I²C control port signals.
MICRO JTAG	J110	Input/Output	I/O for programming the micro controller (U84).
FPGA JTAG	J78	Input/Output	I/O for programming the FPGA (U14).
MICRO RESET	S4	Input	Reset for the micro controller (U84).
FPGA PROGRAM	S2	Input	Reload Xilinx Flash program into the FPGA (U14).
H/W BOARD RESET	S1	Input	Reset for the CS53L21 (U1).
LINEB LINEA	J62 J7	Input	RCA phono jacks for analog input signal to CS53L21.
MIC1 MIC2	J35 J51	Input	Microphone jacks for analog input signal to CS53L21.

Table 3. System Connections

JMP	LABEL	PURPOSE	POSITION	FUNCTION SELECTED
J31	VL	Selects source of voltage for the VL supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator.
			+3.3V	Voltage source is +3.3 V regulator.
J25	VA	Selects source of voltage for the VA supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator. .
J28	VD	Selects source of voltage for the VD supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator. .
J52 J47 J53	VL VA VD	Current Measurement	*SHUNTED	1 Ω series resistor is shorted.
			OPEN	1 Ω series resistor in power supply path.
J2	LINEB MUX	Selects signal source for the ADC I/O	(AIN3B Select)	LINEB signal routed to jumper J8.
			(AIN2B Select)	LINEB signal routed to jumper J3.
			*AIN1B	LINEB signal routed to AIN1B of ADC.
J1	LINEA MUX	Selects signal source for the ADC I/O	(AIN3A Select)	LINEA signal routed to jumper J14.
			AIN2A	LINEA signal routed to AIN2A of ADC.
			*AIN1A	LINEA signal routed to AIN1A of ADC.
J3	(AIN2B Select)	Selects signal source for MIC1 and MIC2 bias or signal source for the ADC input	BIAS1 to MIC2	Bias on AIN2B of ADC routed to jumper J12.
			BIAS1 to MIC1	Bias on AIN2B of ADC routed to MIC1.
			*LINEB	LINEB MUX routed to AIN2B of ADC.
J8	(AIN3B Select)	Selects signal source for MIC2 bias or signal source for the ADC input	BIAS2 to MIC2	Bias on AIN3B of ADC routed to jumper J12.
			MIC2	MIC2 signal routed to AIN3B of ADC.
			*LINEB	LINEB MUX routed to AIN3B of ADC.
J14	(AIN3A Select)	Selects signal source for the ADC input	MIC2	MIC2 signal routed to AIN3A of ADC.
			MIC1	MIC1 signal routed to AIN3A of ADC.
			*LINEA	LINEA MUX routed to AIN3A of ADC.
J12	MIC2 Bias	Selects bias for MIC2	BIAS1	J3 (for Bias on AIN2B of ADC) routed to MIC2.
			BIAS2	J8 (for Bias on AIN3B of ADC) routed to MIC2.
			*Not connected	Jumper placed on pin 2.

*Default factory settings

Table 4. Jumper Settings

6. BLOCK DIAGRAM

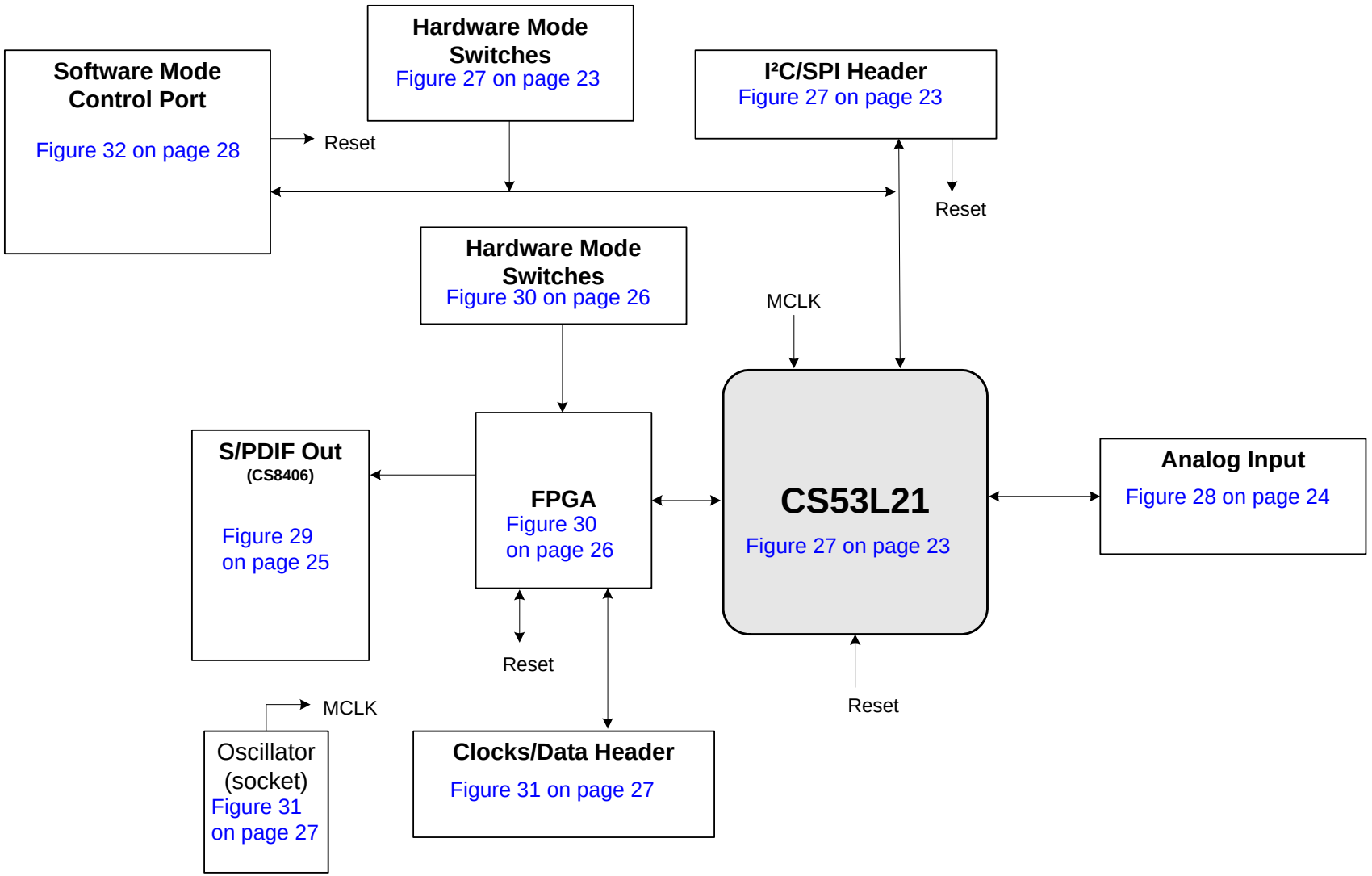
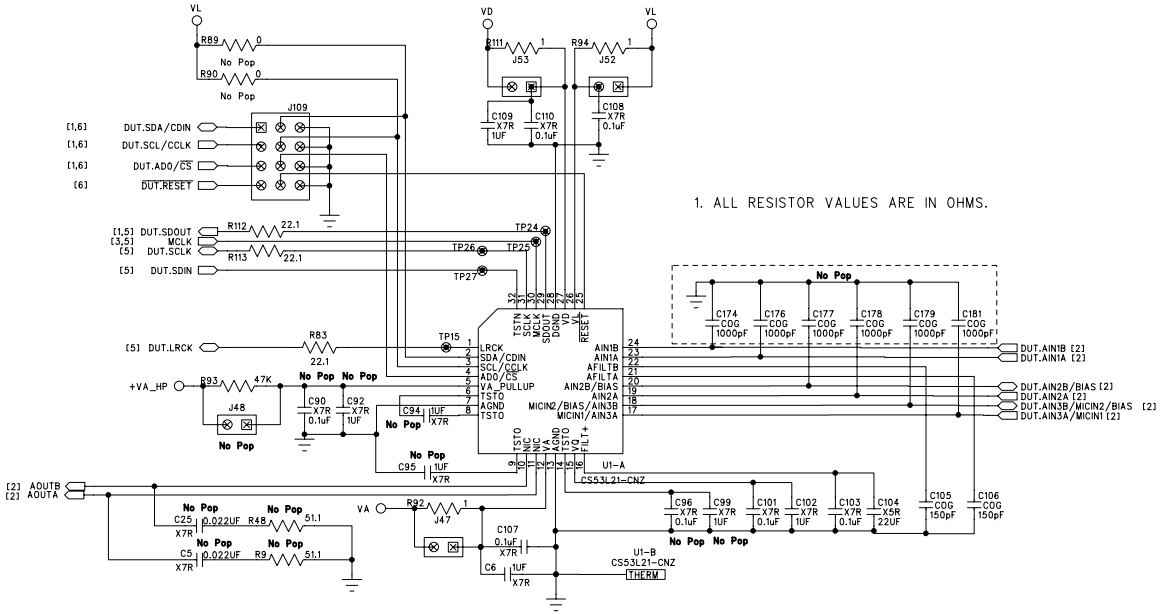


Figure 26. Block Diagram

7. SCHEMATICS



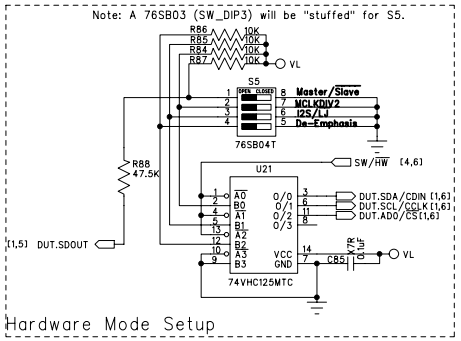
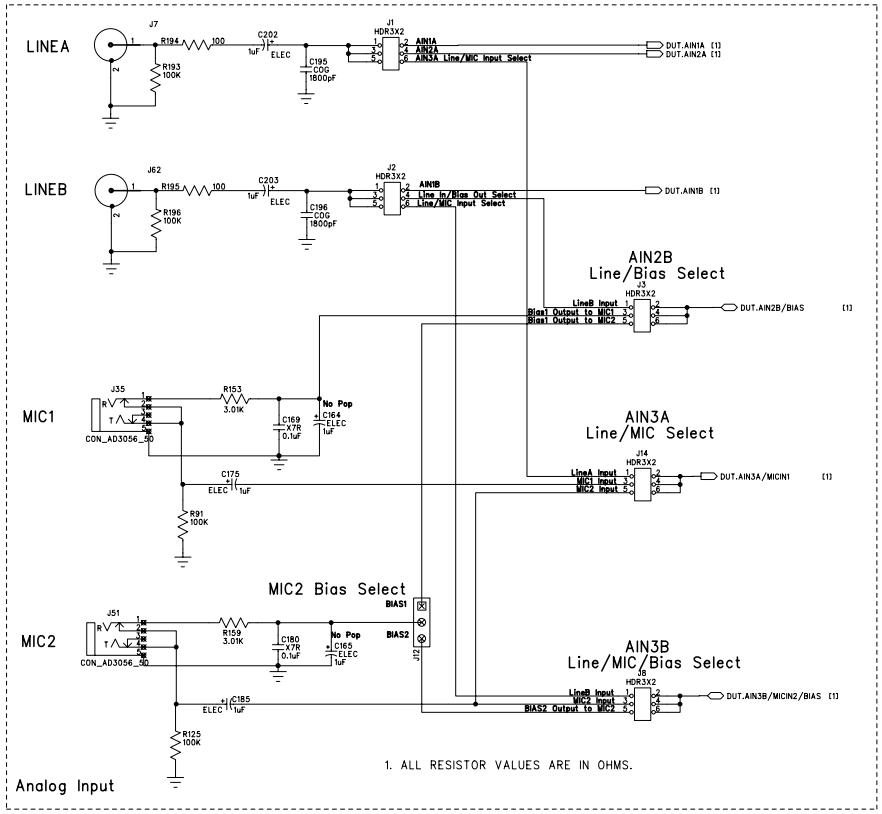


Figure 27. CS53L21 (Part of Schematic Sheet 1)



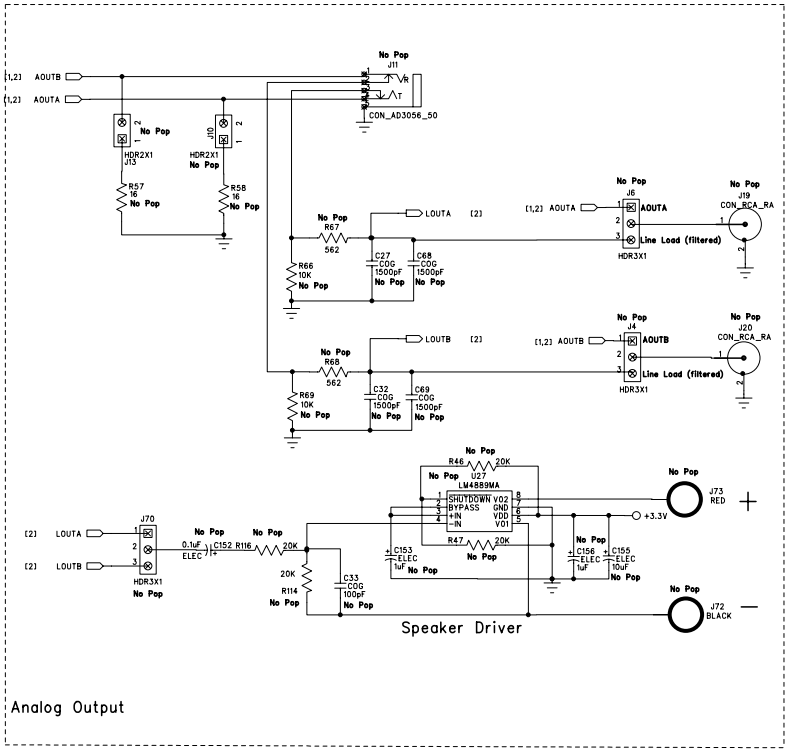


Figure 28. Analog I/O (Part of Schematic Sheet 1)

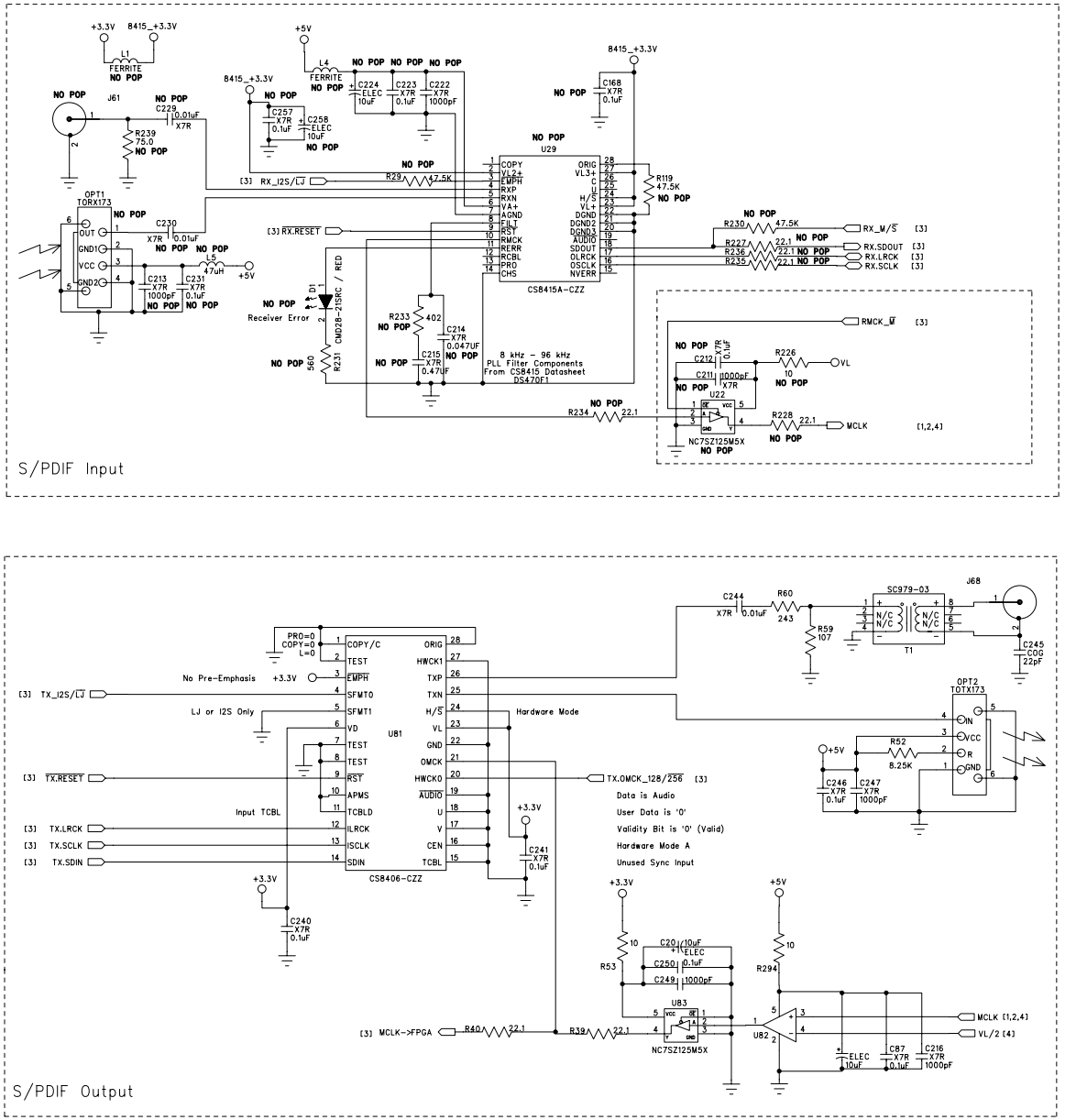


Figure 29. S/PDIF I/O (Schematic Sheet 2)

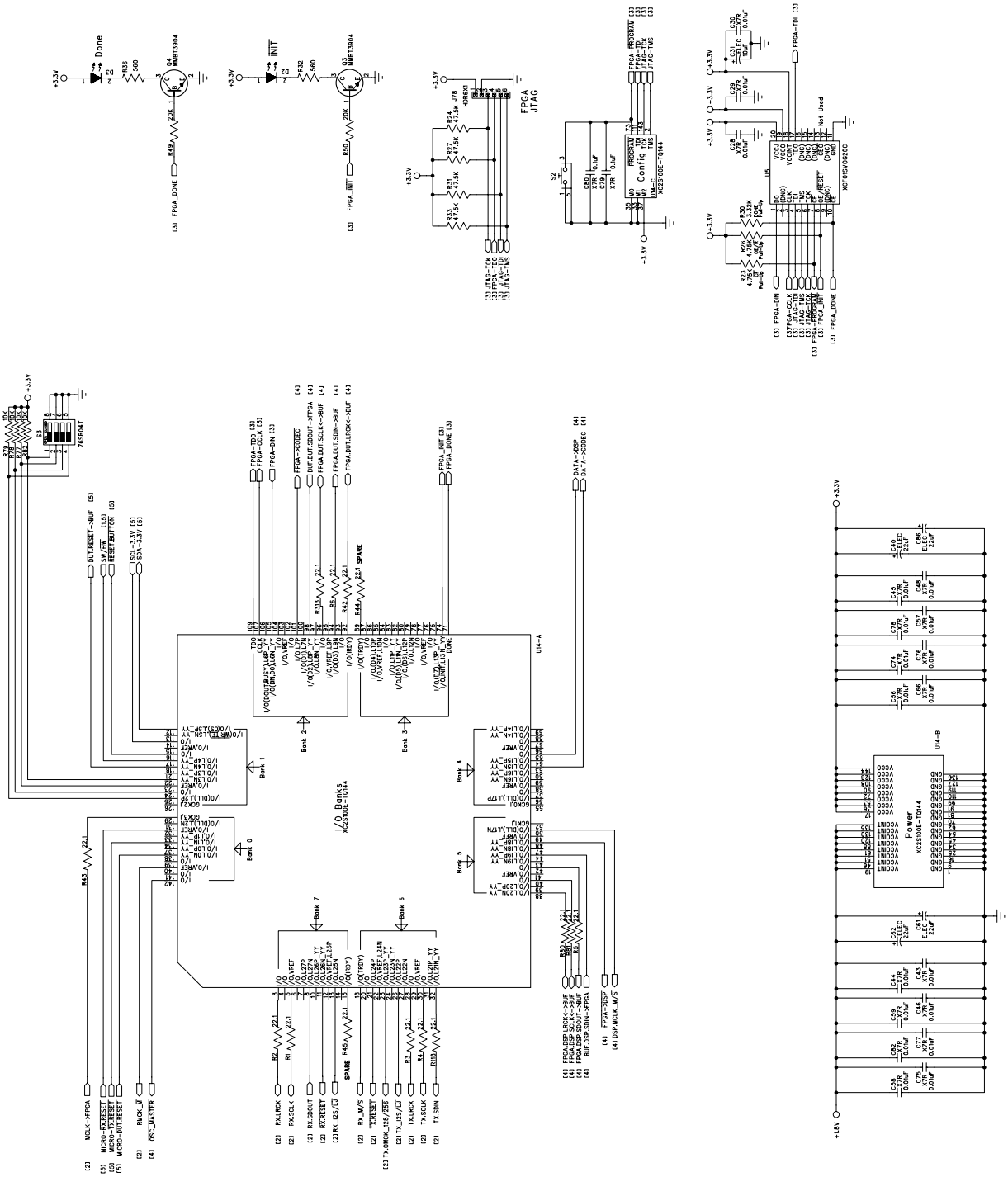


Figure 30. FPGA (Schematic Sheet 3)

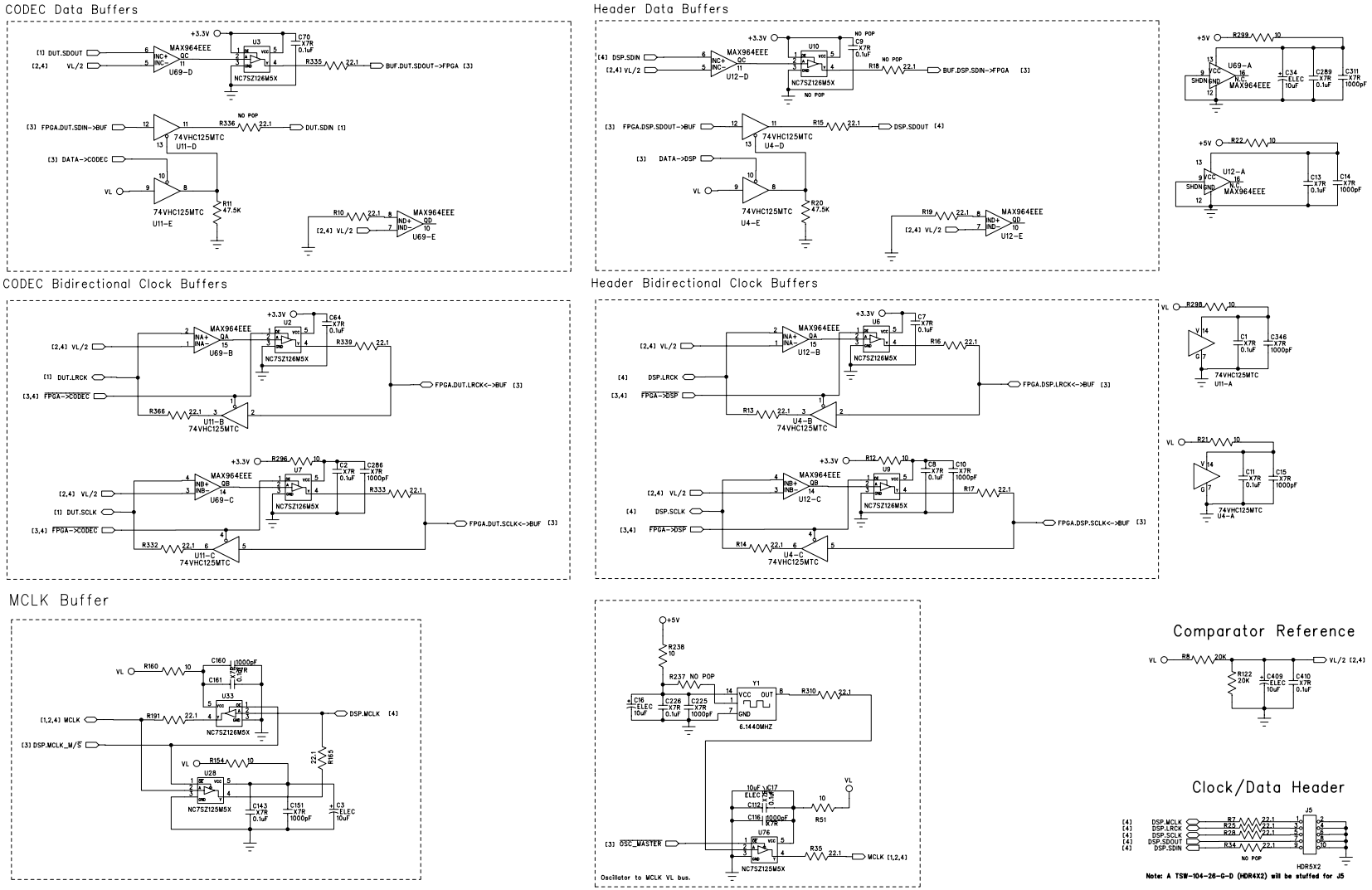


Figure 31. Level Shifters & I/O Stake Header (Schematic Sheet 4)

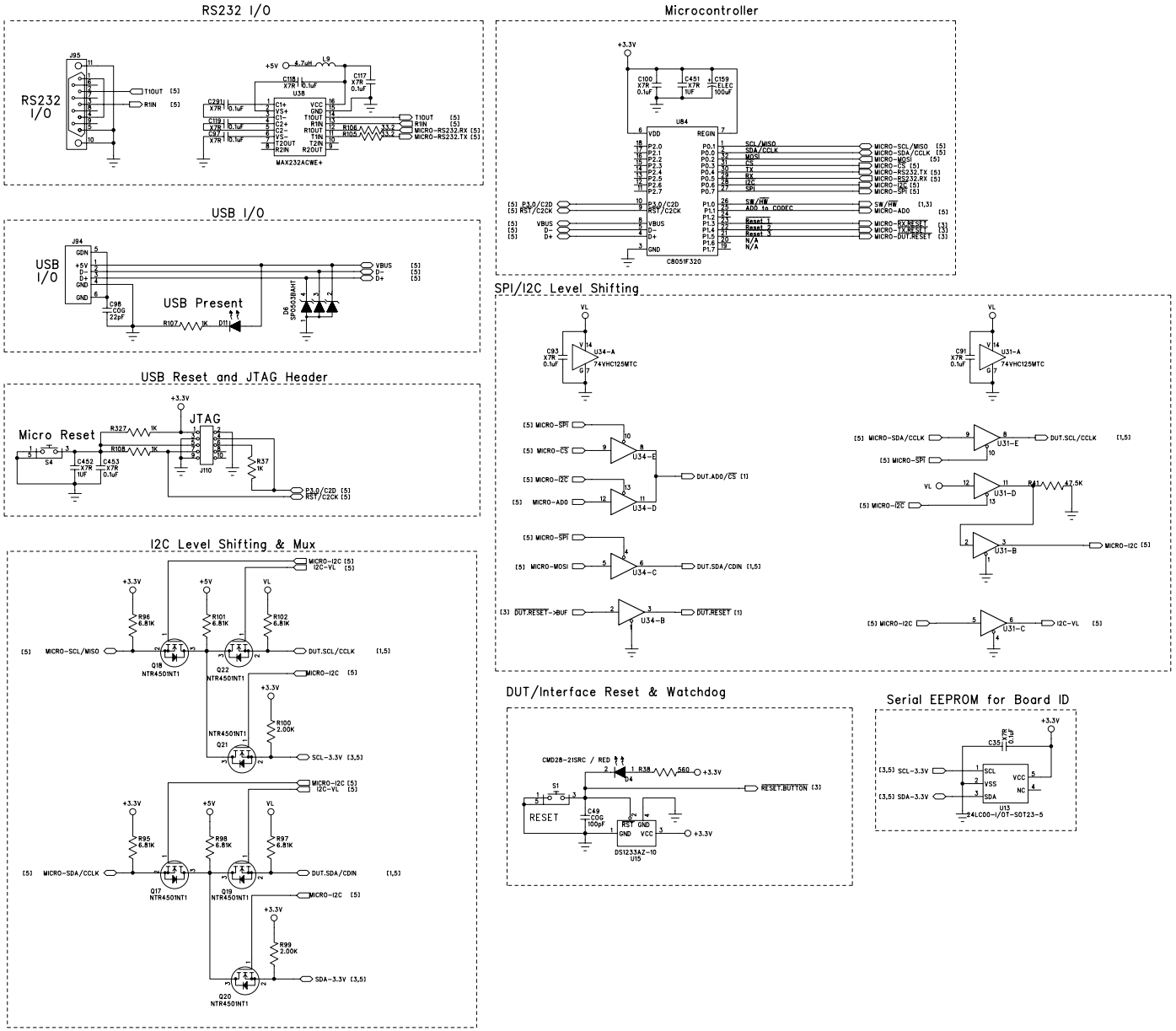


Figure 32. Control Port I/O (Schematic Sheet 5)

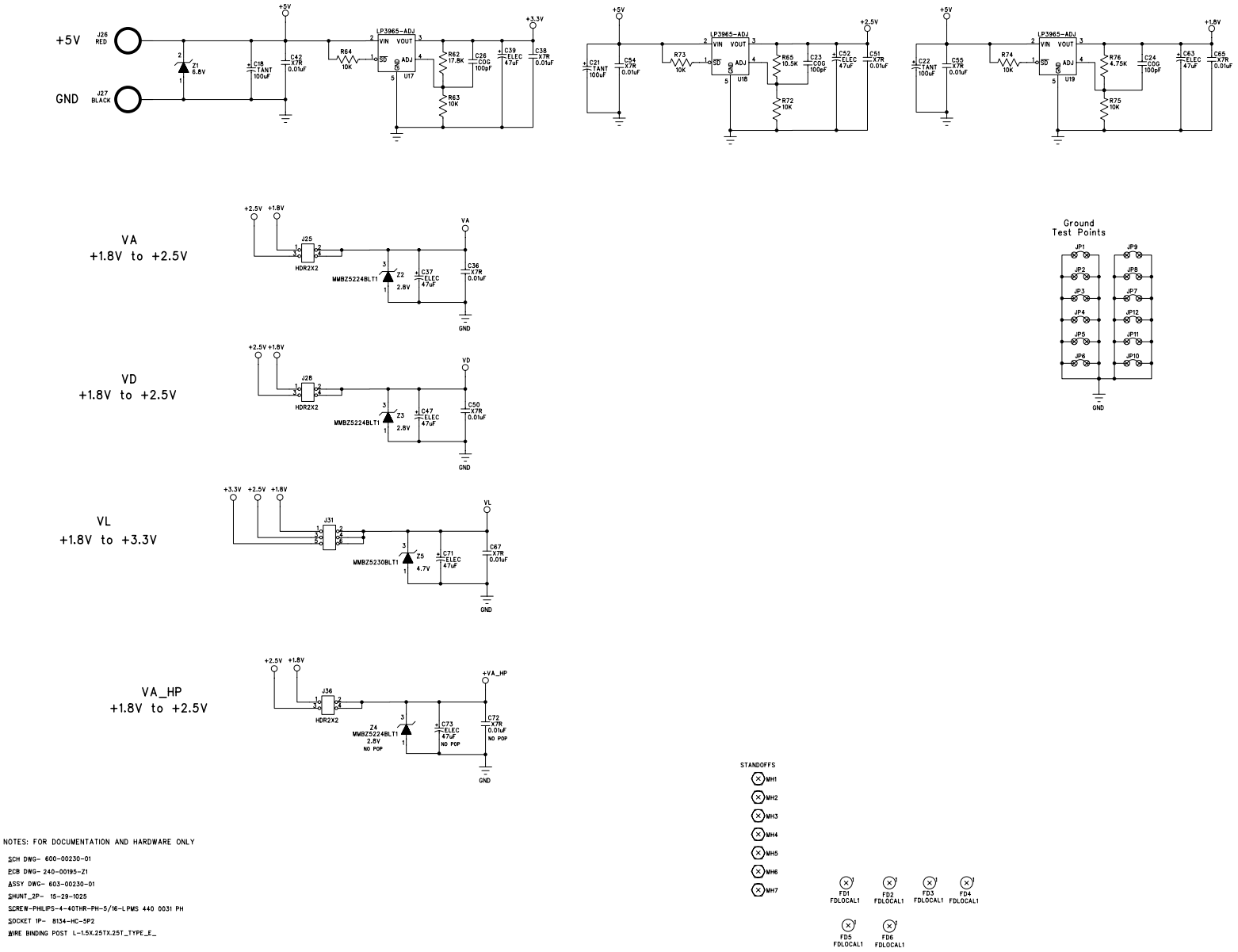


Figure 33. Power (Schematic Sheet 6)lm

8. BOARD LAYOUT

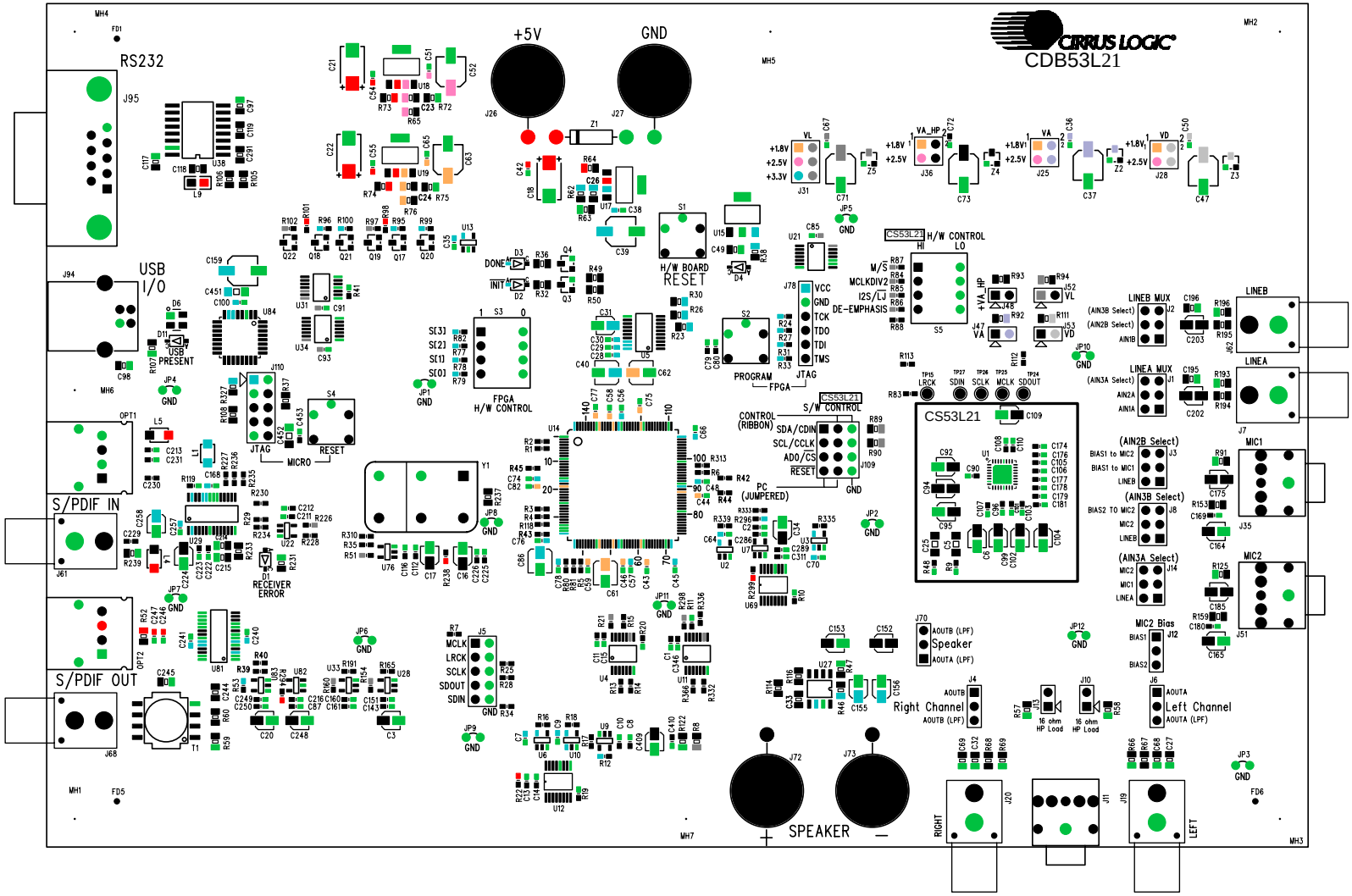


Figure 34. Silk Screen

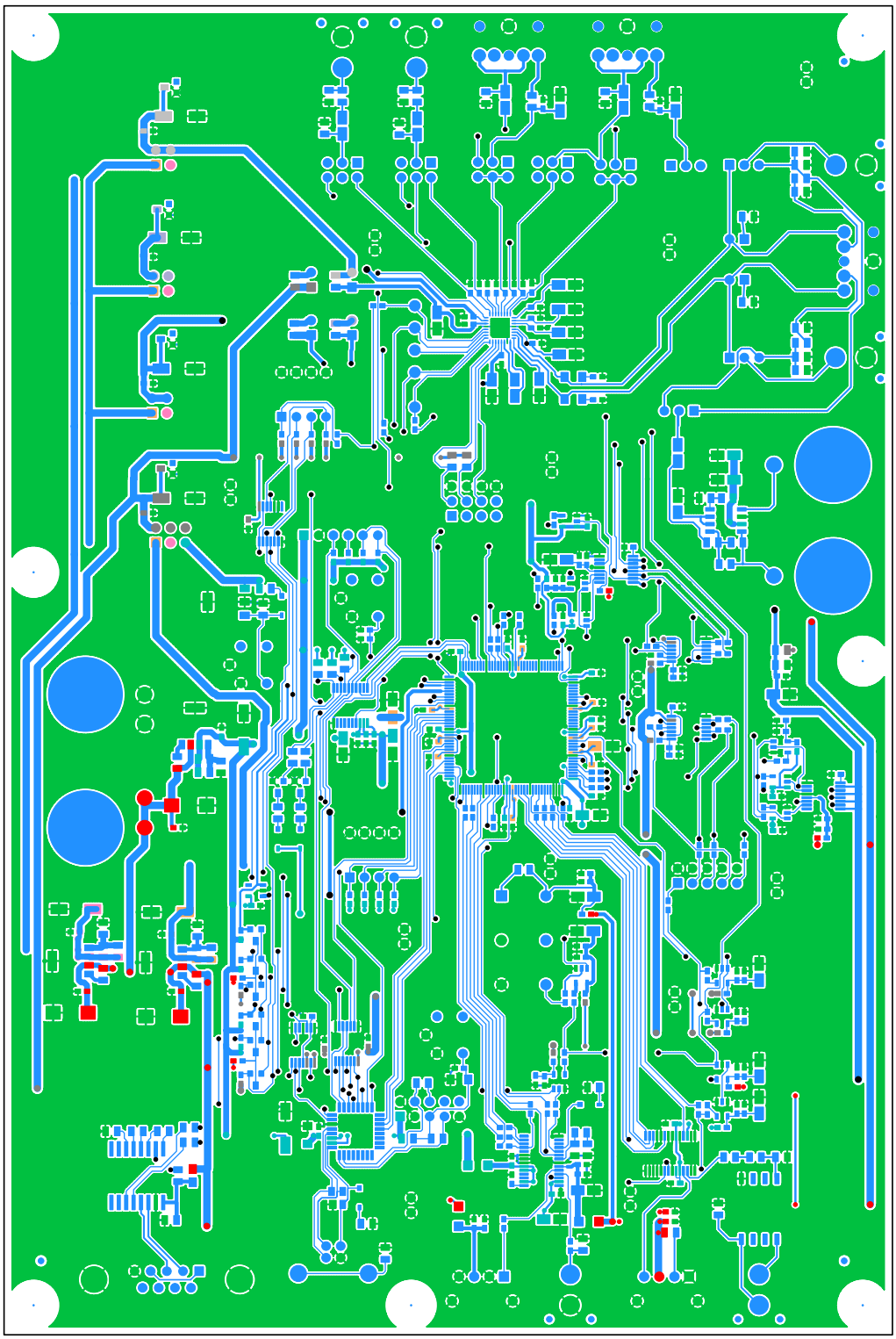


Figure 35. Top-Side Layer

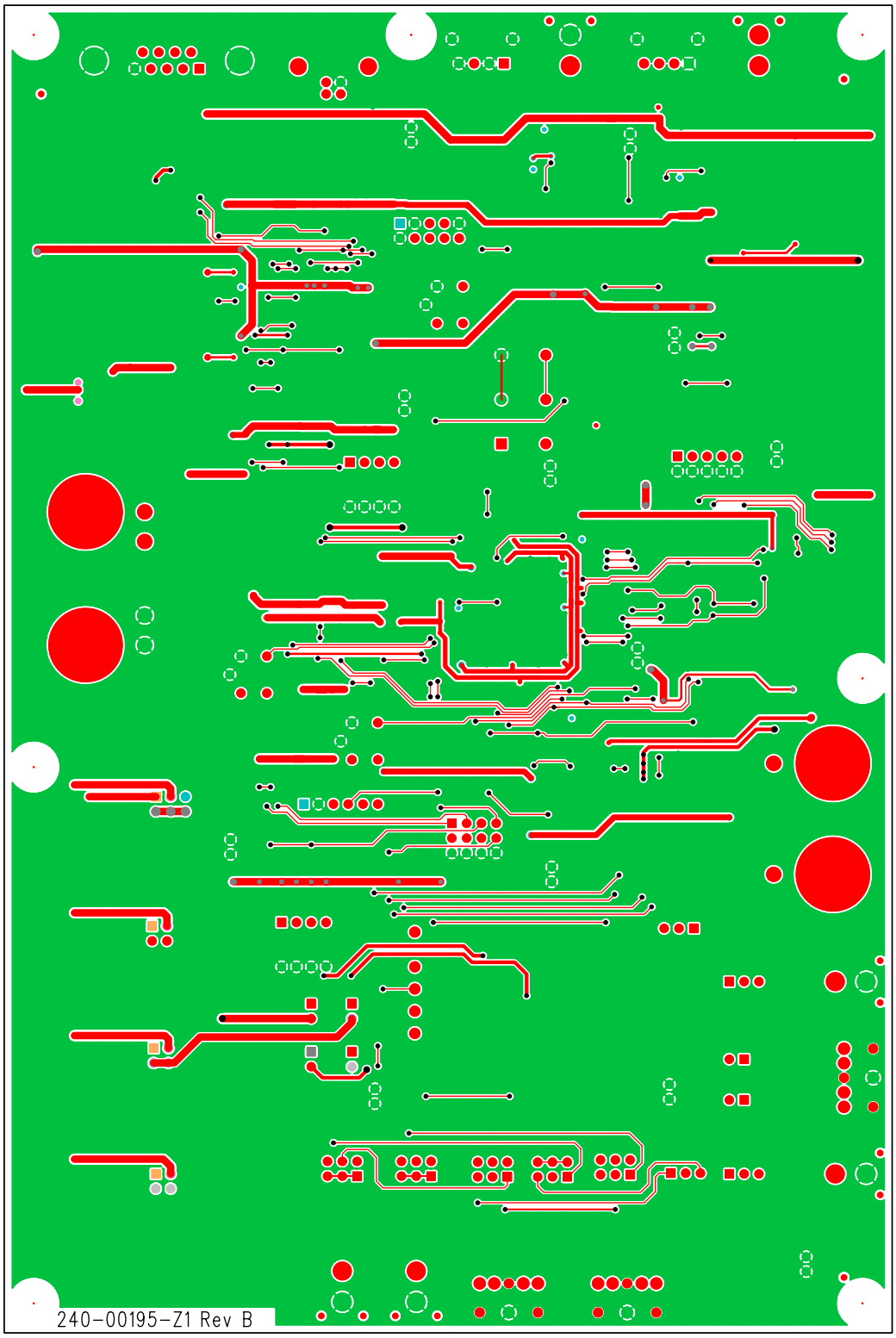


Figure 36. Bottom-Side Layer

9. REVISION HISTORY

Revision	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com

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