CDB4385A

Evaluation Board for CS4385A

Features

- Demonstrates recommended layout and grounding arrangements
- CS8416 receives S/PDIF, & EIAJ-340 compatible digital audio
- Headers for external audio input for either PCM or DSD
- Requires only a digital signal source and power supplies for a complete digital-to-analog converter system

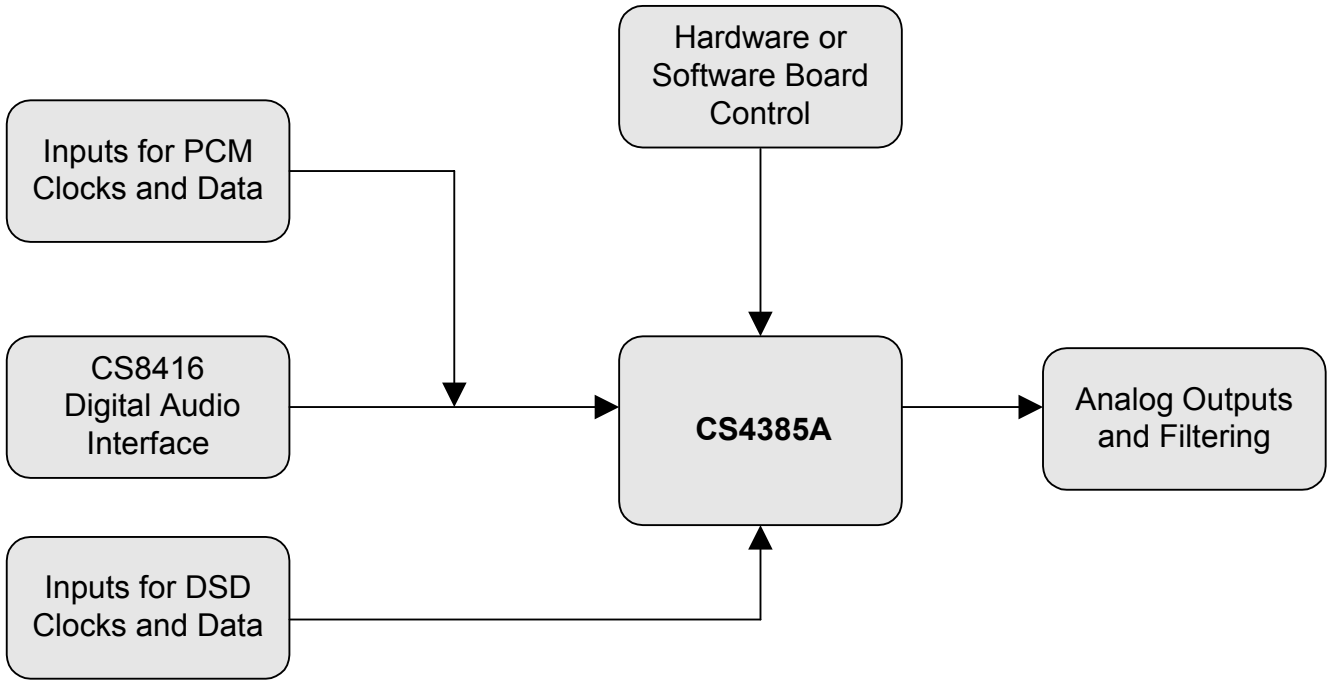
Description

The CDB4385A evaluation board offers an easy way for quickly evaluating the CS4385A 24-bit, 48-pin, 8-channel D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4385A (only required for control port mode), and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the digital-to-analog converter and will accept S/PDIF and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4385A	Evaluation Board



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CDB4385A SYSTEM OVERVIEW

The CDB4385A evaluation board provides a quick method for evaluating the CS4385A. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM or DSD clocks and data through PCB headers for system development.

The CDB4385A schematic is partitioned into the ten schematics shown in Figures 44 through 53. Each partitioned schematic is represented in the system diagram shown in Figure 43. Notice that the system diagram also includes the interconnections between the partitioned schematics.

1. CS4385A DIGITAL-TO-ANALOG CONVERTER

A description of the CS4385A is included in the CS4385A datasheet.

2. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 digital audio receiver (Figure 49). The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is fixed to I^2S. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial, see Figure 49. However, both inputs cannot be driven simultaneously.

Switch position 7 of S1 sets the output MCLK-to-LRCK ratio of the CS8416. This switch should be set to 256 (closed) for inputs Fs≤96 kHz and 128 (open) for Fs≥64 kHz. The CS8416 must be manually reset using 'HW RST' (S2) or through the software when this switch is changed.

3. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via headers J11 and J7. Header J11 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 50. Switch position 6 of S1 selects the source as either CS8416 (open) or header J11 (closed).

Header J7 allows the evaluation board to accept externally generated DSD data and clocks. The schematic for the clock/data input is shown in Figure 50. A synchronous MCLK must still be provided via Header J11. Switch position 8 of S1 selects either PCM (open) or DSD (closed).
Please see the CS4385A datasheet for more information.

4. INPUT FOR CONTROL DATA

The evaluation board can be run in either a standalone mode or with a PC. Standalone mode uses the CS4385A in hardware mode and the mode pins are configured using switch positions 1 through 5 of S1. PC mode uses software to setup the CS4385A through I²C using the PC's serial port. PC mode is automatically selected when the serial port (RS232) is attached and the CDB4385A software is running (USB operation is not available at this time).

Header J15 offers the option for external input of RST and SPI™/I²C clocks and data. The board is setup from the factory to use the on-board microcontroller in conjunction with the supplied software. To use an external control source, remove the shunts on J15 and place a ribbon cable so the signal lines are on the center row and the grounds are on the right side. R116 and R119 should be populated with 2-kΩ resistors when using an external I^2C source which does not already provide pull-ups.

5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (GND, +5V, +12V, and -12V), see Figure 53. The '+5V' terminal supplies VA and the rest of the +5-V circuitry on the board. The +3.3-V circuitry is powered from a regulator. The +2.5 volts required for VD is also provided from an on-board regulator. The +5-V supply should be set within the recommended values for VA stated in the CS4385A datasheet.

WARNING: Refer to the CS4385A datasheet for maximum allowable voltage levels. Operation outside this range can cause permanent damage to the device.

6. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4385A requires close attention to power supply and grounding arrangements to optimize performance. Figure 44 details the connections to the CS4385A; Figures 54, 55, and 56 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4385A as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

7. ANALOG OUTPUT FILTERING

The analog output on the CDB4385A is designed according to the CS4385A datasheet. The output circuit includes an active 2-pole, 50-kHz filter which utilizes the multiple-feedback topology.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 V power
GND	Input	Ground connection from power supply
+12V	Input	+12 V positive supply for the on-board filtering
-12V	Input	-12 V negative supply for the on-board filtering
S/PDIF IN - J9	Input	Digital audio interface input via coax
S/PDIF IN - OPT1	Input	Digital audio interface input via optical
PCM INPUT - J11	Input	Input for master, serial, left/right clocks and serial data
DSD INPUT - J7	Input	Input for DSD serial clock and DSD data
OUTA1-B4	Output	RCA line level analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
J15	Selects source of control data	*shunts on Left shunts removed	*Control from PC and on-board microcontroller External control input using center and right columns
J16	JTAG micro programming	-	Reserved for factory use only
S2	Resets CS8416 and CS4385A		The CS8416 must be reset if switch S1 is changed
S1	CS4385A mode settings M0-4	1-5	Default: M0, M4 open (HI) M1, M2, M3 closed (LO)
	Sets clock source	6	Sets clock source for CS4385A *open = RX(CS8416), closed = $\overline{\text{EXT}}$(J11)
	Sets MCLK ratio of CS8416	7	Selects 128x (open) or $\overline{256x}$ (*closed) MCLK/LRCK ratio output for CS8416
	Selects PCM or DSD mode	8	For PCM input set to *Open, for DSD set to Closed
*Default Factory Settings			

Table 2. CDB4385A Jumper Settings

8. PERFORMANCE PLOTS

The plots in the following section were acheived using an Audio Precision System 2700 and a randomly chosen production CDB4385A. In some cases performance may be limited by the CDB4385A. All measurements were taken at room temp using the standard AP filter options (20 Hz to 22 kHz) with default board settings and nominal datasheet voltages applied unless otherwise noted.

The impulse response plots were taken both pre-and post filtering as the off-chip filter was degrading the performance at higher sample rates. The pre-filter impulse response plots were taken directly at the output pins of the DAC (with the analog filter still connected) to show the effect of the CDB's analog filtering on the impulse response (as the analog filtering adds its own signature to the impulse response of the DAC, and in the case of the higher sampling rates it was band-limiting it).

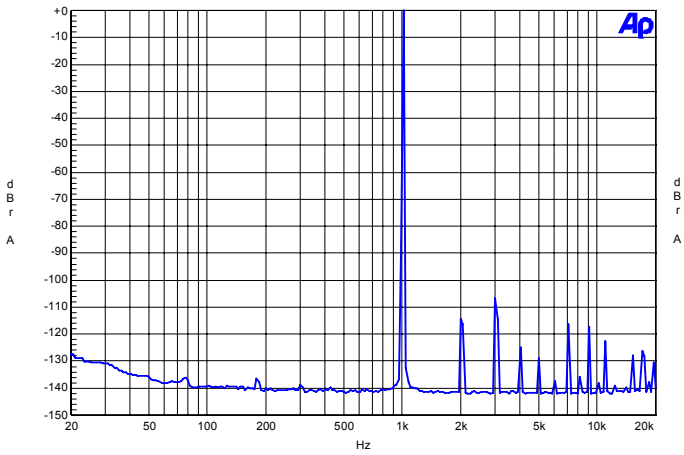


Figure 1. FFT (48 kHz, 0 dB)

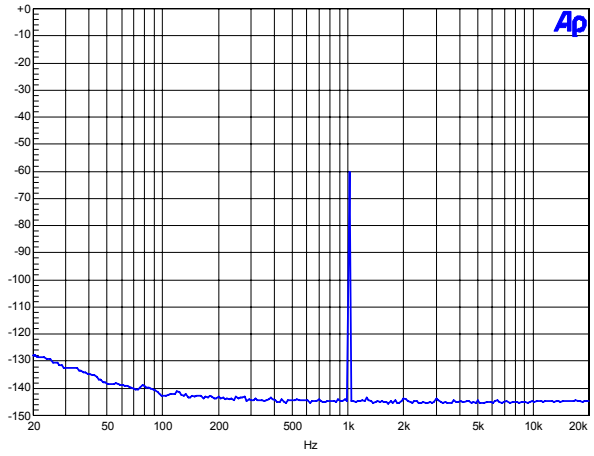


Figure 2. FFT (48 kHz, -60 dB)

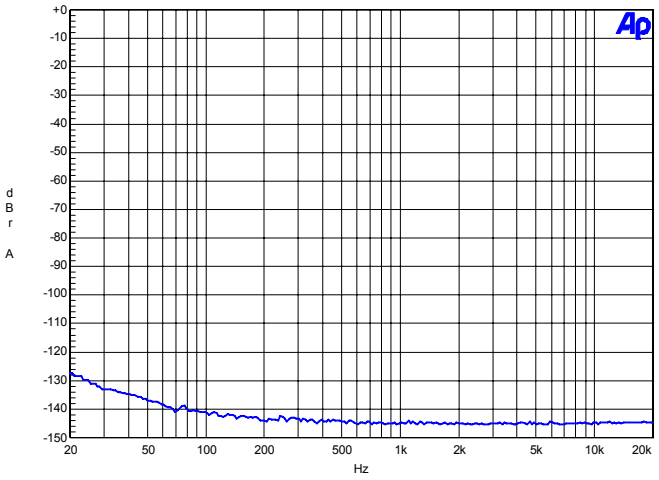


Figure 3. FFT (48 kHz, No Input)

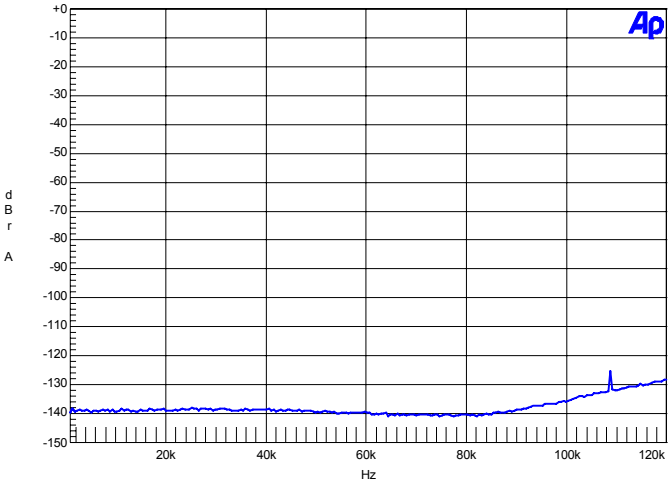


Figure 4. FFT (48 kHz Out-of-Band, No Input)

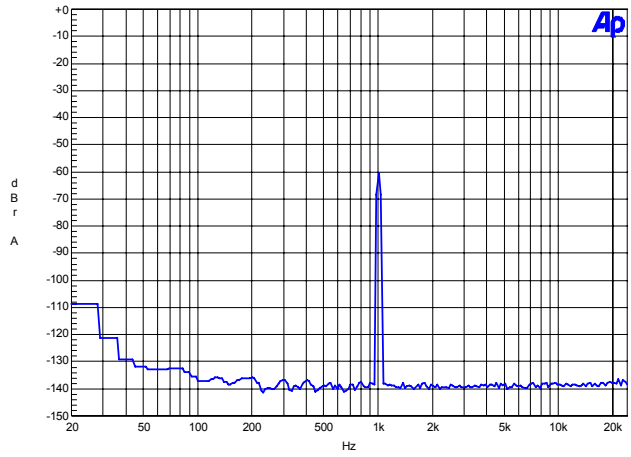


Figure 5. FFT (48 kHz, -60 dB Wideband)

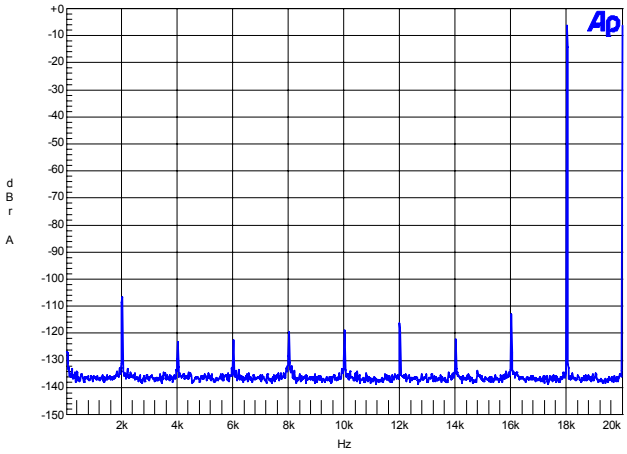


Figure 6. FFT (IMD 48 kHz)

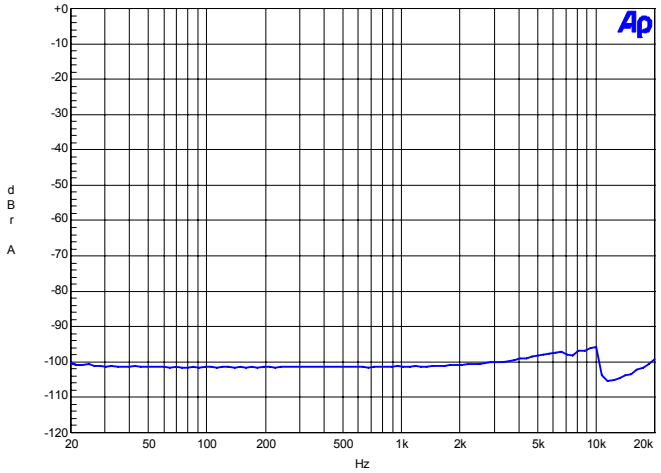


Figure 7. 48 kHz, THD+N vs. Input Freq

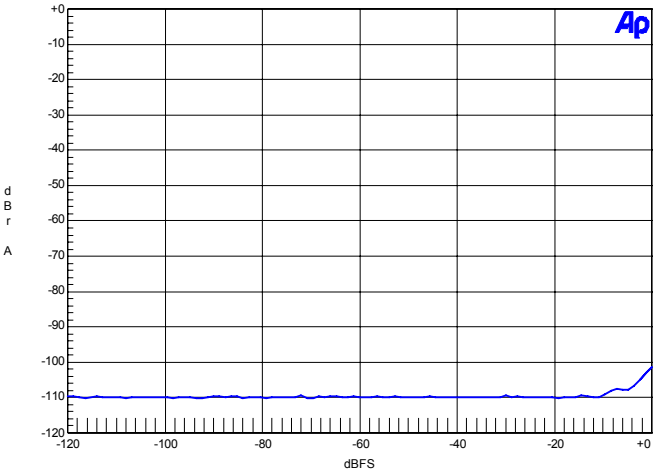


Figure 8. 48 kHz, THD+N vs. Level

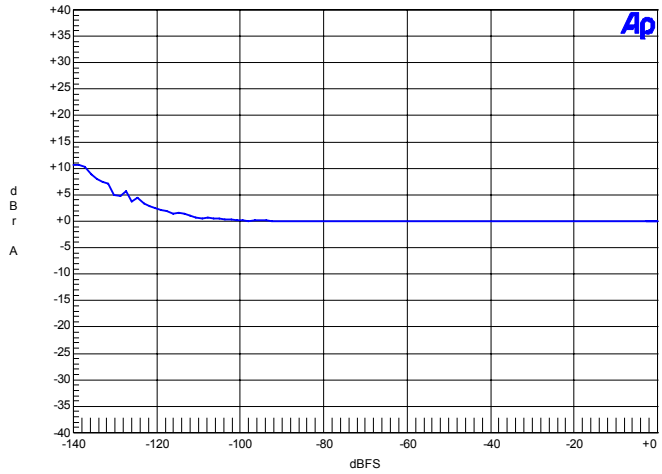


Figure 9. 48 kHz, Fade-to-Noise Linearity

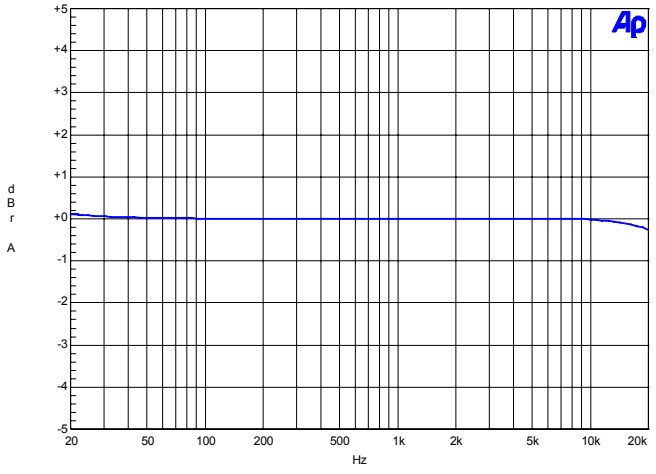


Figure 10. 48 kHz, Frequency Response

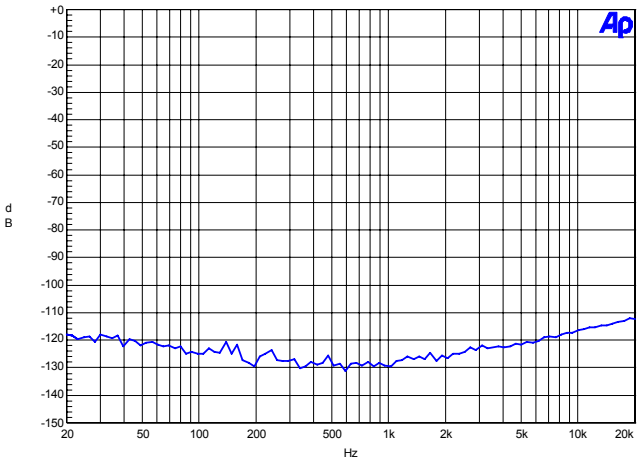


Figure 11. 48 kHz, Crosstalk

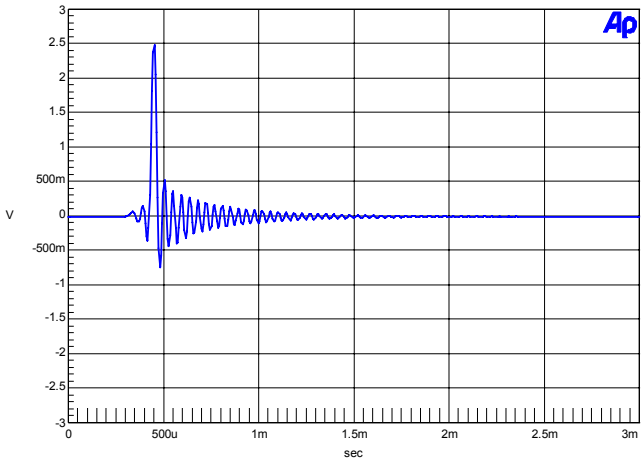


Figure 12. 48 kHz, Impulse Response

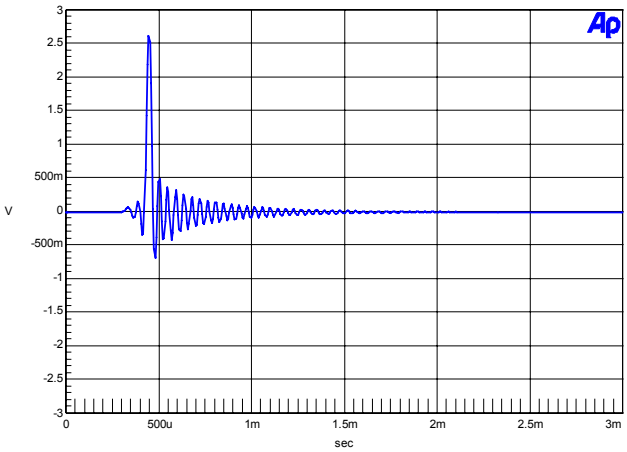


Figure 13. 48 kHz, Impulse Prefilter

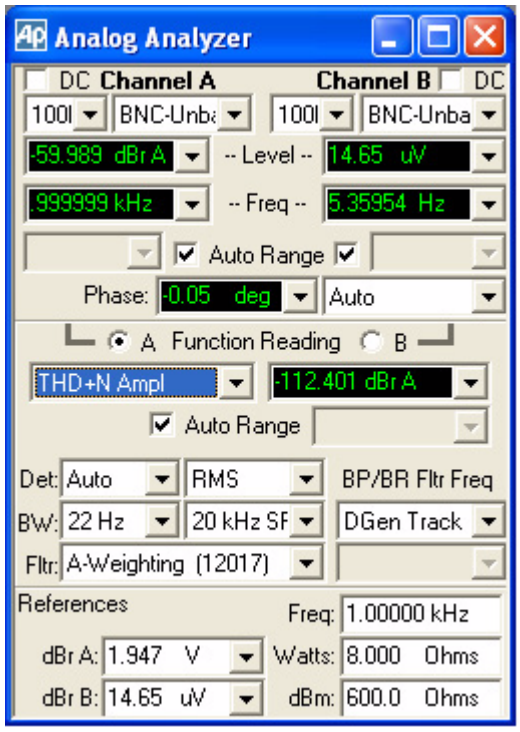


Figure 14. Dynamic Range 48 kHz

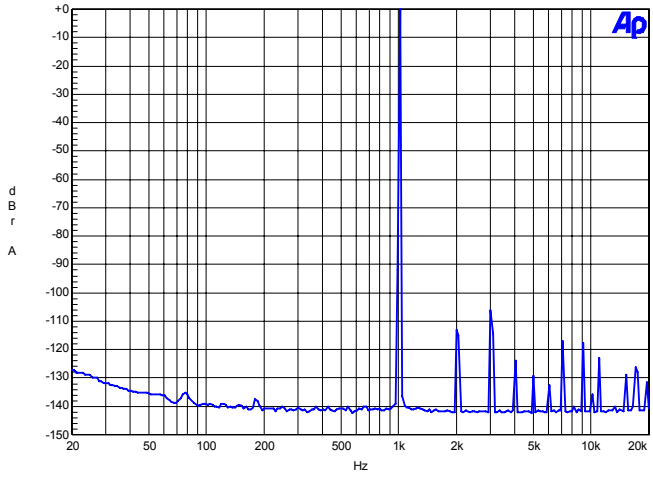


Figure 15. FFT (96 kHz, 0 dB)

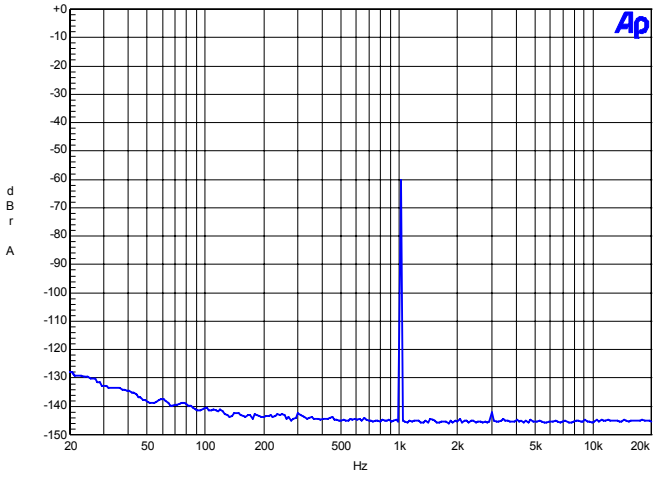


Figure 16. FFT (96 kHz, -60 dB)

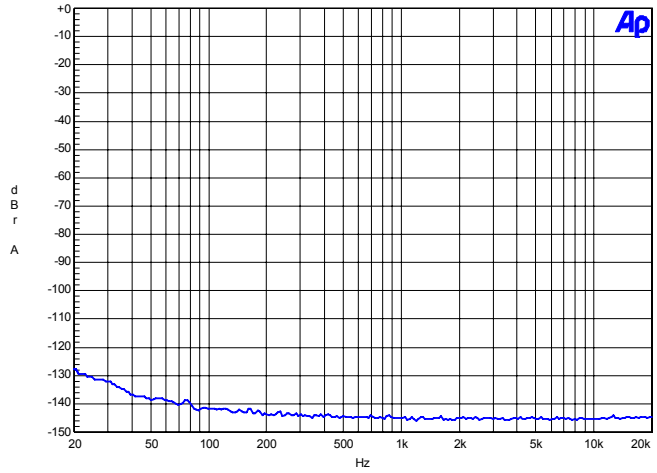


Figure 17. FFT (96 kHz, No Input)

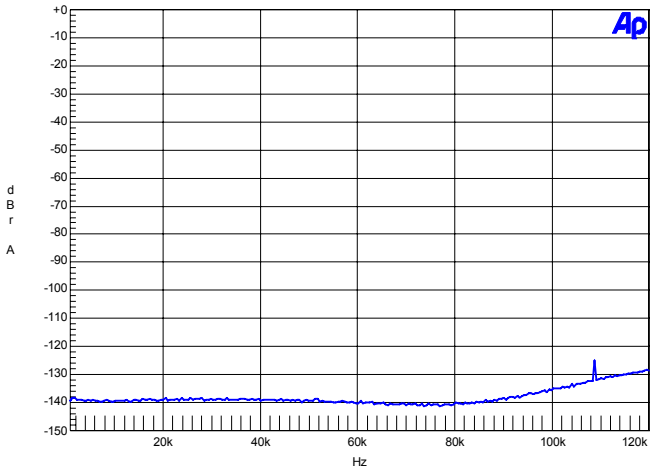


Figure 18. FFT (96 kHz Out-of-Band, No Input)

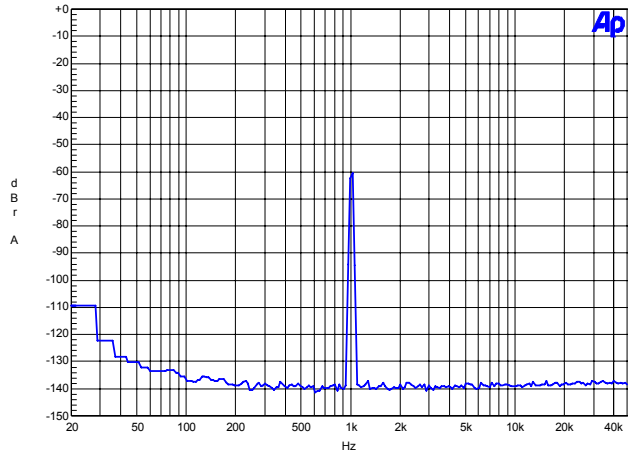


Figure 19. FFT (96 kHz, -60 dB Wideband)

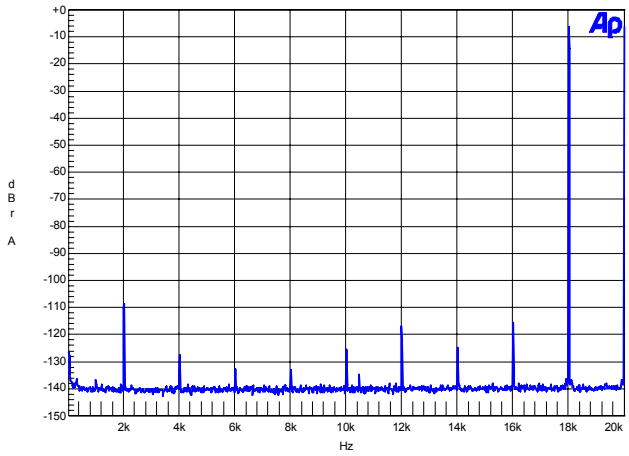


Figure 20. FFT (IMD 96 kHz)

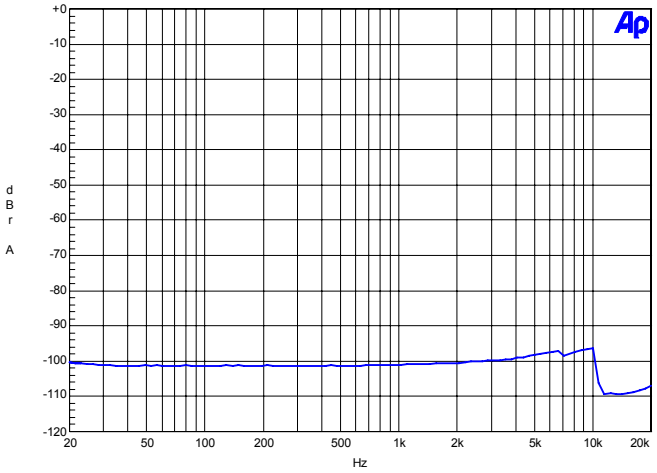


Figure 21. 96 kHz, THD+N vs. Input Freq

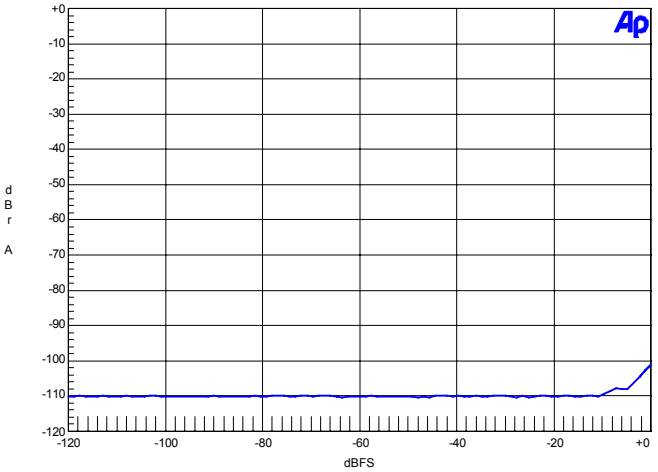


Figure 22. 96 kHz, THD+N vs. Level

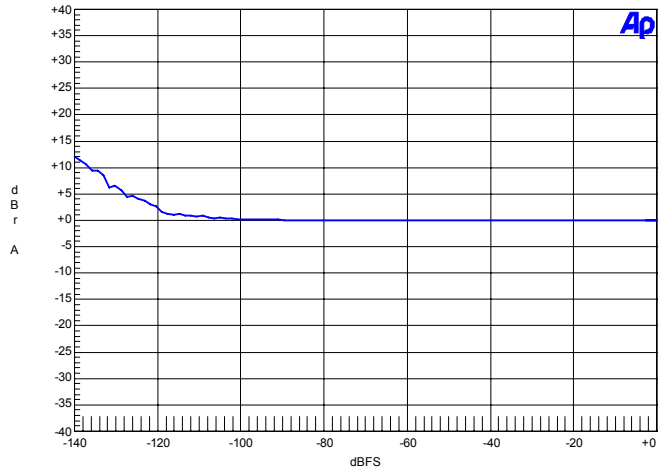


Figure 23. 96 kHz, Fade-to-Noise Linearity

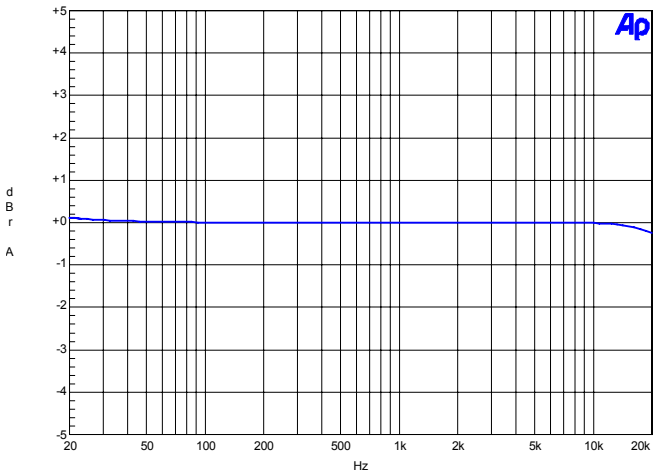


Figure 24. 96 kHz, Frequency Response

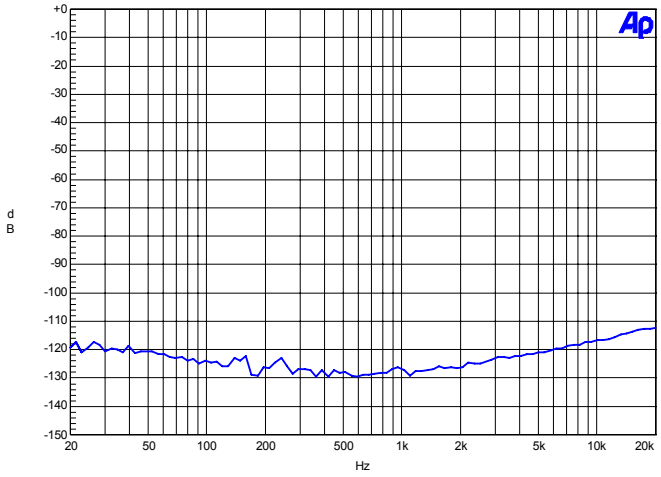


Figure 25. 96 kHz, Crosstalk

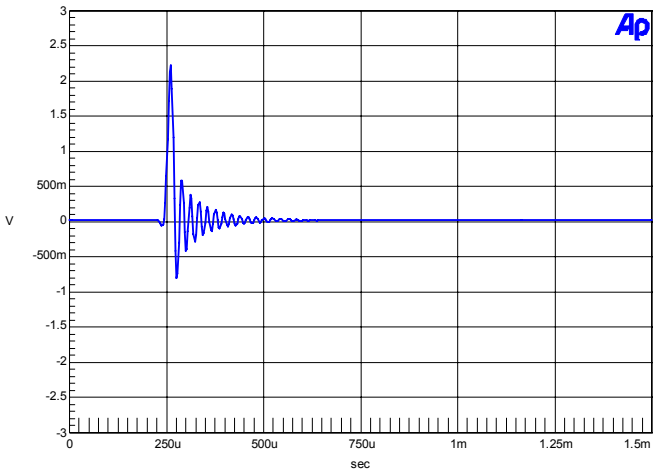


Figure 26. 96 kHz, Impulse Response

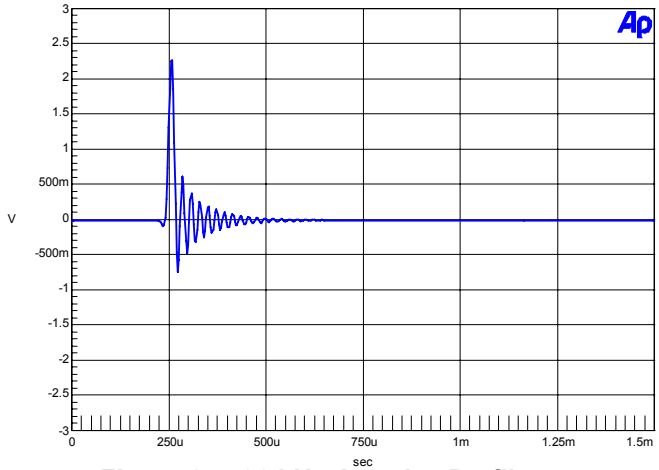


Figure 27. 96 kHz, Impulse Prefilter

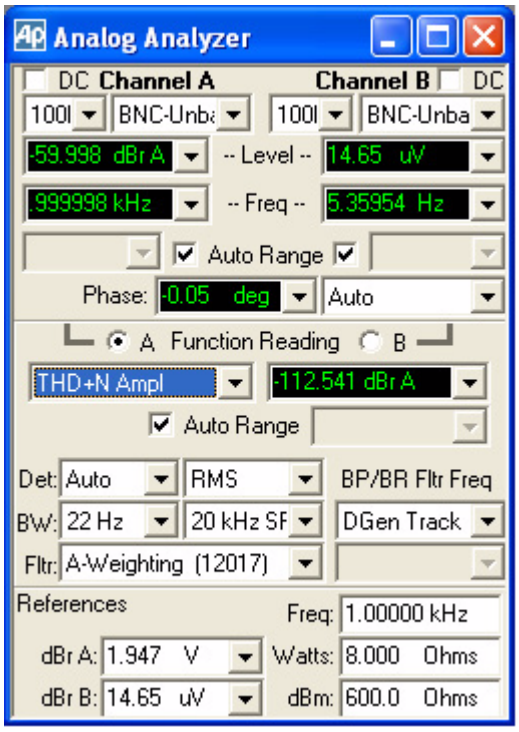


Figure 28. Dynamic Range 96 kHz

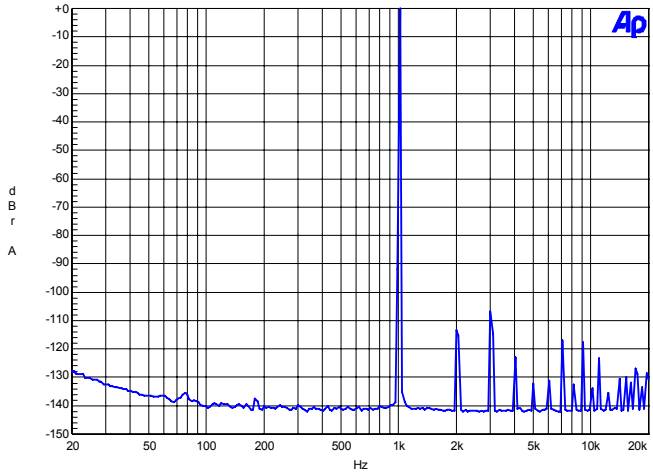


Figure 29. FFT (192 kHz, 0 dB)

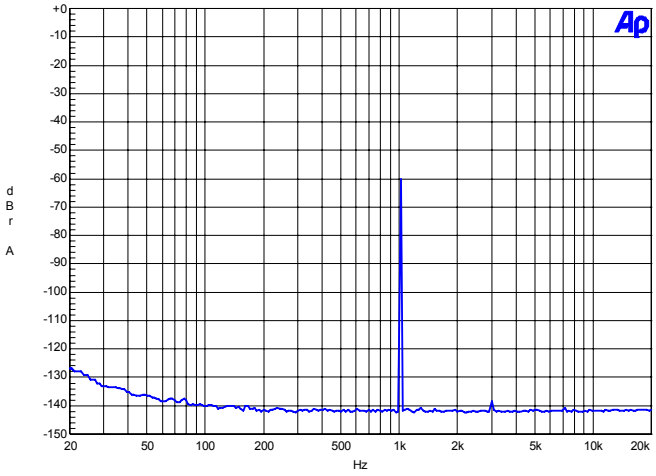


Figure 30. FFT (192 kHz, -60 dB)

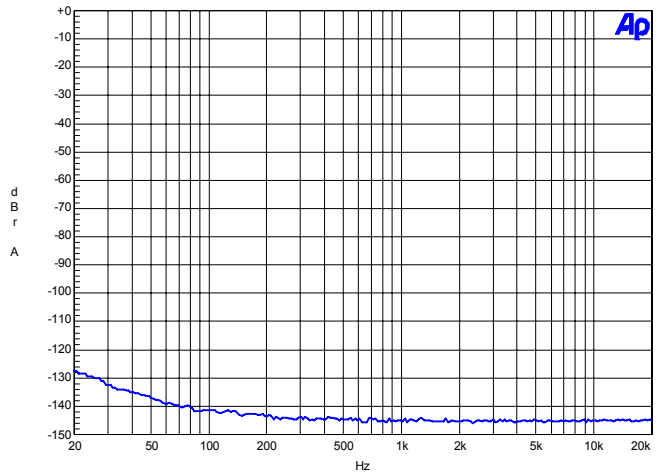


Figure 31. FFT (192 kHz, No Input)

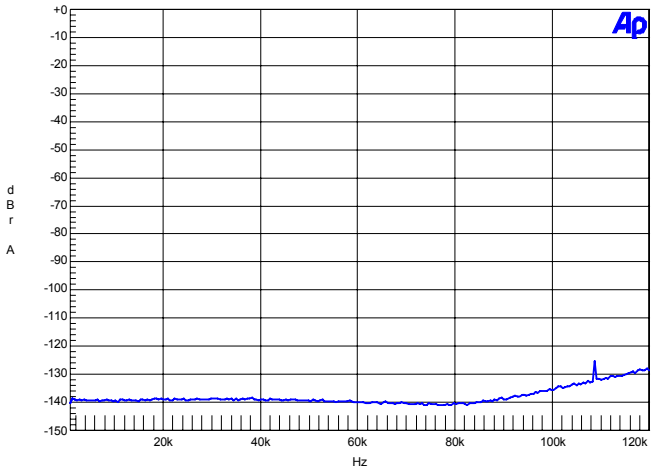


Figure 32. FFT (192 kHz Out-of-Band, No Input)

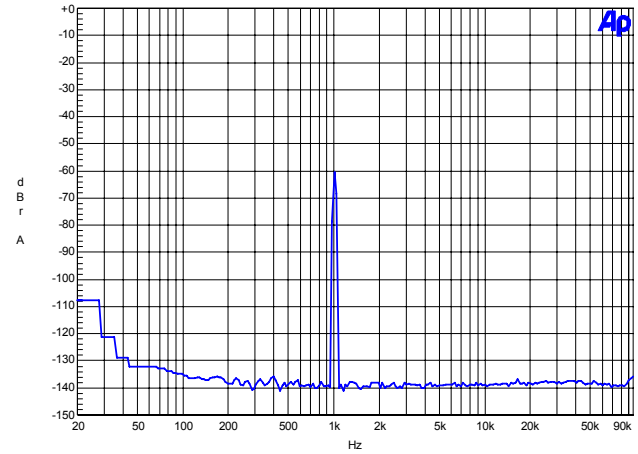


Figure 33. FFT (192 kHz, -60 dB Wideband)

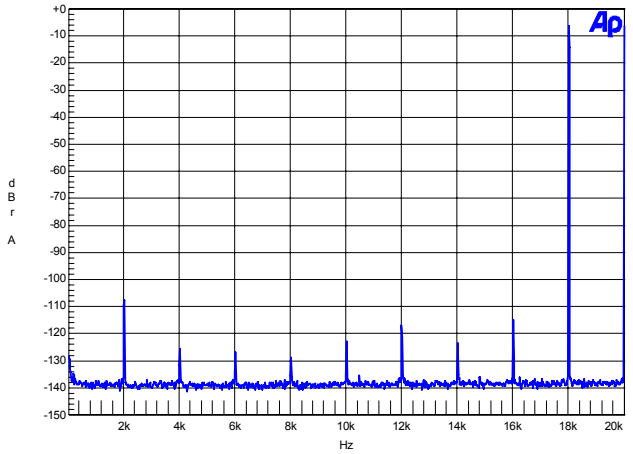


Figure 34. FFT (IMD 192 kHz)

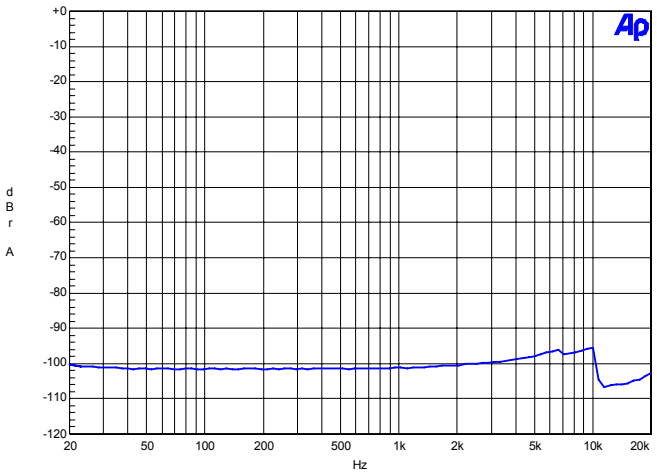


Figure 35. 192 kHz, THD+N vs. Input Freq

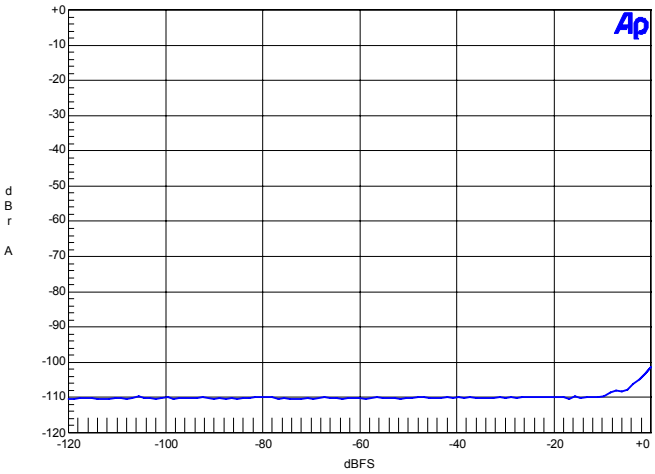


Figure 36. 192 kHz, THD+N vs. Level

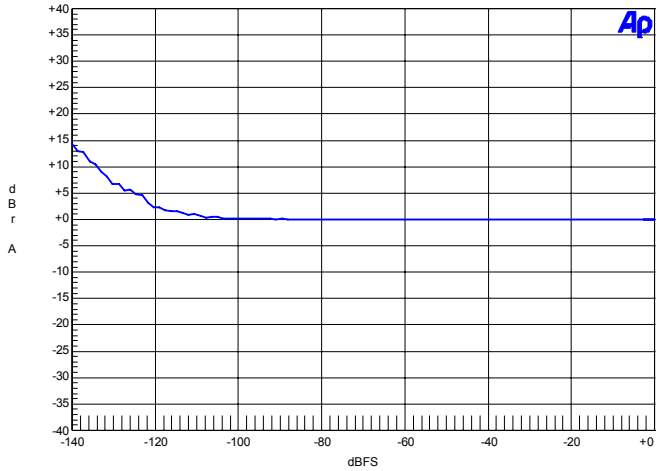


Figure 37. 192 kHz, Fade-to-Noise Linearity

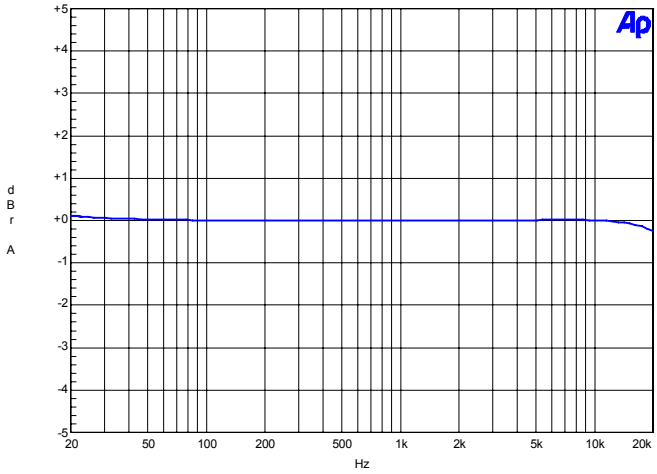


Figure 38. 192 kHz, Frequency Response

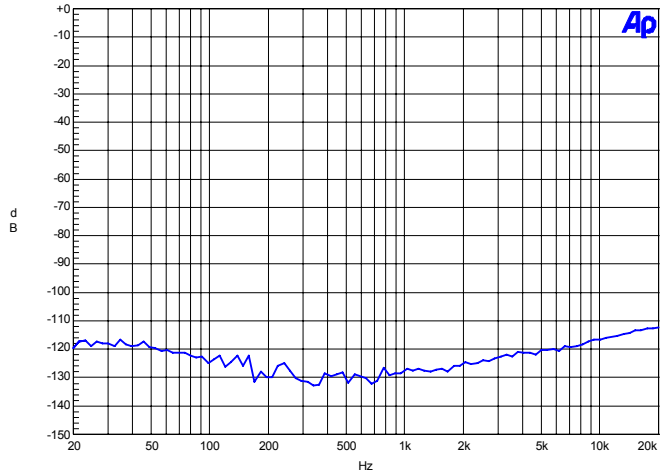


Figure 39. 192 kHz, Crosstalk

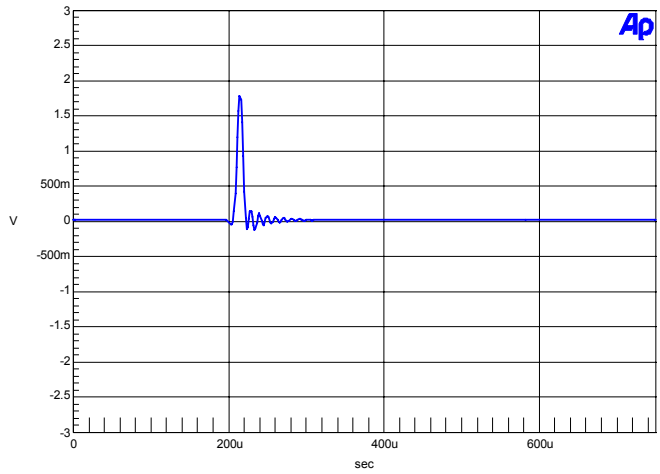


Figure 40. 192 kHz, Impulse Response

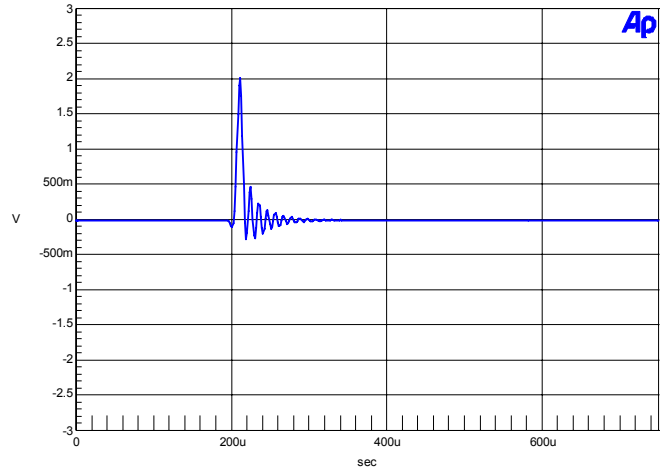


Figure 41. 192 kHz, Impulse Prefilter

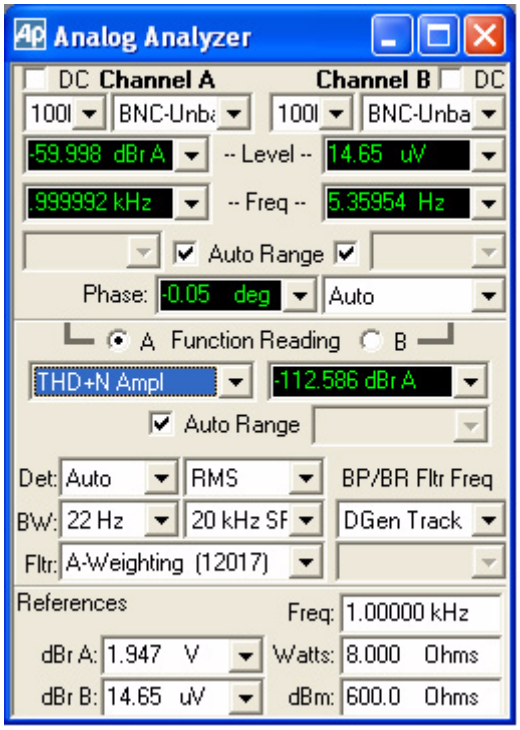


Figure 42. Dynamic Range 192 kHz

9. SCHEMATICS

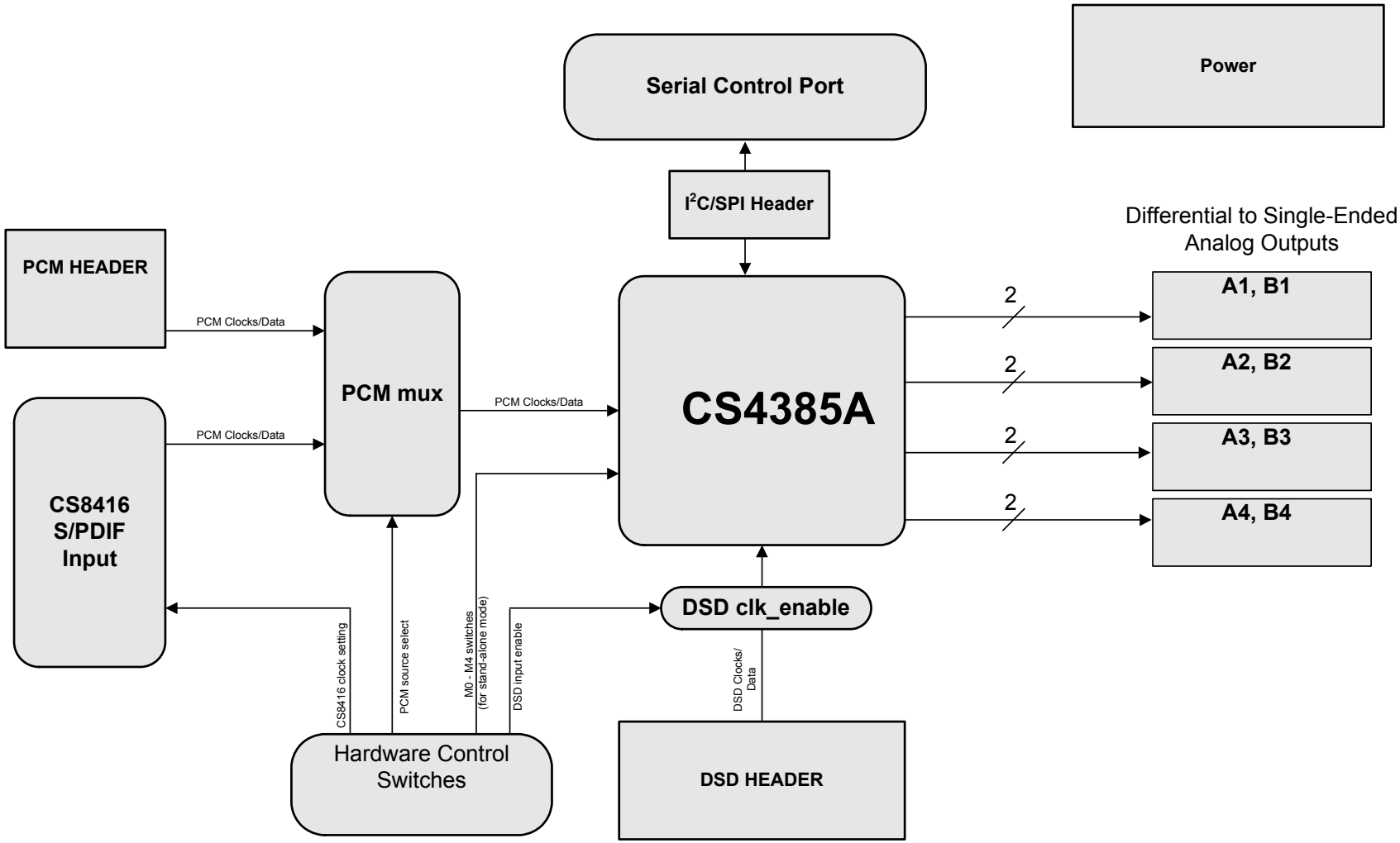


Figure 43. System Block Diagram and Signal Flow

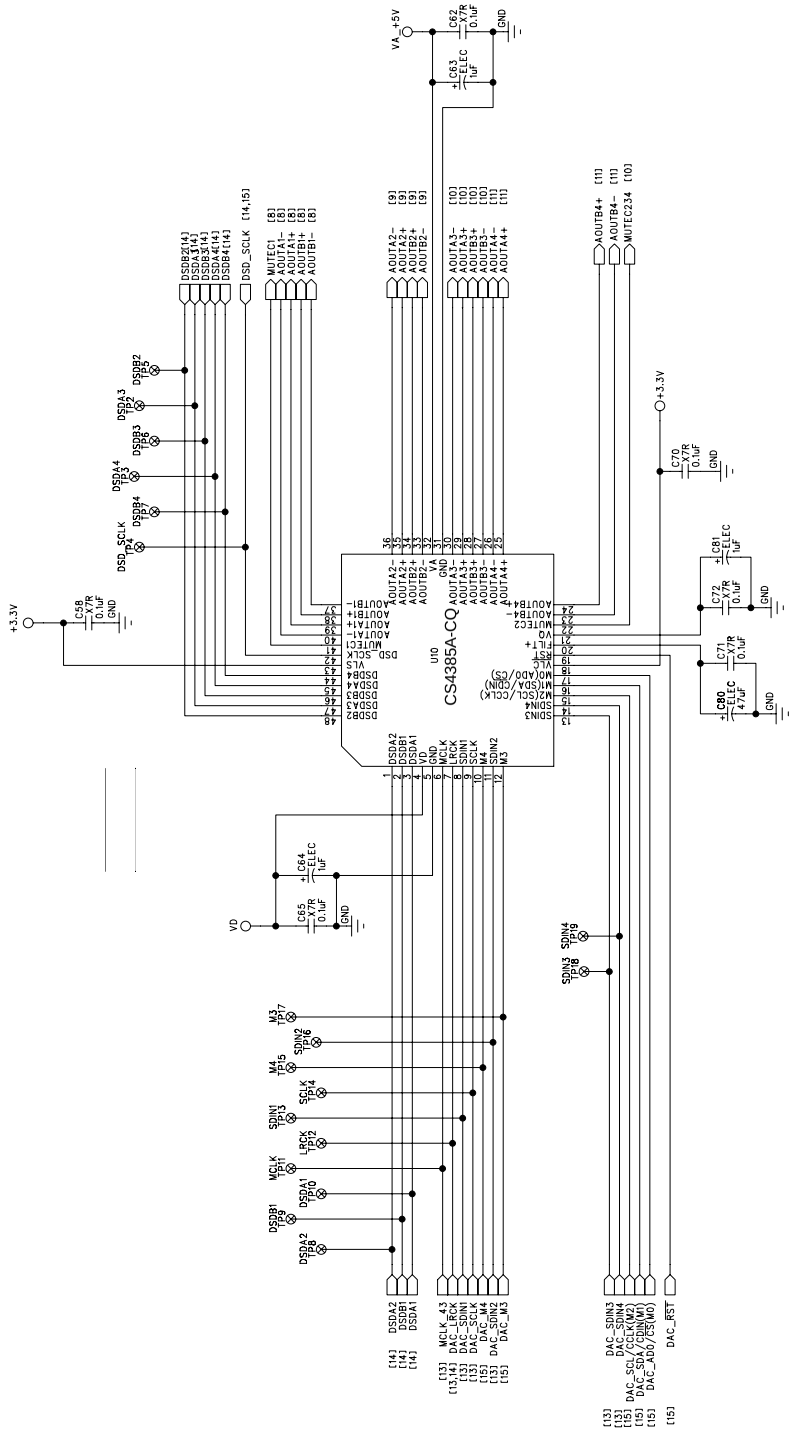


Figure 44. CS4385A

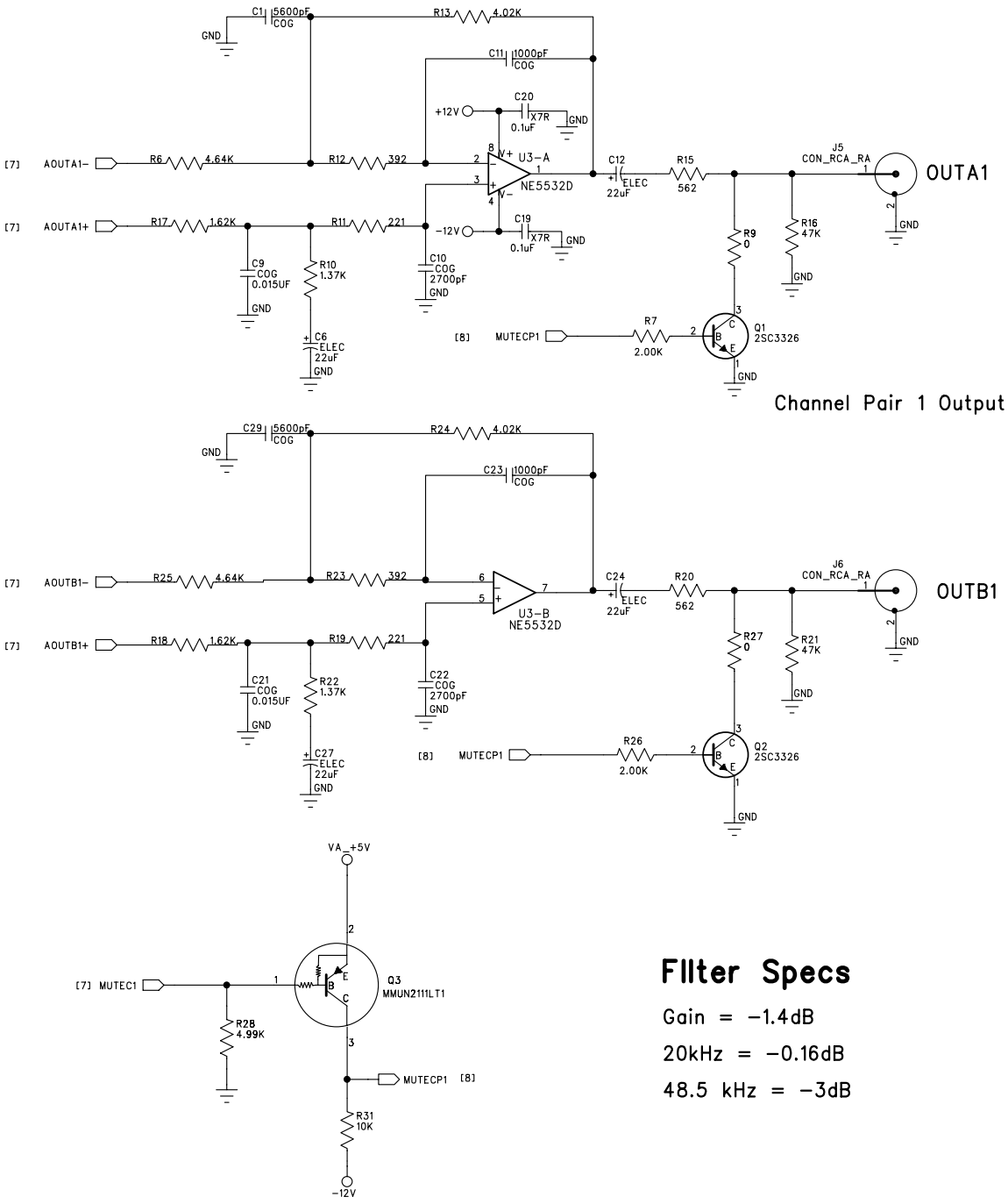


Figure 45. Analog Outputs A1 - B1

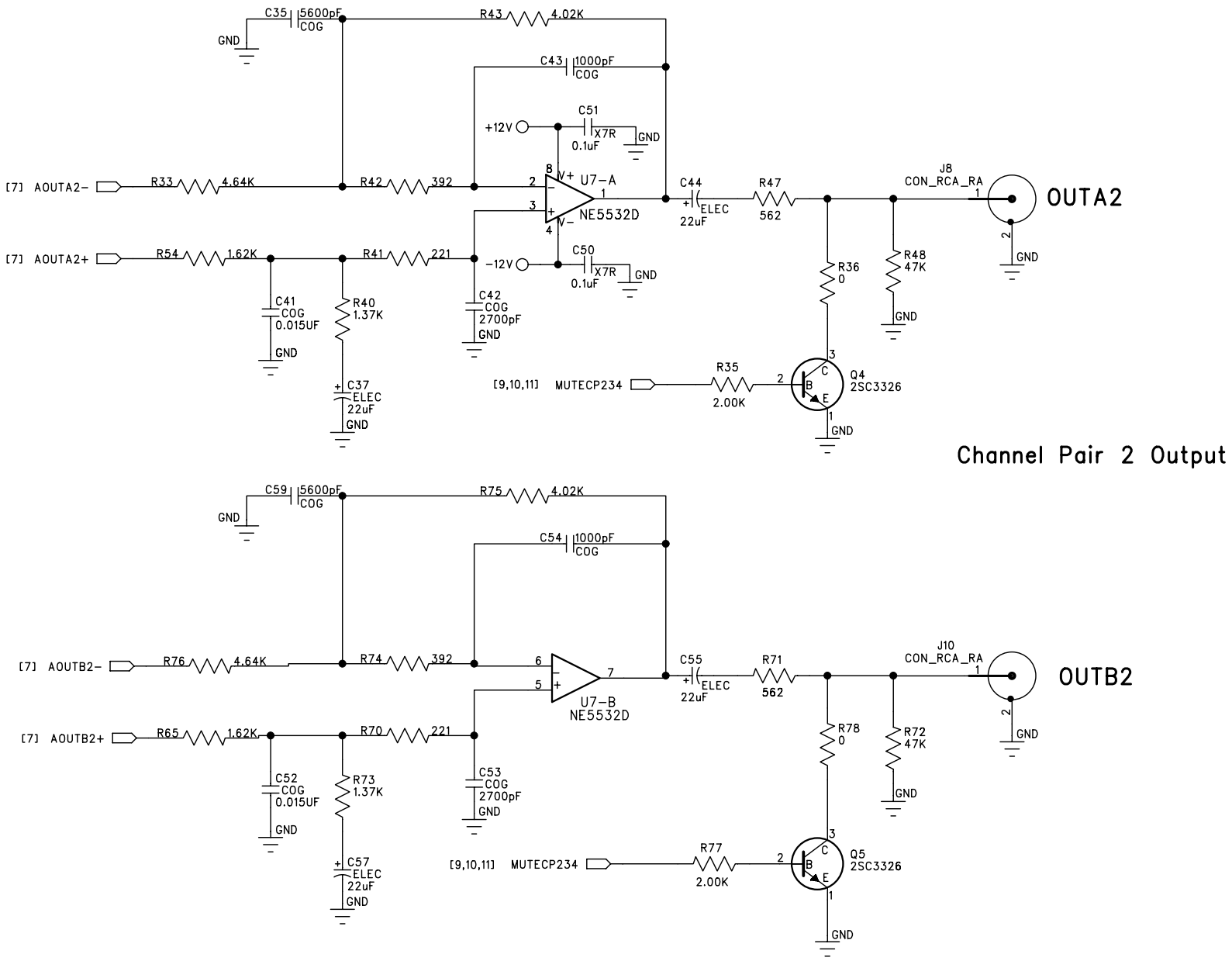


Figure 46. Analog Outputs A2 - B2

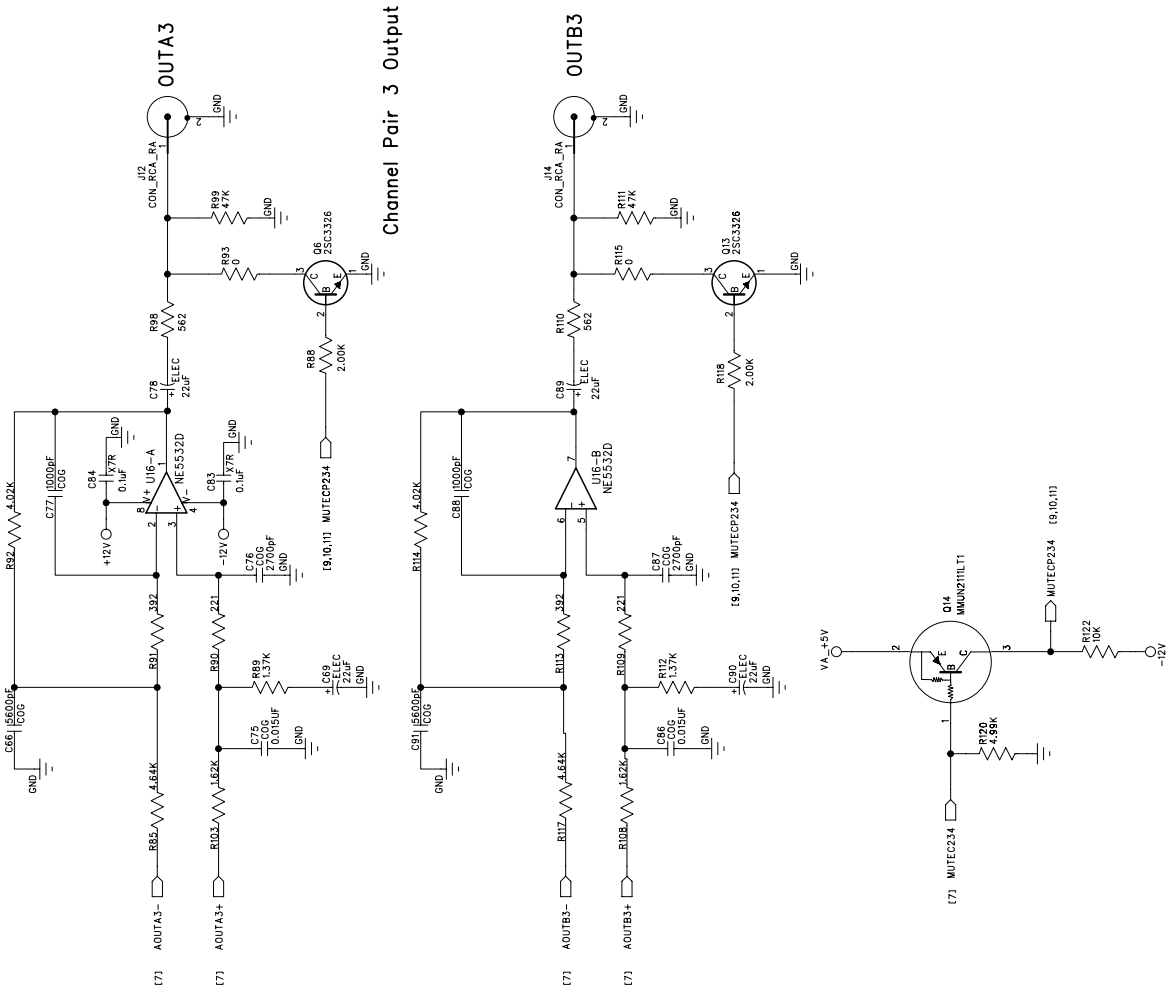


Figure 47. Analog Outputs A3 - B3

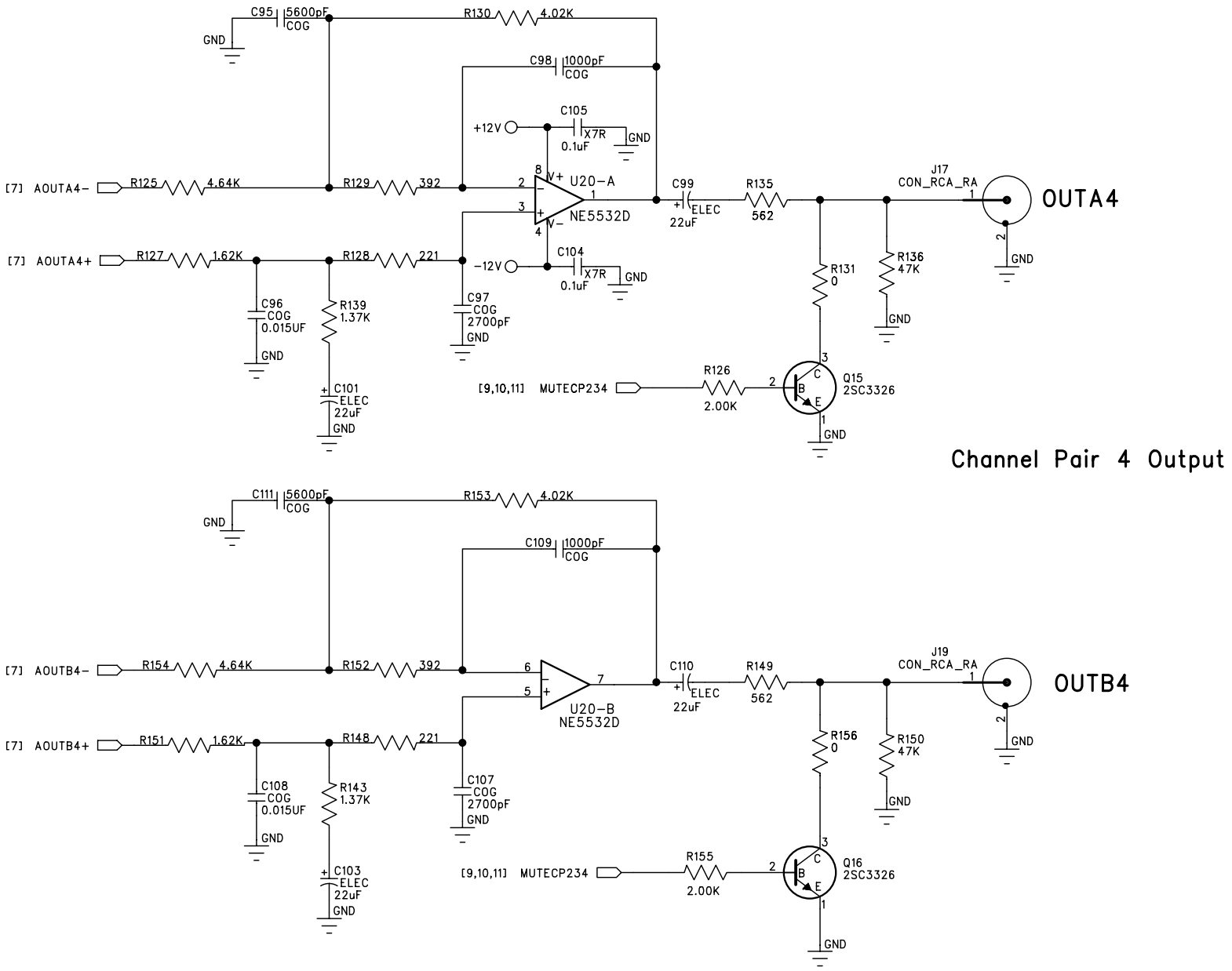


Figure 48. Analog Outputs A4 - B4

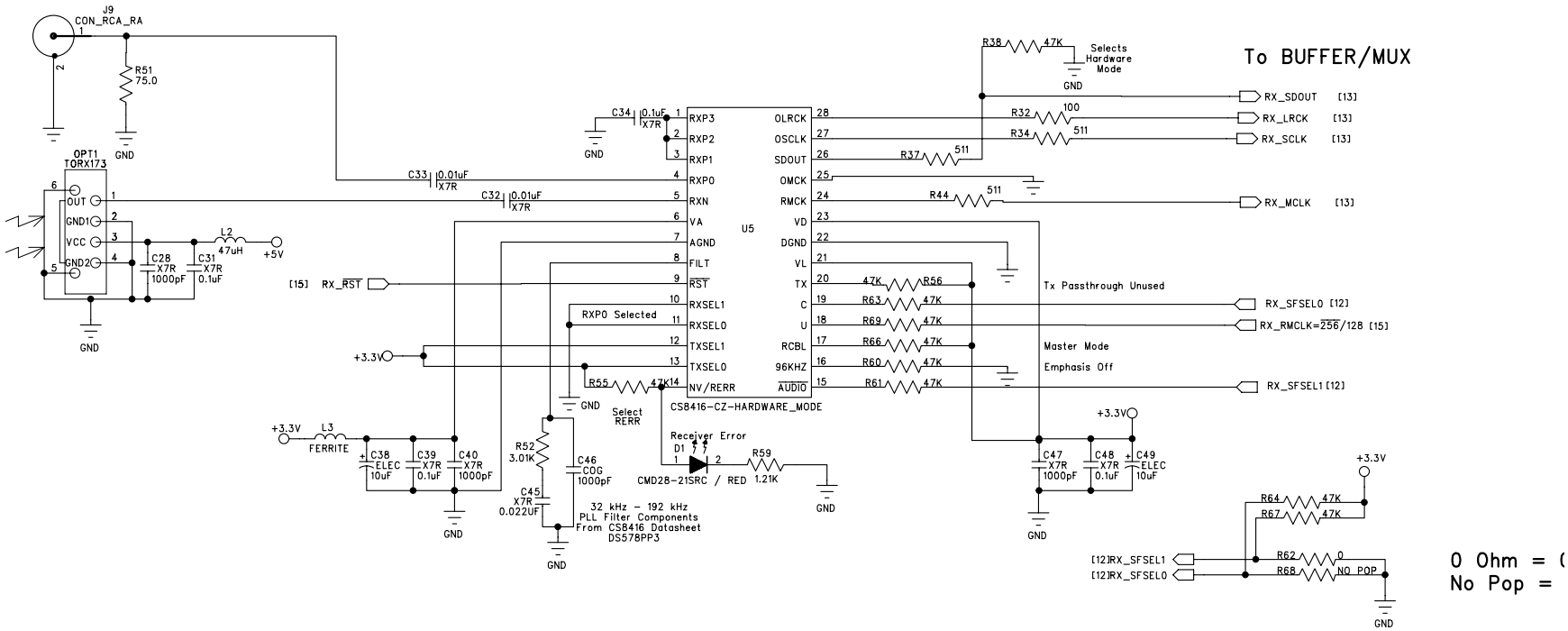


Figure 49. CS8416 S/PDIF Input

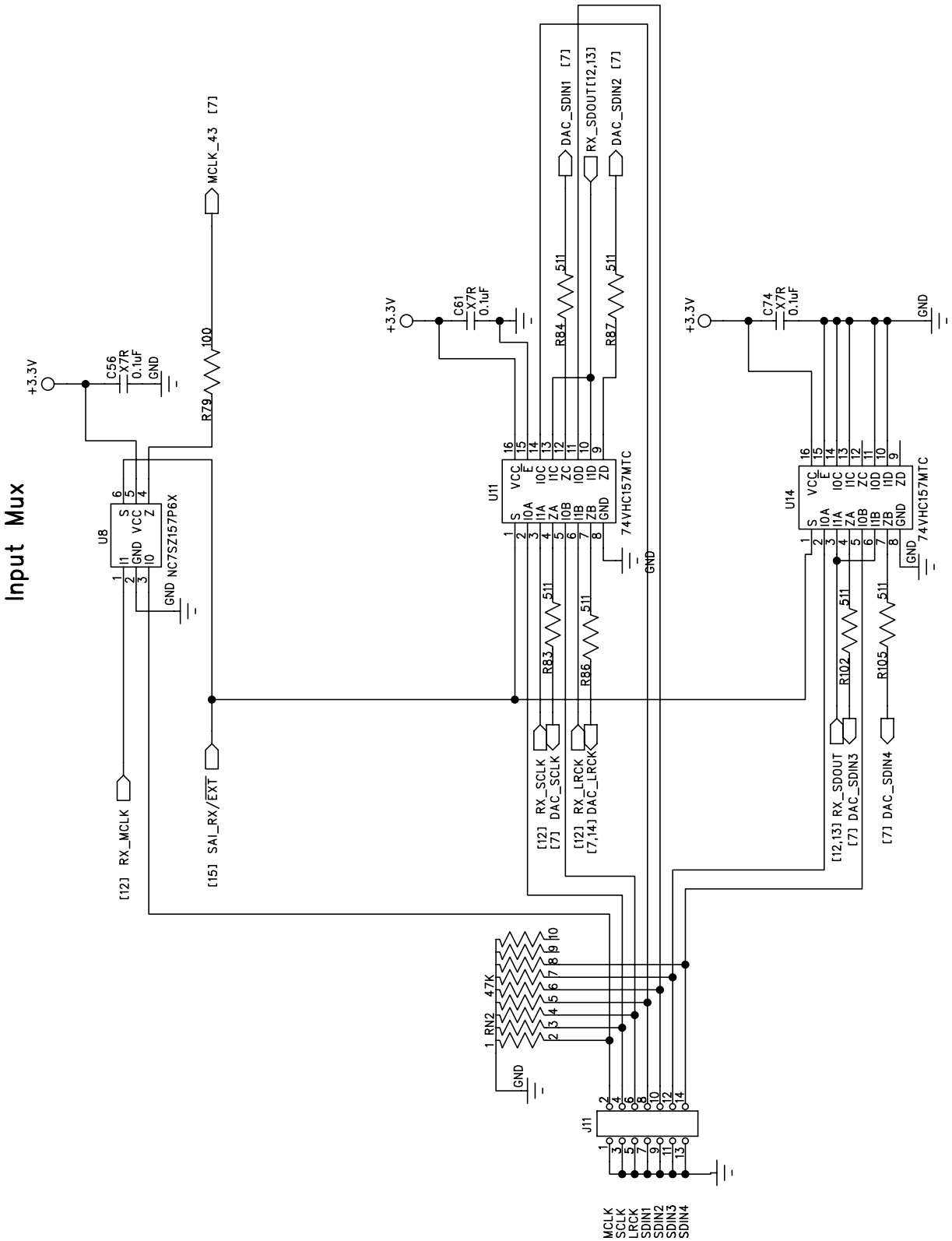
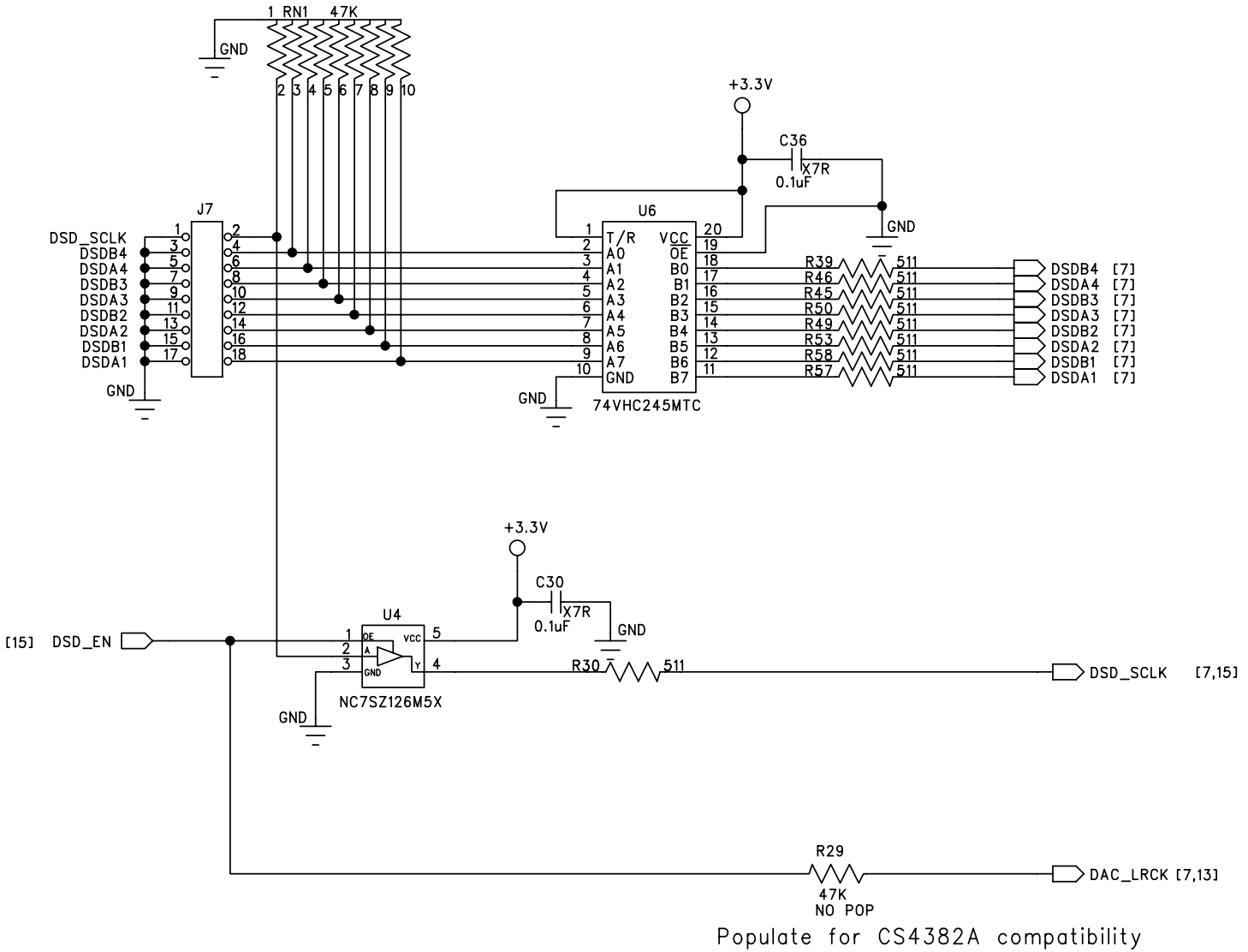


Figure 50. PCM Input Header and Muxing



DSD Input

Figure 51. DSD Input Header

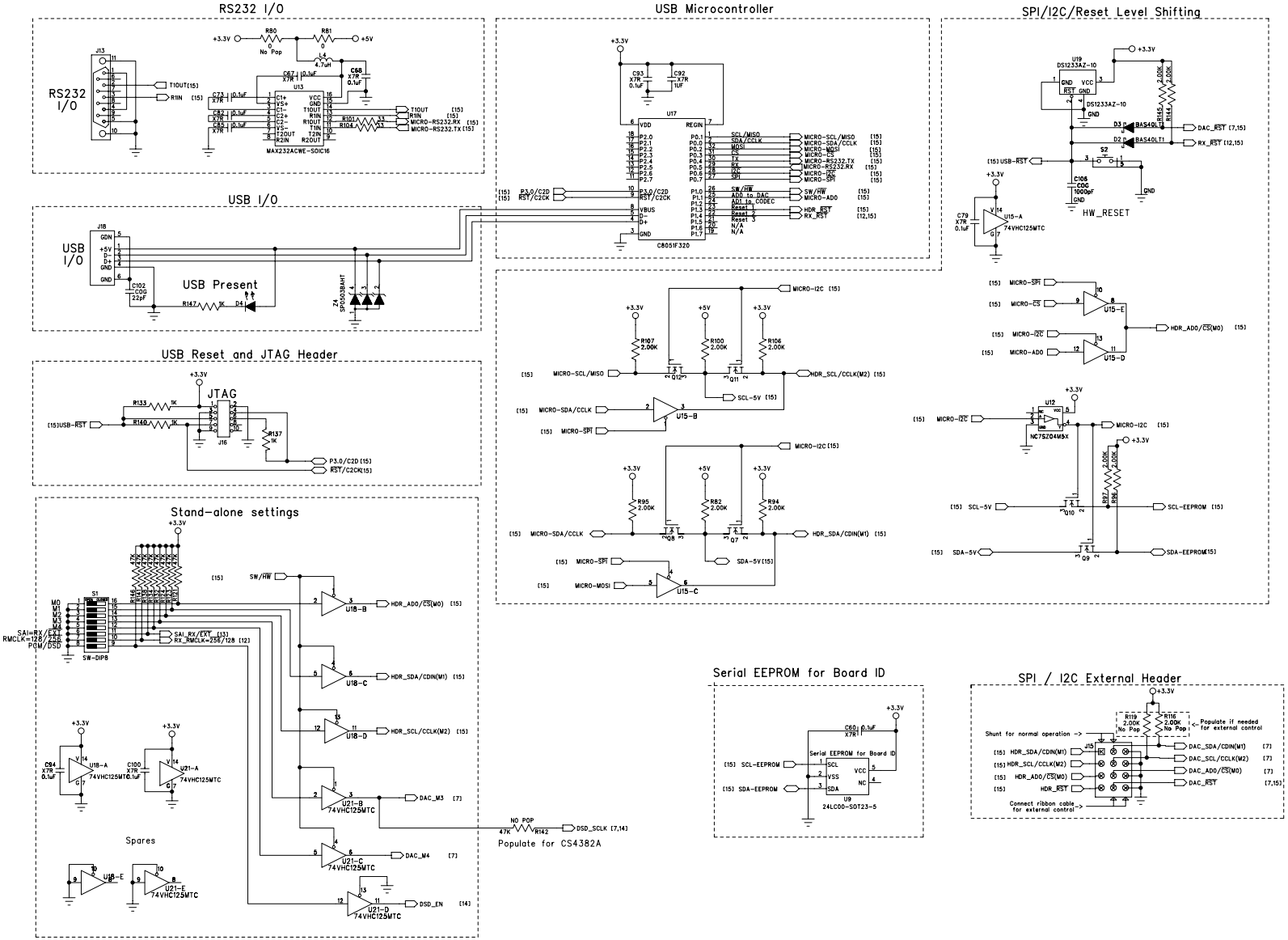


Figure 52. Control Input

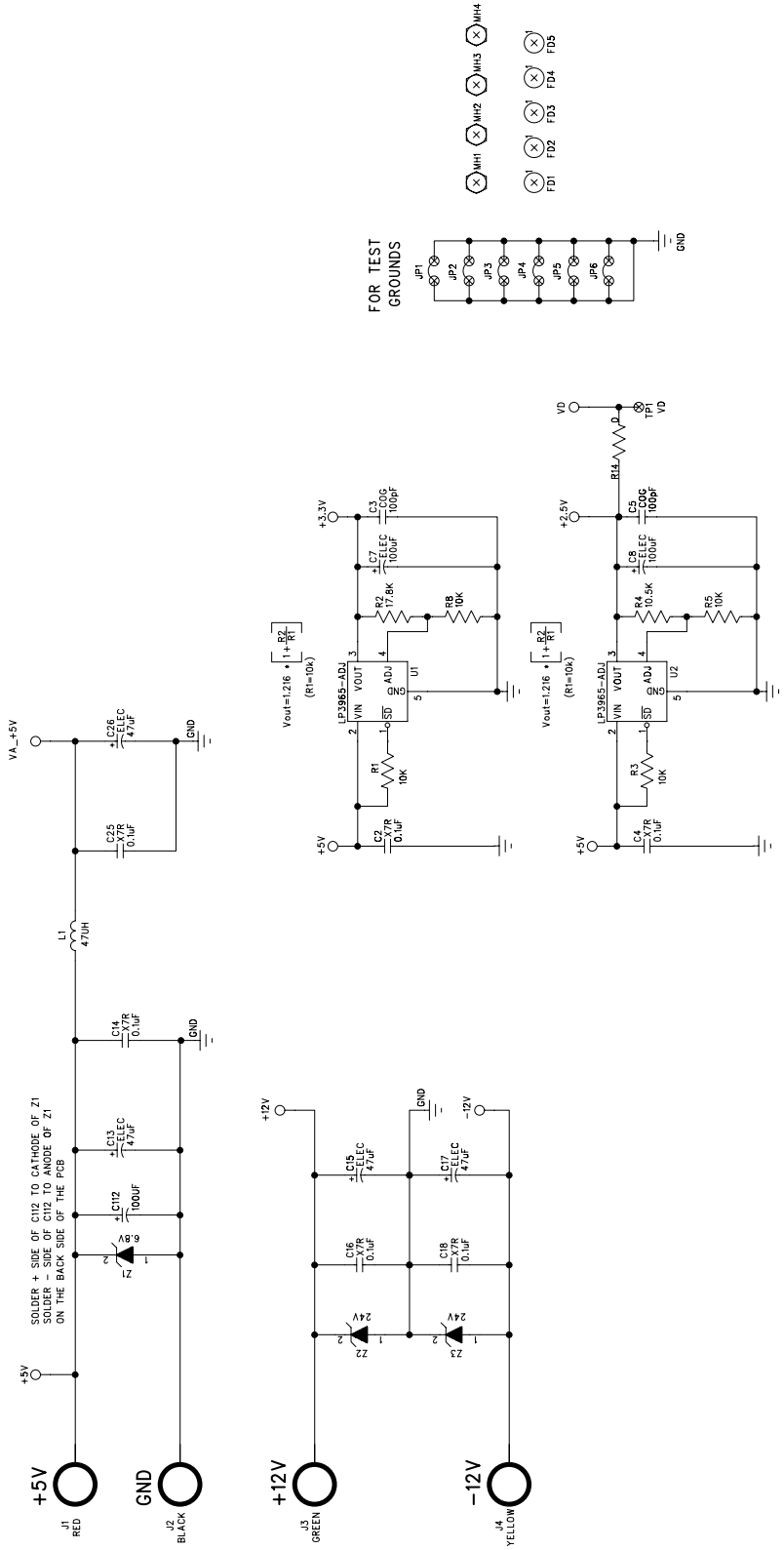
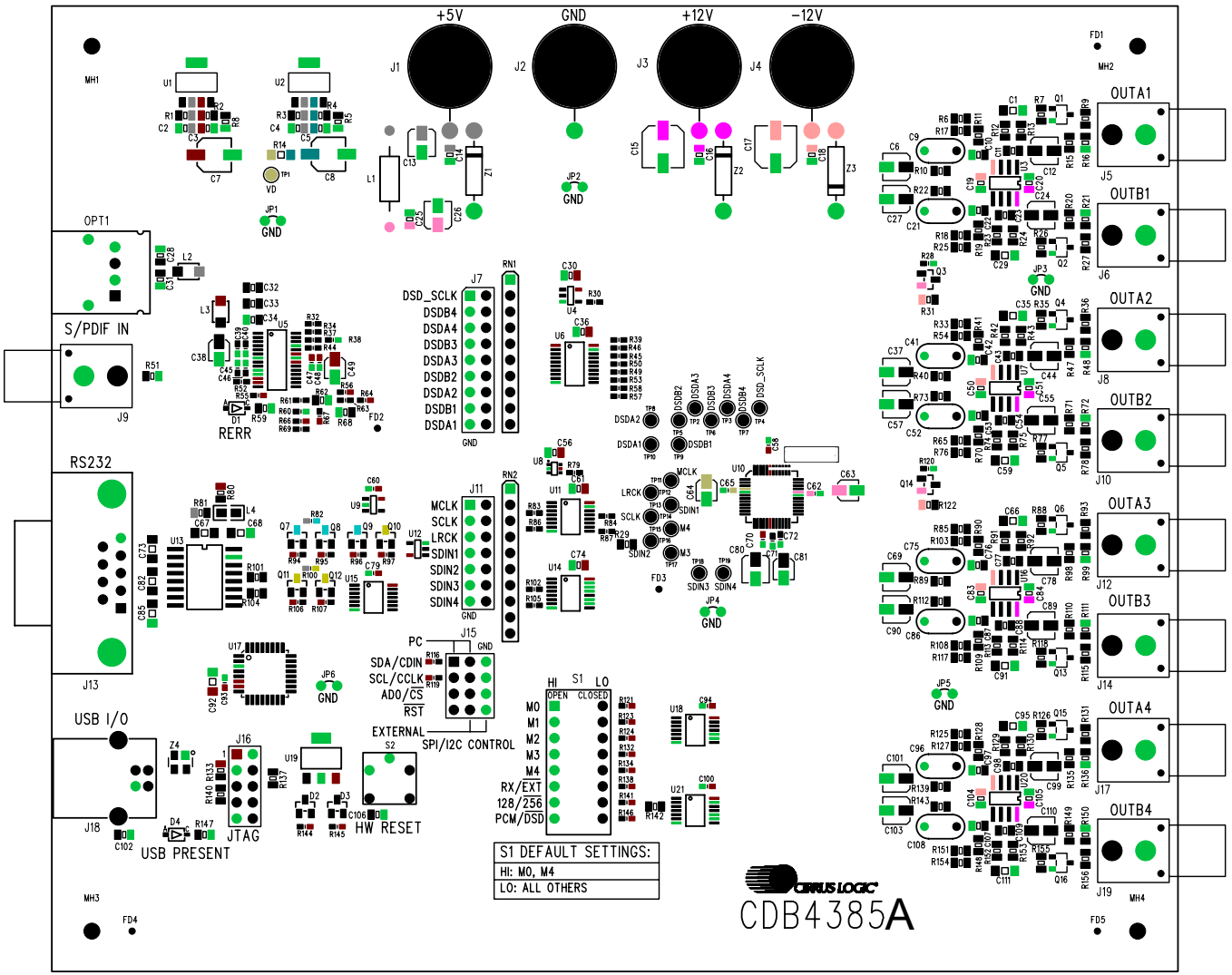


Figure 53. Power Inputs



CIRRUS LOGIC CDB4385A PCB 240-00123-01 Rev B

SILKSCREEN TOP

Figure 54. Silkscreen Top

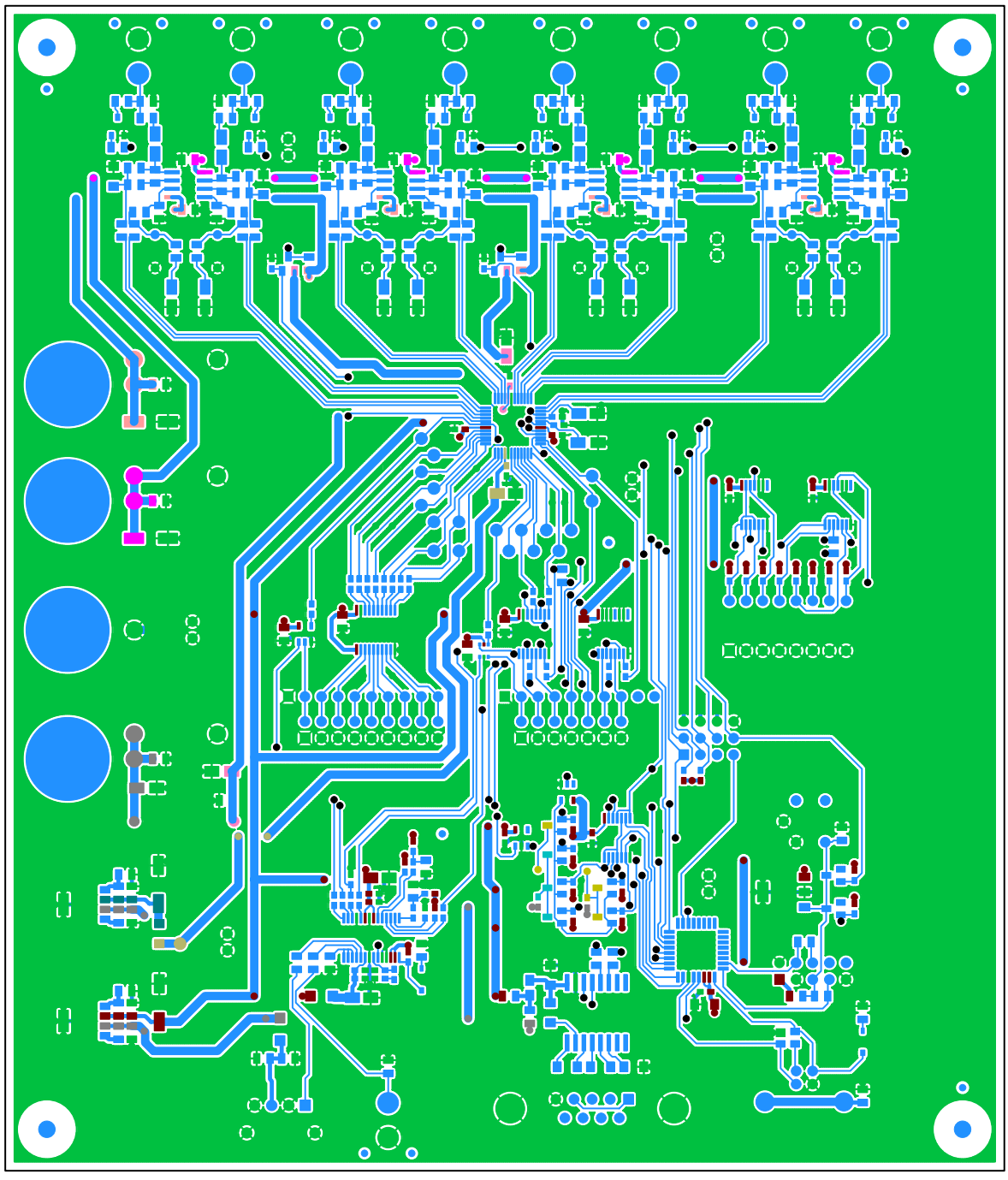


Figure 55. Top Side

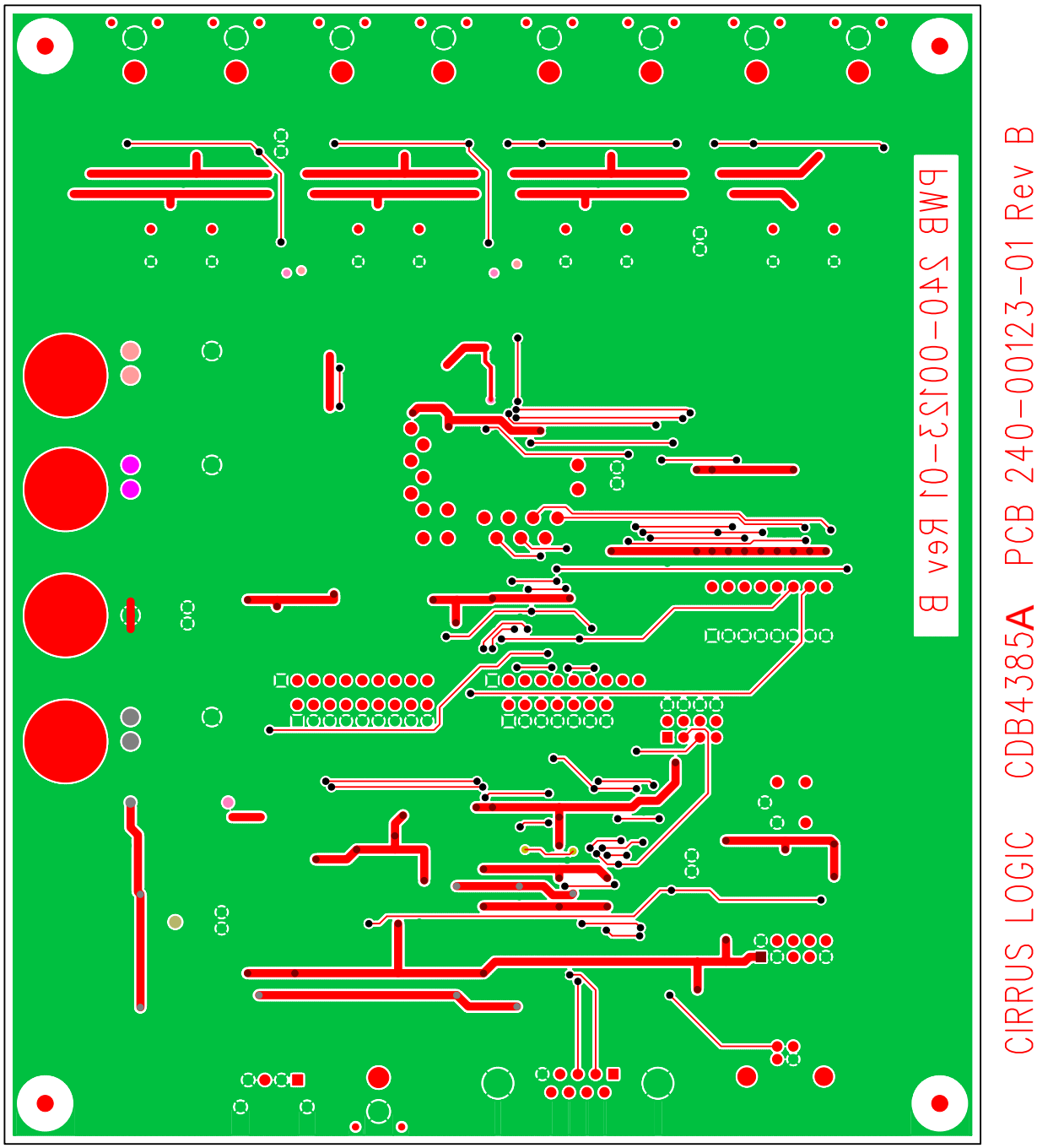


Figure 56. Bottom Side

10.REVISION HISTORY

Revision	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.

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