

## High-Speed CMOS Logic Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

### Features

- Buffered Inputs
- Common Three-State Output Enable Control
- Three-State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay (Clock to Q) = 15ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2-V to 6-V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5-V to 5.5-V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

### Ordering Information

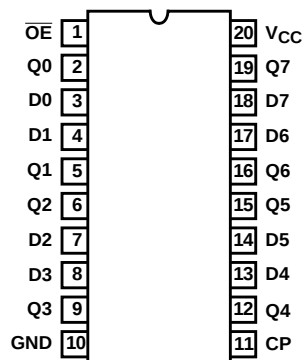
| PART NUMBER   | TEMP. RANGE<br>(°C) | PACKAGE      |
|---------------|---------------------|--------------|
| CD54HC374F3A  | -55 to 125          | 20 Ld Cerdip |
| CD54HC574F3A  | -55 to 125          | 20 Ld Cerdip |
| CD54HCT374F3A | -55 to 125          | 20 Ld Cerdip |
| CD54HCT574F3A | -55 to 125          | 20 Ld Cerdip |
| CD74HC374E    | -55 to 125          | 20 Ld PDIP   |
| CD74HC374M    | -55 to 125          | 20 Ld SOIC   |
| CD74HC374M96  | -55 to 125          | 20 Ld SOIC   |
| CD74HC574E    | -55 to 125          | 20 Ld PDIP   |
| CD74HC574M    | -55 to 125          | 20 Ld SOIC   |
| CD74HC574M96  | -55 to 125          | 20 Ld SOIC   |
| CD74HCT374E   | -55 to 125          | 20 Ld PDIP   |
| CD74HCT374M   | -55 to 125          | 20 Ld SOIC   |
| CD74HCT374M96 | -55 to 125          | 20 Ld SOIC   |
| CD74HCT574E   | -55 to 125          | 20 Ld PDIP   |
| CD74HCT574M   | -55 to 125          | 20 Ld SOIC   |
| CD74HCT574M96 | -55 to 125          | 20 Ld SOIC   |
| CD74HCT574PWR | -55 to 125          | 20 Ld TSSOP  |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel.

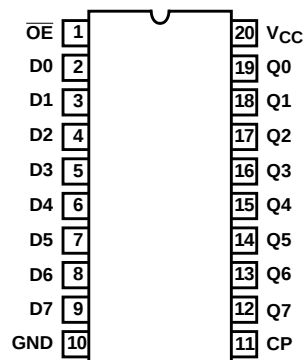
# CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574

## Pinouts

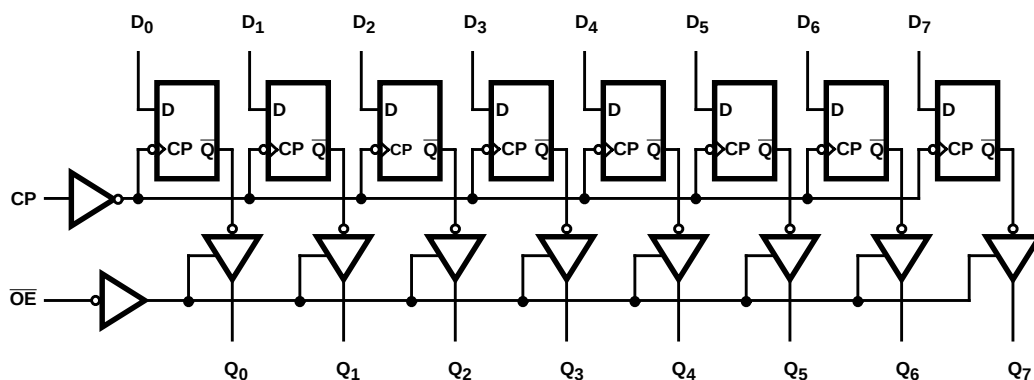
CD54HC374, CD54HCT374  
(CERDIP)  
CD74HC374, CD74HCT374  
(PDIP, SOIC)  
TOP VIEW



CD54HC574, CD54HCT574  
(CERDIP)  
CD74HC574  
(PDIP, SOIC)  
CD74HCT574  
(PDIP, SOIC, TSSOP)  
TOP VIEW



## Functional Diagram



TRUTH TABLE

| INPUTS |    |    | OUTPUT |
|--------|----|----|--------|
| OE     | CP | Dn | Qn     |
| L      | ↑  | H  | H      |
| L      | ↑  | L  | L      |
| L      | L  | X  | Q0     |
| H      | X  | X  | Z      |

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

↑ = Transition from Low to High Level

Q0 = The level of Q before the indicated steady-state input conditions were established

Z = High Impedance State

# CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574

## Absolute Maximum Ratings

|                                                        |             |
|--------------------------------------------------------|-------------|
| DC Supply Voltage, $V_{CC}$                            | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$                      | $\pm 35mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$             | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$                | $\pm 50mA$  |

## Thermal Information

|                                          |                                  |
|------------------------------------------|----------------------------------|
| Thermal Resistance (Typical, Note 1)     | $\theta_{JA}$ ( $^{\circ}C/W$ )  |
| E (PDIP) Package                         | 69                               |
| M (SOIC) Package                         | 58                               |
| PW (TSSOP) Package                       | 83                               |
| Maximum Junction Temperature             | $150^{\circ}C$                   |
| Maximum Storage Temperature Range        | $-65^{\circ}C$ to $150^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | $300^{\circ}C$                   |
| (SOIC - Lead Tips Only)                  |                                  |

## Operating Conditions

|                                           |                                  |
|-------------------------------------------|----------------------------------|
| Temperature Range, $T_A$                  | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$            |                                  |
| HC Types                                  | .2V to 6V                        |
| HCT Types                                 | .4.5V to 5.5V                    |
| DC Input or Output Voltage, $V_I$ , $V_O$ | 0V to $V_{CC}$                   |
| Input Rise and Fall Time                  |                                  |
| 2V                                        | 1000ns (Max)                     |
| 4.5V                                      | 500ns (Max)                      |
| 6V                                        | 400ns (Max)                      |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                    |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -                   | -                   | -    | -   | -    | -             | -    | -              | -    | V     |
|                                         |                 |                                    | -6                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                    | -7.8                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -                   | -                   | -    | -   | -    | -             | -    | -              | -    | V     |
|                                         |                 |                                    | 6                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                    | 7.8                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |

**CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574**

**DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                             | TEST CONDITIONS                         |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|------------------------------------|-----------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                                    | V <sub>I</sub> (V)                      | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| Quiescent Device Current                                       | I <sub>CC</sub>                    | V <sub>CC</sub> or GND                  | 0                   | 6                   | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Three- State Leakage Current                                   | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | -                   | 6                   | -    | -   | ±0.5 | -             | ±5.0 | -              | ±10 | μA    |
| <b>HCT TYPES</b>                                               |                                    |                                         |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>                    | -                                       | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>                    | -                                       | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>                    | V <sub>IH</sub> or V <sub>IL</sub>      | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                                    |                                         | -6                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>                    | V <sub>IH</sub> or V <sub>IL</sub>      | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                                    |                                         | 6                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>                     | V <sub>CC</sub> and GND                 | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>                    | V <sub>CC</sub> or GND                  | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Three- State Leakage Current                                   | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | -                   | 6                   | -    | -   | ±0.5 | -             | ±5.0 | -              | ±10 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2)          | V <sub>CC</sub> -2.1                    | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

- For dual-supply systems, theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT   | UNIT LOADS |        |
|---------|------------|--------|
|         | HCT374     | HCT574 |
| D0 - D7 | 0.3        | 0.4    |
| CP      | 0.9        | 0.75   |
| OE      | 1.3        | 0.6    |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specific in DC Electrical Specifications Table, e.g., 360μA max. at 25°C.

**CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574**

**Prerequisite for Switching Specifications**

| PARAMETER                | SYMBOL           | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     |     | -55°C TO 125°C |     |     | UNITS |
|--------------------------|------------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|
|                          |                  |                     | MIN  | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |       |
| HC TYPES                 |                  |                     |      |     |     |               |     |     |                |     |     |       |
| Maximum Clock Frequency  | f <sub>MAX</sub> | 2                   | 6    | -   | -   | 5             | -   | -   | 4              | -   | -   | MHz   |
|                          |                  | 4.5                 | 30   | -   | -   | 25            | -   | -   | 20             | -   | -   | MHz   |
|                          |                  | 6                   | 35   | -   | -   | 29            | -   | -   | 23             | -   | -   | MHz   |
| Clock Pulse Width        | t <sub>W</sub>   | 2                   | 80   | -   | -   | 100           | -   | -   | 120            | -   | -   | ns    |
|                          |                  | 4.5                 | 16   | -   | -   | 20            | -   | -   | 24             | -   | -   | ns    |
|                          |                  | 6                   | 14   | -   | -   | 17            | -   | -   | 20             | -   | -   | ns    |
| Setup Time Data to Clock | t <sub>SU</sub>  | 2                   | 60   | -   | -   | 75            | -   | -   | 90             | -   | -   | ns    |
|                          |                  | 4.5                 | 12   | -   | -   | 15            | -   | -   | 18             | -   | -   | ns    |
|                          |                  | 6                   | 10   | -   | -   | 13            | -   | -   | 15             | -   | -   | ns    |
| Hold Time Data to Clock  | t <sub>H</sub>   | 2                   | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
|                          |                  | 4.5                 | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
|                          |                  | 6                   | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
| HCT TYPES                |                  |                     |      |     |     |               |     |     |                |     |     |       |
| Maximum Clock Frequency  | f <sub>MAX</sub> | 4.5                 | 30   | -   | -   | 25            | -   | -   | 20             | -   | -   | MHz   |
| Clock Pulse Width        | t <sub>W</sub>   | 4.5                 | 16   | -   | -   | 20            | -   | -   | 24             | -   | -   | ns    |
| Setup Time Data to Clock | t <sub>SU</sub>  | 4.5                 | 12   | -   | -   | 15            | -   | -   | 18             | -   | -   | ns    |
| Hold Time Data to Clock  | t <sub>H</sub>   | 4.5                 | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |

**Switching Specifications** C<sub>L</sub> = 50pF, Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                            | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                      |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                             |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay<br>Clock to Output | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 165 | -             | 205 | -              | 250 | ns    |
|                                      |                                     |                       | 4.5                 | -    | -   | 33  | -             | 41  | -              | 50  | ns    |
|                                      |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 15  | -   | -             | -   | -              | -   | ns    |
|                                      |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 28  | -             | 35  | -              | 43  | ns    |
| Output Disable to Q                  | t <sub>PLZ</sub> , t <sub>PHZ</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 135 | -             | 170 | -              | 205 | ns    |
|                                      |                                     |                       | 4.5                 | -    | -   | 27  | -             | 34  | -              | 41  | ns    |
|                                      |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |
|                                      |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 23  | -             | 29  | -              | 35  | ns    |

**CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574**

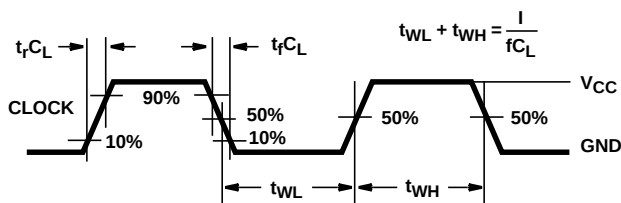
**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

| PARAMETER                                  | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------------------------|--------------------|---------------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                            |                    |                     |              | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Output Enable to Q                         | $t_{PZL}, t_{PZH}$ | $C_L = 50\text{pF}$ | 2            | -    | -   | 150 | -             | 190 | -              | 225 | ns    |
|                                            |                    |                     | 4.5          | -    | -   | 30  | -             | 38  | -              | 45  | ns    |
|                                            |                    | $C_L = 15\text{pF}$ | 5            | -    | 12  | -   | -             | -   | -              | -   | ns    |
|                                            |                    | $C_L = 50\text{pF}$ | 6            | -    | -   | 26  | -             | 33  | -              | 38  | ns    |
| Maximum Clock Frequency                    | $f_{MAX}$          | $C_L = 15\text{pF}$ | 5            | -    | 60  | -   | -             | -   | -              | -   | MHz   |
| Output Transition Time                     | $t_{THL}, t_{TLH}$ | $C_L = 50\text{pF}$ | 2            | -    | -   | 60  | -             | 75  | -              | 90  | ns    |
|                                            |                    |                     | 4.5          | -    | -   | 12  | -             | 15  | -              | 18  | ns    |
|                                            |                    |                     | 6            | -    | -   | 10  | -             | 13  | -              | 15  | ns    |
| Input Capacitance                          | $C_I$              | $C_L = 50\text{pF}$ | -            | 10   | -   | 10  | -             | 10  | -              | 10  | pF    |
| Three-State Output Capacitance             | $C_O$              | -                   | -            | 20   | -   | 20  | -             | 20  | -              | 20  | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5            | -    | 39  | -   | -             | -   | -              | -   | pF    |
| <b>HCT TYPES</b>                           |                    |                     |              |      |     |     |               |     |                |     |       |
| Propagation Delay<br>Clock to Output       | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 4.5          | -    | -   | 33  | -             | 41  | -              | 50  | ns    |
|                                            |                    | $C_L = 15\text{pF}$ | 5            | -    | 15  | -   | -             | -   | -              | -   | ns    |
| Output Disable to Q                        | $t_{PLZ}, t_{PHZ}$ | $C_L = 50\text{pF}$ | 4.5          | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
|                                            |                    | $C_L = 15\text{pF}$ | 5            | -    | 11  | -   | -             | -   | -              | -   | ns    |
| Output Enable to Q                         | $t_{PZL}, t_{PZH}$ | $C_L = 50\text{pF}$ | 4.5          | -    | -   | 30  | -             | 38  | -              | 45  | ns    |
|                                            |                    | $C_L = 15\text{pF}$ | 5            | -    | 12  | -   | -             | -   | -              | -   | ns    |
| Maximum Clock Frequency                    | $f_{MAX}$          | $C_L = 15\text{pF}$ | 5            | -    | 60  | -   | -             | -   | -              | -   | MHz   |
| Output Transition Time                     | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | -   | 12  | -             | 15  | -              | 18  | ns    |
| Input Capacitance                          | $C_I$              | $C_L = 50\text{pF}$ | -            | 10   | -   | 10  | -             | 10  | -              | 10  | pF    |
| Three-State Output Capacitance             | $C_O$              | -                   | -            | 20   | -   | 20  | -             | 20  | -              | 20  | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5            | -    | 47  | -   | -             | -   | -              | -   | pF    |

**NOTES:**

- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_O C_L$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

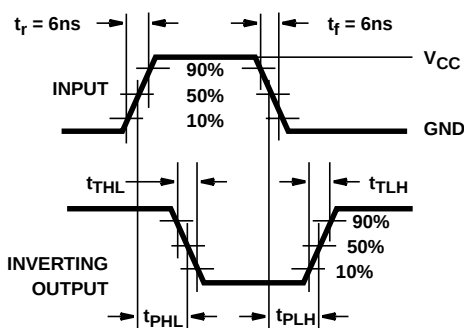


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS



FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

# Test Circuits and Waveforms (Continued)

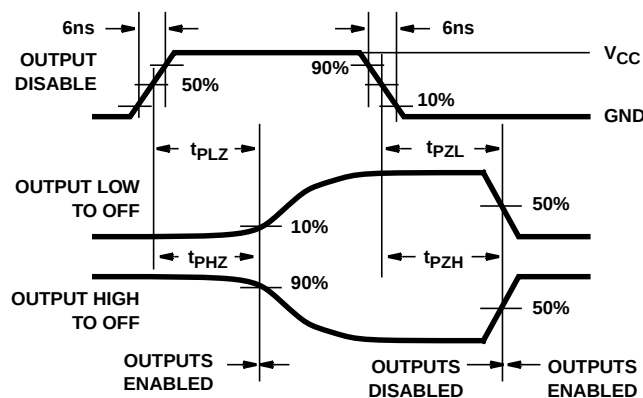


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

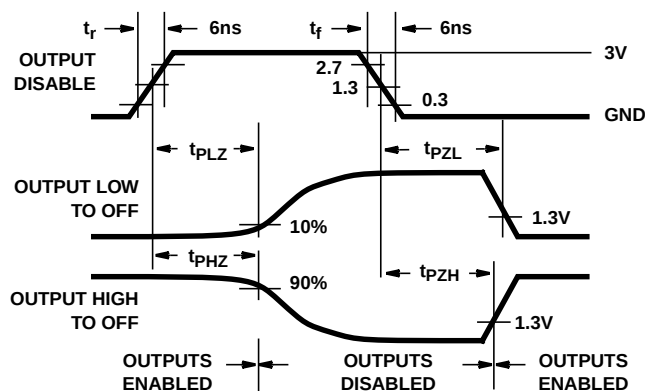


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)         | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 5962-8974201RA   | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8974201RA<br>CD54HCT574F3A | <a href="#">Samples</a> |
| CD54HC374F3A     | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8407101RA<br>CD54HC374F3A       | <a href="#">Samples</a> |
| CD54HC574F       | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | CD54HC574F                      | <a href="#">Samples</a> |
| CD54HC574F3A     | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | CD54HC574F3A                    | <a href="#">Samples</a> |
| CD54HCT374F3A    | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8550701RA<br>CD54HCT374F3A      | <a href="#">Samples</a> |
| CD54HCT574F      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | CD54HCT574F                     | <a href="#">Samples</a> |
| CD54HCT574F3A    | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8974201RA<br>CD54HCT574F3A | <a href="#">Samples</a> |
| CD74HC374E       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HC374E                      | <a href="#">Samples</a> |
| CD74HC374M       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC374M                          | <a href="#">Samples</a> |
| CD74HC374M96     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC374M                          | <a href="#">Samples</a> |
| CD74HC374M96E4   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC374M                          | <a href="#">Samples</a> |
| CD74HC574E       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HC574E                      | <a href="#">Samples</a> |
| CD74HC574M       | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC574M                          | <a href="#">Samples</a> |
| CD74HC574M96     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC574M                          | <a href="#">Samples</a> |
| CD74HC574M96E4   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC574M                          | <a href="#">Samples</a> |
| CD74HC574M96G4   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC574M                          | <a href="#">Samples</a> |
| CD74HCT374E      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT374E                     | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74HCT374EE4    | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT374E             | <a href="#">Samples</a> |
| CD74HCT374M      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT374M                 | <a href="#">Samples</a> |
| CD74HCT374M96    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT374M                 | <a href="#">Samples</a> |
| CD74HCT574E      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT574E             | <a href="#">Samples</a> |
| CD74HCT574M      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT574M                 | <a href="#">Samples</a> |
| CD74HCT574M96    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT574M                 | <a href="#">Samples</a> |
| CD74HCT574M96G4  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT574M                 | <a href="#">Samples</a> |
| CD74HCT574ME4    | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT574M                 | <a href="#">Samples</a> |
| CD74HCT574PWR    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HK574                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC374, CD54HC574, CD54HCT374, CD54HCT574, CD74HC374, CD74HC574, CD74HCT374, CD74HCT574 :**

- Catalog: [CD74HC374](#), [CD74HC574](#), [CD74HCT374](#), [CD74HCT574](#)
- Automotive: [CD74HCT574-Q1](#), [CD74HCT574-Q1](#)
- Enhanced Product: [CD74HCT574-EP](#), [CD74HCT574-EP](#)
- Military: [CD54HC374](#), [CD54HC574](#), [CD54HCT374](#), [CD54HCT574](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC374M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HC574M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT374M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT574M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HCT574PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC374M96  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| CD74HC574M96  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| CD74HCT374M96 | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| CD74HCT574M96 | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| CD74HCT574PWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



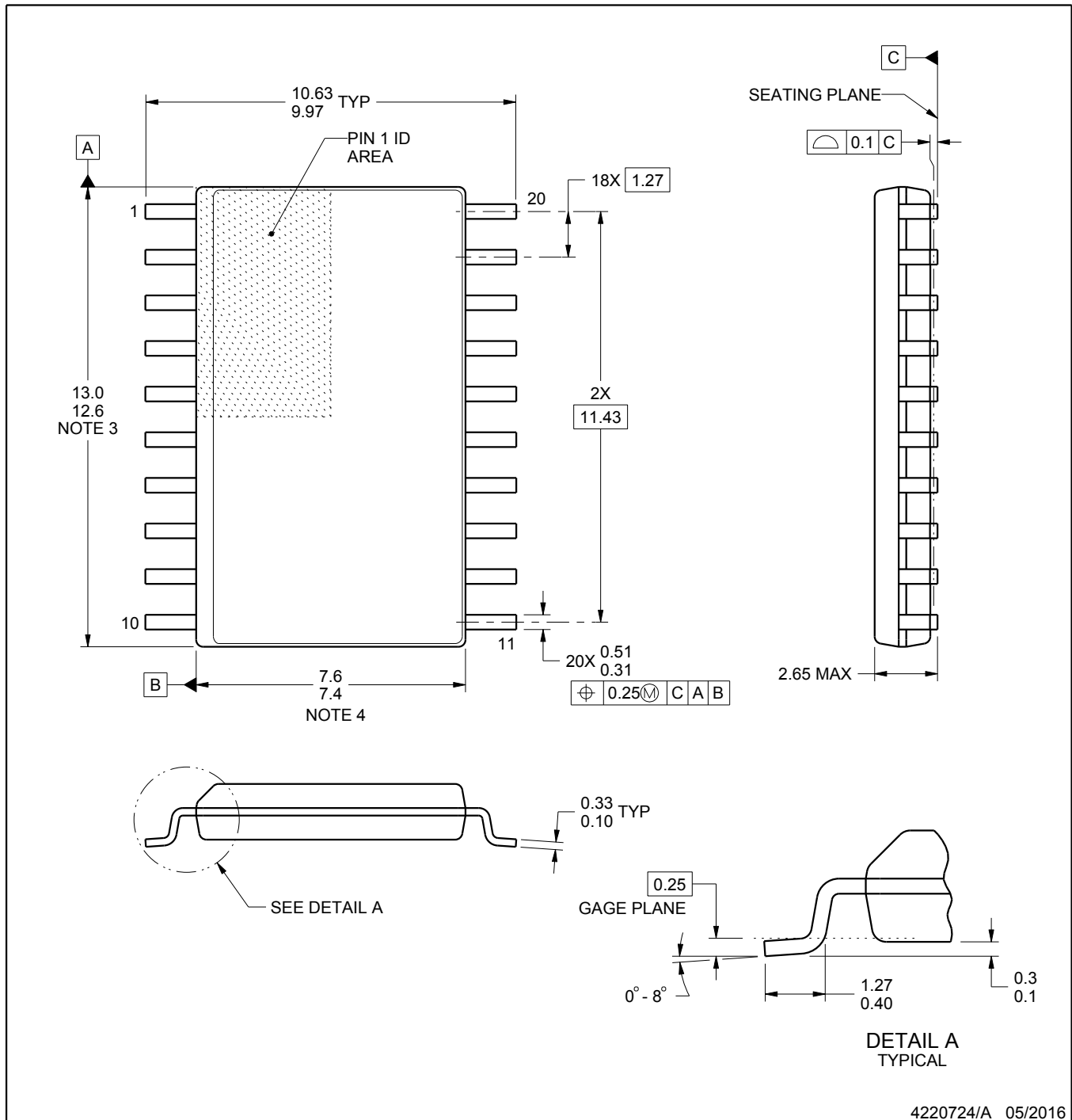
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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