# CD4095BMS
# CD4096BMS

## CMOS Gated J-K Master-Slave Flip-Flops

December 1992

### Features

- **Set-Reset Capability**
- **High Voltage Types (20V Rating)**
- **CD4095BMS Non-Inverting J and K Inputs**
- **CD4096BMS Inverting and Non-Inverting J and K Inputs**
- **16MHz Toggle Rate (Typ.) at VDD - VSS = 10V**
- **Gated Inputs**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Standardized Symmetrical Output Characteristics**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package/Temperature Range)**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

### Applications

- **Registers**
- **Counters**
- **Control Circuits**

### Description

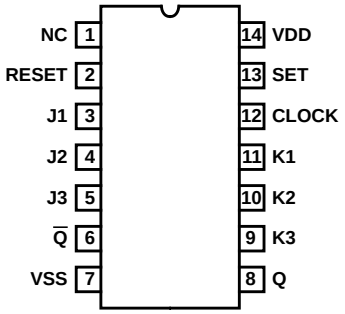
CD4095BMS and CD4096BMS are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095BMS and CD4096BMS are supplied in these 14 lead outline packages:

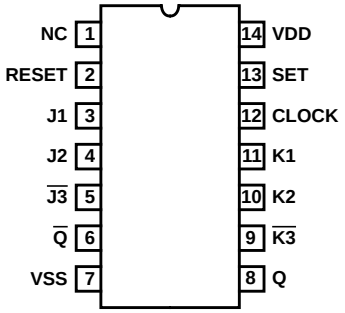
| | |
|---|---|
| Braze Seal DIP | H4Q |
| Frit Seal DIP | H1A |

### Pinouts

**CD4095BMS**
TOP VIEW



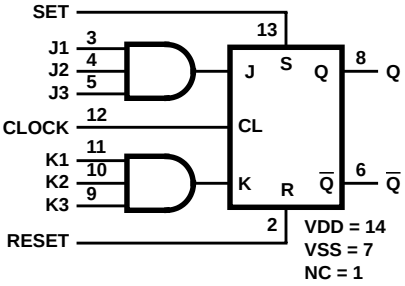

**CD4096BMS**
TOP VIEW



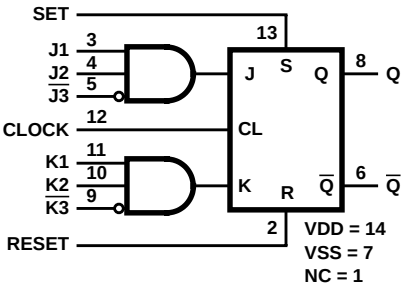

NC = NO CONNECTION

### Functional Diagrams

**CD4095BMS**




**CD4096BMS**




CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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## Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

## Reliability Information

| Thermal Resistance | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---|---|
| Ceramic DIP and FRIT Package | 80°C/W | 20°C/W |
| Flatpack Package | 70°C/W | 20°C/W |

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) . . . . . 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor . . . . . 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1) | | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | | 1 | +25°C | - | 2 | µA |
| | | | | 2 | +125°C | - | 200 | µA |
| | | VDD = 18V, VIN = VDD or GND | | 3 | -55°C | - | 2 | µA |
| Input Leakage Current | IIL | VIN = VDD or GND | VDD = 20 | 1 | +25°C | -100 | - | nA |
| | | | | 2 | +125°C | -1000 | - | nA |
| | | | VDD = 18V | 3 | -55°C | -100 | - | nA |
| Input Leakage Current | IIH | VIN = VDD or GND | VDD = 20 | 1 | +25°C | - | 100 | nA |
| | | | | 2 | +125°C | - | 1000 | nA |
| | | | VDD = 18V | 3 | -55°C | - | 100 | nA |
| Output Voltage | VOL15 | VDD = 15V, No Load | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH15 | VDD = 15V, No Load (Note 3) | | 1, 2, 3 | +25°C, +125°C, -55°C | 14.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | | 1 | +25°C | 0.53 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | | 1 | +25°C | 1.4 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | | 1 | +25°C | 3.5 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | | 1 | +25°C | - | -0.53 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | | 1 | +25°C | - | -1.8 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | | 1 | +25°C | - | -1.4 | mA |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | | 1 | +25°C | - | -3.5 | mA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10µA | | 1 | +25°C | -2.8 | -0.7 | V |
| P Threshold Voltage | VPTH | VSS = 0V, IDD = 10µA | | 1 | +25°C | 0.7 | 2.8 | V |
| Functional | F | VDD = 2.8V, VIN = VDD or GND | | 7 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 20V, VIN = VDD or GND | | 7 | +25°C | | | |
| | | VDD = 18V, VIN = VDD or GND | | 8A | +125°C | | | |
| | | VDD = 3V, VIN = VDD or GND | | 8B | -55°C | | | |
| Input Voltage Low (Note 2) | VIL | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 1.5 | V |
| Input Voltage High (Note 2) | VIH | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 3.5 | - | V |
| Input Voltage Low (Note 2) | VIL | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 4 | V |
| Input Voltage High (Note 2) | VIH | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 11 | - | V |

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1, 2) | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Propagation Delay Clock to Output | TPHL1 TPLH1 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 500 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 675 | ns |
| Propagation Delay Set or Reset to Output | TPHL2 TPLH2 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 300 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 405 | ns |
| Transition Time | TTHL TTLH | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 200 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 270 | ns |
| Maximum Clock Input Frequency | FCL | VDD = 5V, VIN = VDD or GND | 9 | +25°C | 3.5 | - | MHz |
| | | | 10, 11 | +125°C, -55°C | 2.59 | - | MHz |

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current | IDD | VDD = 5V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 1 | µA |
| | | | | +125°C | - | 30 | µA |
| | | VDD = 10V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 2 | µA |
| | | | | +125°C | - | 60 | µA |
| | | VDD = 15V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 2 | µA |
| | | | | +125°C | - | 120 | µA |
| Output Voltage | VOL | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOL | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | 4.95 | - | V |
| Output Voltage | VOH | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | 9.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | 1, 2 | +125°C | 0.36 | - | mA |
| | | | | -55°C | 0.64 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | 1, 2 | +125°C | 0.9 | - | mA |
| | | | | -55°C | 1.6 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | 1, 2 | +125°C | 2.4 | - | mA |
| | | | | -55°C | 4.2 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | 1, 2 | +125°C | - | -0.36 | mA |
| | | | | -55°C | - | -0.64 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | 1, 2 | +125°C | - | -1.15 | mA |
| | | | | -55°C | - | -2.0 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | 1, 2 | +125°C | - | -0.9 | mA |
| | | | | -55°C | - | -1.6 | mA |

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| Output Current (Source) | IOH15 | VDD =15V, VOUT = 13.5V | 1, 2 | +125°C | - | -2.4 | mA |
| | | | | -55°C | - | -4.2 | mA |
| Input Voltage Low | VIL | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | - | 3 | V |
| Input Voltage High | VIH | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | +7 | - | V |
| Propagation Delay Clock to Output | TPHL TPLH | VDD = 10V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 150 | ns |
| Propagation Delay Set or Reset to Output | TPHL TPLH | VDD = 10V | 1, 2, 3 | +25°C | - | 150 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |
| Transition Time | TTHL TTLH | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |
| Maximum Clock Input Frequency | FCL | VDD = 10V | 1, 2, 3 | +25°C | 8 | - | MHz |
| | | VDD = 15V | 1, 2, 3 | +25°C | 12 | - | MHz |
| Minimum Set or Reset Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 50 | ns |
| Minimum Data Setup Time | TS | VDD = 5V | 1, 2, 3 | +25°C | - | 400 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 160 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |
| Minimum Clock Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 140 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 60 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 40 | ns |
| Maximum Clock Input Rise or Fall Time | TRCL TFCL | VDD = 5V | 1, 2, 3 | +25°C | - | 15 | µs |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 5 | µs |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 5 | µs |
| Input Capacitance | CIN | Any Input | 1, 2 | +25°C | - | 7.5 | pF |

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | 1, 4 | +25°C | - | 7.5 | µA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10µA | 1, 4 | +25°C | -2.8 | -0.2 | V |

**TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| N Threshold Voltage Delta | ΔVTN | VDD = 10V, ISS = -10μA | 1, 4 | +25°C | - | ±1 | V |
| P Threshold Voltage | VTP | VSS = 0V, IDD = 10μA | 1, 4 | +25°C | 0.2 | 2.8 | V |
| P Threshold Voltage Delta | ΔVTP | VSS = 0V, IDD = 10μA | 1, 4 | +25°C | - | ±1 | V |
| Functional | F | VDD = 18V, VIN = VDD or GND | 1 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 3V, VIN = VDD or GND | | | | | |
| Propagation Delay Time | TPHL TPLH | VDD = 5V | 1, 2, 3, 4 | +25°C | - | 1.35 x +25°C Limit | ns |

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

**TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C**

| PARAMETER | SYMBOL | DELTA LIMIT |
|---|---|---|
| Supply Current - MSI-1 | IDD | ± 0.2μA |
| Output Current (Sink) | IOL5 | ± 20% x Pre-Test Reading |
| Output Current (Source) | IOH5A | ± 20% x Pre-Test Reading |

**TABLE 6. APPLICABLE SUBGROUPS**

| CONFORMANCE GROUP | | MIL-STD-883 METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|---|---|---|---|---|
| Initial Test (Pre Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 1 (Post Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 2 (Post Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | | 100% 5004 | 1, 7, 9, Deltas | |
| Interim Test 3 (Post Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | | 100% 5004 | 1, 7, 9, Deltas | |
| Final Test | | 100% 5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A | | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | Sample 5005 | 1, 7, 9 | |
| Group D | | Sample 5005 | 1, 2, 3, 8A, 8B, 9 | Subgroups 1, 2 3 |

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

**TABLE 7. TOTAL DOSE IRRADIATION**

| CONFORMANCE GROUPS | MIL-STD-883 METHOD | TEST | | READ AND RECORD | |
|---|---|---|---|---|---|
| | | PRE-IRRAD | POST-IRRAD | PRE-IRRAD | POST-IRRAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 |

**TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS**

| FUNCTION | OPEN | GROUND | VDD | 9V ± -0.5V | OSCILLATOR | |
|---|---|---|---|---|---|---|
| | | | | | 50kHz | 25kHz |
| CD4095BMS | | | | | | |
| Static Burn-In 1 Note 1 | 1, 6, 8 | 2-5, 7, 9-13 | 14 | | | |
| Static Burn-In 2 Note 1 | 1, 6, 8 | 7 | 2-5, 9-14 | | | |
| Dynamic Burn-In Note 1 | 1 | 2, 7, 13 | 3-5, 9-11, 14 | 6, 8 | - | 12 |
| Irradiation Note 2 | 1, 6, 8 | 7 | 2-5, 9-14 | | | |
| CD4096BMS | | | | | | |
| Static Burn-In 1 Note 1 | 1, 6, 8 | 2-5, 7, 9-13 | 14 | | | |
| Static Burn-In 2 Note 1 | 1, 6, 8 | 7 | 2-5, 9-14 | | | |
| Dynamic Burn-In Note 1 | 1 | 2, 5, 7, 9, 13 | 3, 4, 10, 11, 14 | 6, 8 | 12 | |
| Irradiation Note 2 | 1, 6, 8 | 7 | 2-5, 9-14 | | | |

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

## Logic Diagram

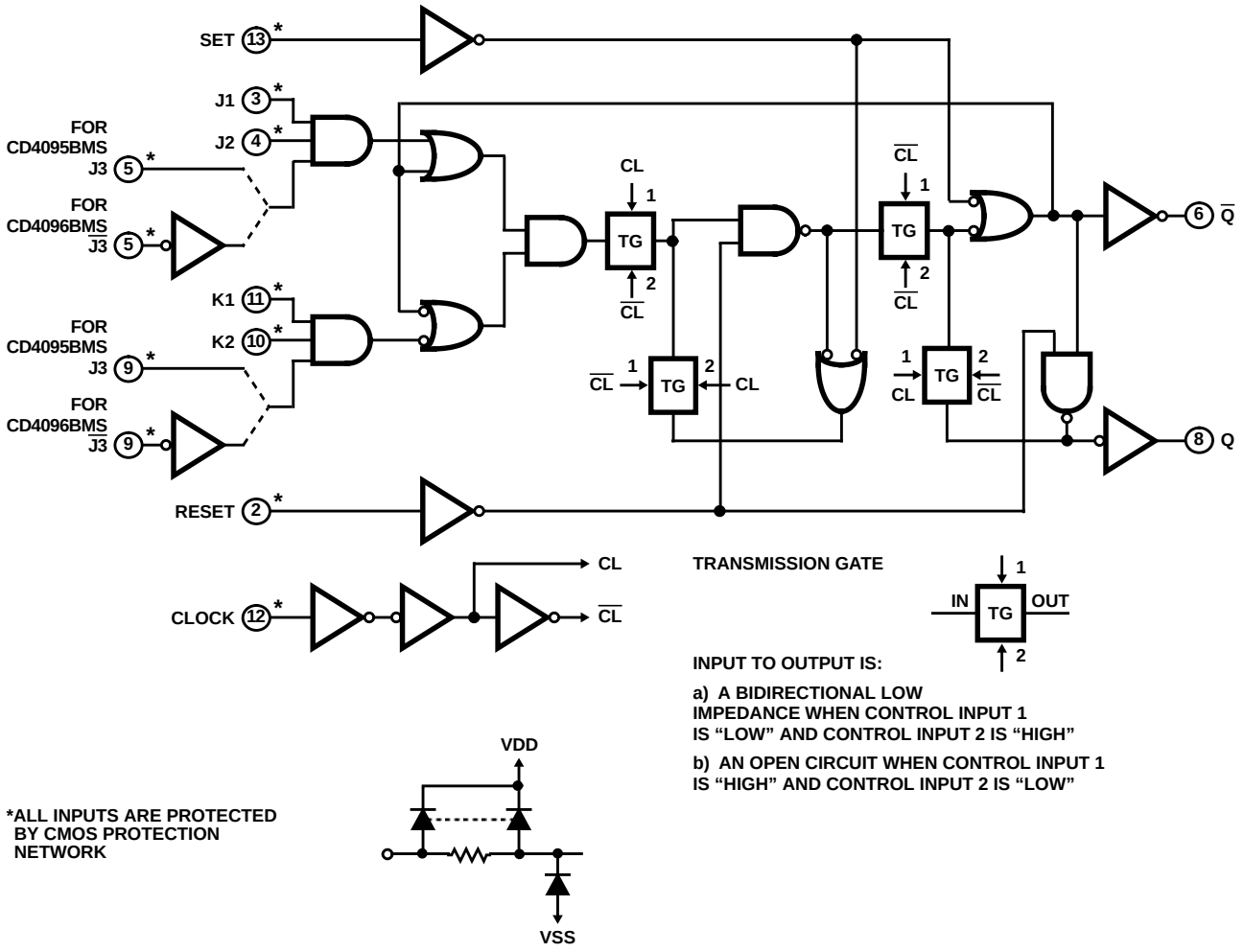



**FIGURE 1. CD4095BMS AND CD4096BMS LOGIC DIAGRAM**

**TRUTH TABLES**

| SYNCHRONOUS OPERATION (S = 0, R = 0) | | | | ASYNCHRONOUS OPERATION (J AND K = Don't Care) | | | |
|---|---|---|---|---|---|---|---|
| INPUTS BEFORE POSITIVE CLOCK TRANSITION | | OUTPUTS AFTER POSITIVE CLOCK TRANSITION | | INPUTS BEFORE POSITIVE CLOCK TRANSITION | | OUTPUTS AFTER POSITIVE CLOCK TRANSITION | |
| J* | K* | Q | $\overline{Q}$ | S | R | Q | $\overline{Q}$ |
| 0 | 0 | No Change | No Change | 0 | 0 | No Change | No Change |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | Toggles | Toggles | 1 | 1 | 0 | 0 |

* For CD4095BMS
J = J1 • J2 • J3
K = K1 • K2 • K3

For CD4096BMS
J = J1 • J2 • $\overline{J3}$
K = K1 • K2 • $\overline{K3}$

0 = VSS, 1 = VDD

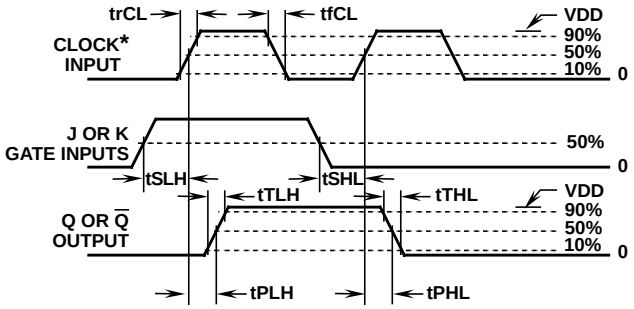



FIGURE 2. PROPAGATION DELAY, TRANSITION, AND SETUP TIME WAVEFORMS

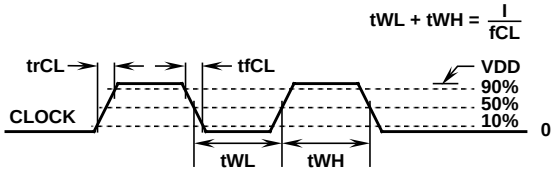



FIGURE 3. CLOCK PULSE RISE AND FALL TIME WAVEFORMS

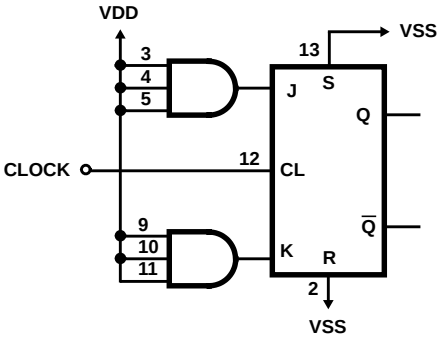



FIGURE 4. CD4095BMS CONNECTED IN TOGGLE MODE

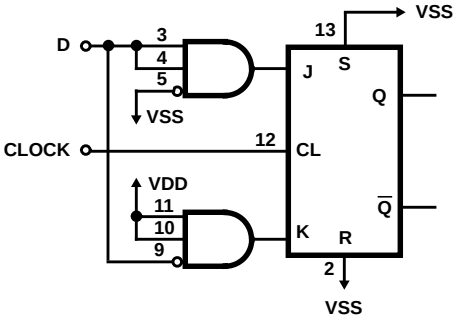
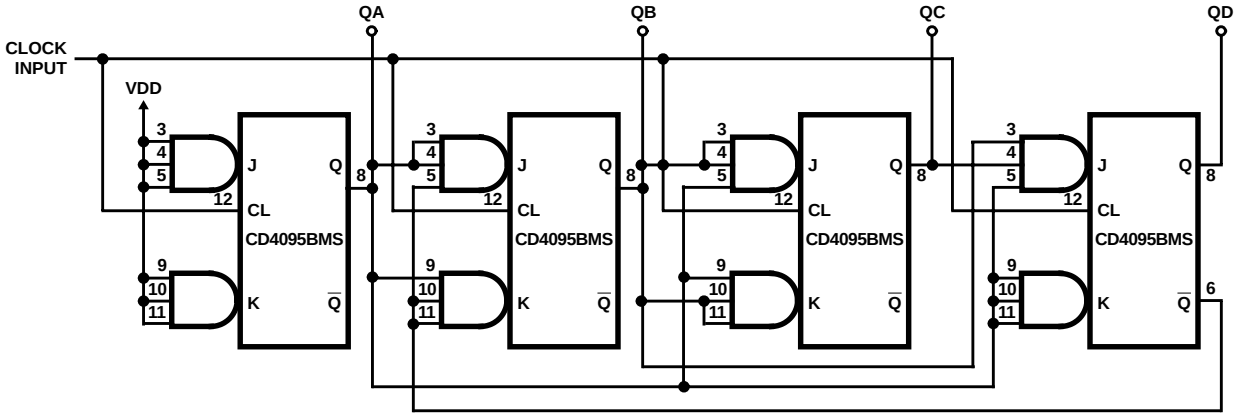
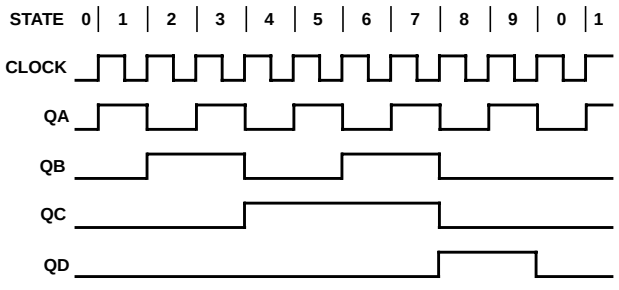



FIGURE 5. CD4096BMS CONNECTED AS A "D" TYPE FLIP-FLOP




| STATE | QA | QB | QC | QD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |

NOTE:
PINS 2 & 13 RESET & SET, GO TO VSS ON ALL UNITS

FIGURE 6. SYNCHRONOUS BINARY DIVIDE-BY-TEN COUNTER

## Typical Performance Characteristics

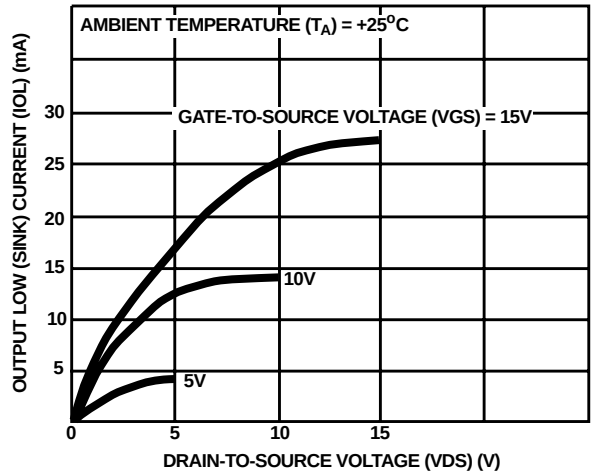



FIGURE 7. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

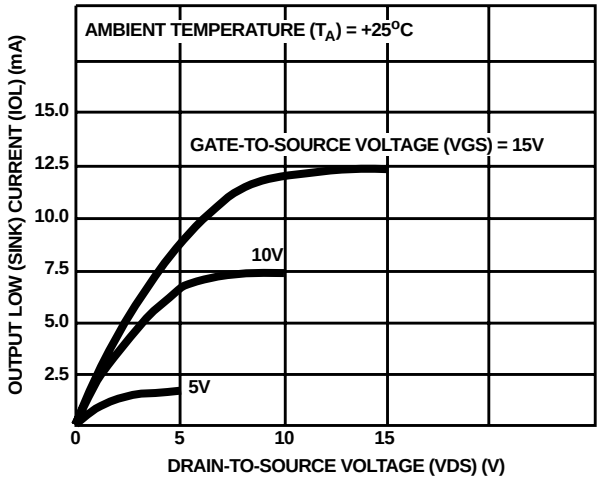



FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

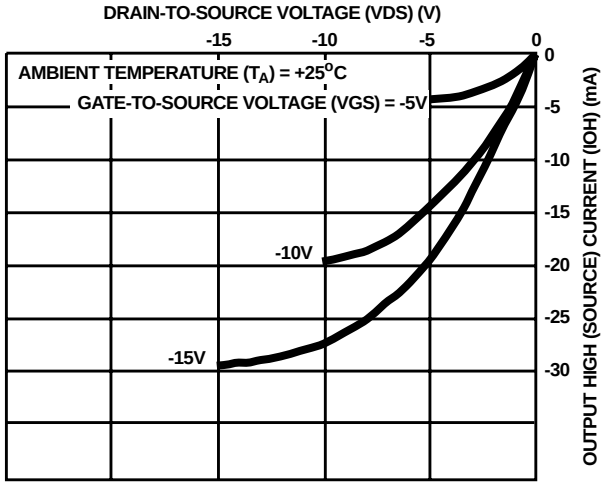



FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

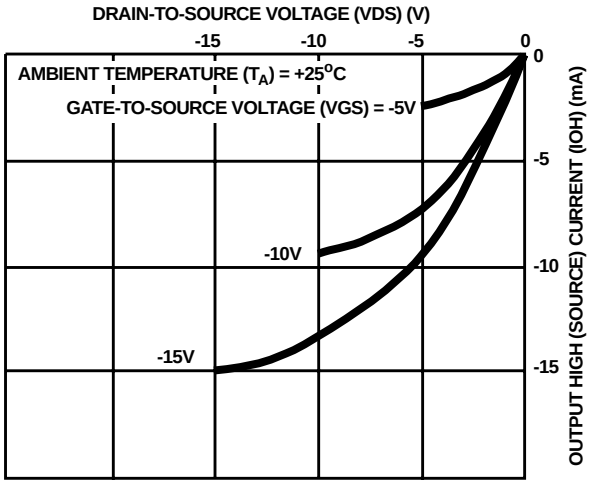



FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

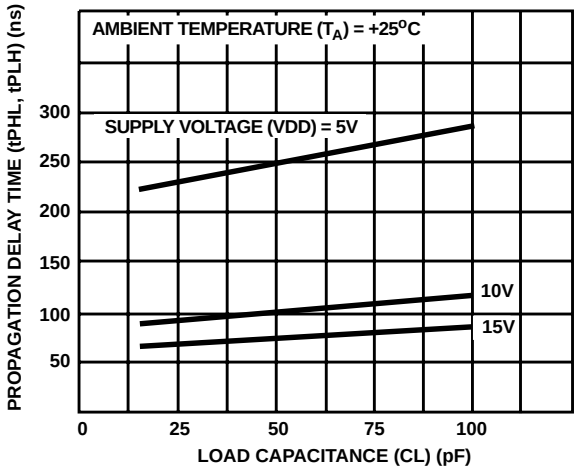



FIGURE 11. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

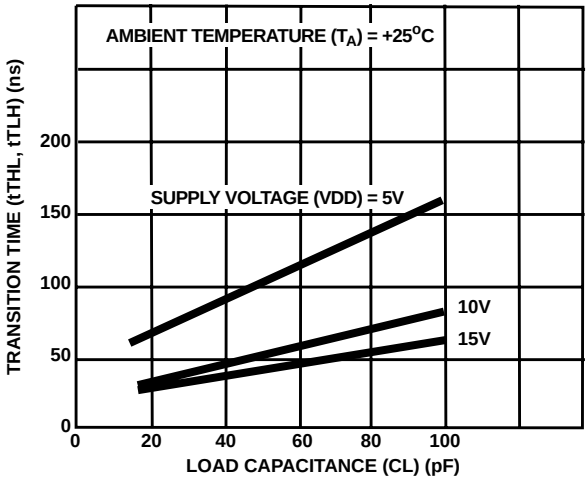



FIGURE 12. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

## Typical Performance Characteristics (Continued)

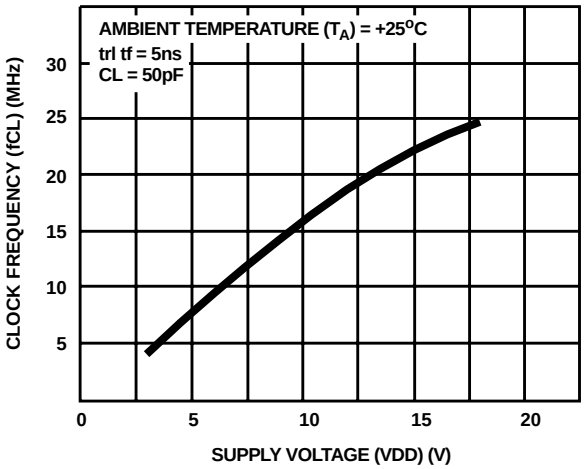



FIGURE 13. TYPICAL CLOCK FREQUENCY vs SUPPLY VOLTAGE (TOGGLE MODE - SEE FIGURE 4)

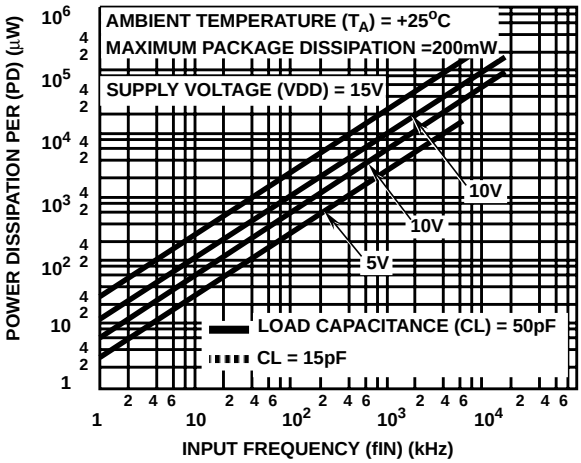
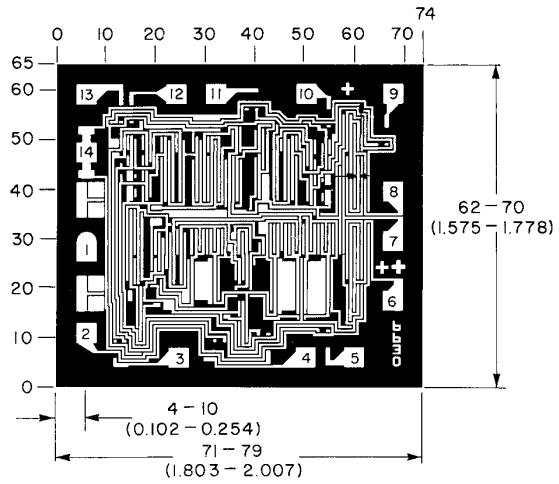
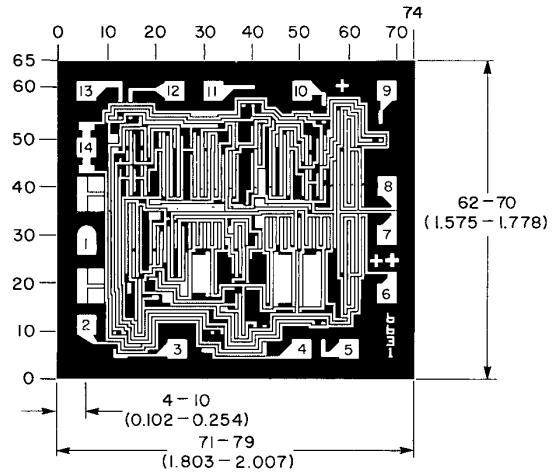



FIGURE 14. TYPICAL POWER DISSIPATION vs INPUT CLOCK FREQUENCY

## Chip Dimensions and Pad Layouts




CD4095BHMS




CD4096BHMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).

**METALLIZATION:** Thickness: 11kÅ – 14kÅ, AL.

**PASSIVATION:** 10.4kÅ - 15.6kÅ, Silane

**BOND PADS:** 0.004 inches X 0.004 inches MIN

**DIE THICKNESS:** 0.0198 inches - 0.0218 inches

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