

## **CC400**

# Single Chip High Performance RF Transceiver

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## Applications

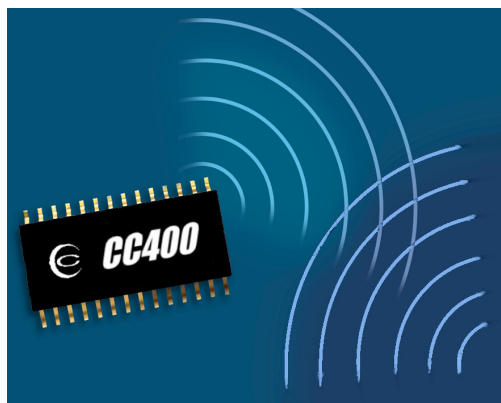
- *UHF wireless data transmitters and receivers*
- *Wireless alarm and security systems*
- *315 / 426 / 429 / 433 MHz ISM/SRD band systems*
- *Point of sale terminals*
- *Remote control systems*
- *Home security and automation*
- *Low power telemetry*
- *AMR – Automatic Meter Reading*
- *Environmental control*

## Product Description

**CC400** is a single-chip high performance, half-duplex, FSK, UHF transceiver designed for low power and low-voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) frequency bands at 315, 418 and 433 MHz, but can easily be programmed for operation at other frequency bands in the 300 - 500 MHz range.

The main operating parameters of **CC400** can be programmed via a serial interface, thus making **CC400** a very flexible and easy to use component. In a typical system **CC400** will be used together with a microcontroller and a few external passive components.

**CC400** is based on Chipcon's SmartRF® technology.



## Features

- Single chip RF transceiver
- Frequency range 300 – 500 MHz
- High sensitivity (typical -110 dBm)
- Programmable output power up to 25 mW (14 dBm)
- Small size (SSOP-28 package)
- Low supply voltage (2.7 V to 3.3 V)
- Very few external components required
- FSK modulation
- Very low phase noise
- Data-rate up to 9.6 kbps
- Suitable for both narrow and wide band systems
- Suitable for frequency hopping protocols
- Frequency-Lock indicator
- Development kit available
- Easy-to-use software (SmartRF Studio) for generating the **CC400** configuration data

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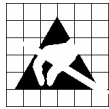
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## 1. Absolute Maximum Ratings

The absolute maximum ratings given in Table 1 must under no circumstances be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

| Parameter                 | Min. | Max.                | Units | Condition |
|---------------------------|------|---------------------|-------|-----------|
| Supply voltage, VDD       | -0.3 | 7.0                 | V     |           |
| Voltage on any pin        | -0.3 | VDD+0.3,<br>max 7.0 | V     |           |
| Input RF level            |      | 10                  | dBm   |           |
| Storage temperature range | -50  | 150                 | °C    |           |
| Reflow solder temperature |      | 260                 | °C    | T = 10 s  |

**Table 1: Absolute Maximum Ratings**



**Caution!** ESD sensitive device.  
Precaution should be used when handling  
the device in order to prevent permanent  
damage.

## 2. Operating Conditions

The operating conditions for **CC400** are listed in Table 2 below.

| Parameter                     | Min. | Max. | Units | Condition |
|-------------------------------|------|------|-------|-----------|
| Operating ambient temperature | -30  | 85   | °C    |           |

**Table 2: Operating Conditions**

## 3. Electrical Specifications

T<sub>c</sub> = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's **CC400DB** reference design.

| Parameter                                                        | Min. | Typ.      | Max. | Unit     | Condition                                       |
|------------------------------------------------------------------|------|-----------|------|----------|-------------------------------------------------|
| Supply voltage                                                   |      | 3.0       |      | V        | Recommended operation voltage                   |
|                                                                  | 2.7  |           | 3.3  | V        | Operating limits                                |
| Current Consumption,<br>receive mode                             |      | 23        |      | mA       |                                                 |
| Current Consumption,<br>average in receive mode using<br>polling |      | 230       |      | μA       | 1:100 receive to power down ratio               |
| Current Consumption,<br>transmit mode:                           |      |           |      |          | The output power is delivered to<br>a 50 Ω load |
| P=1 mW (0 dBm)                                                   |      | 33        |      | mA       |                                                 |
| P=4 mW (6 dBm)                                                   |      | 44        |      | mA       |                                                 |
| P=10 mW (10 dBm)                                                 |      | 59        |      | mA       |                                                 |
| P=20 mW (13 dBm)                                                 |      | 68        |      | mA       |                                                 |
| P=25 mW (14 dBm)                                                 |      | 77        |      | mA       |                                                 |
| Current Consumption,<br>Power Down                               |      | 23<br>0.2 | 2    | μA<br>μA | Oscillator core on<br>Oscillator core off       |

**Table 3: Electrical Specifications**

#### 4. General Characteristics

The general characteristics of **CC400** are listed in Table 4 below.

| Parameter          | Min. | Typ.                 | Max. | Unit | Condition                                                                       |
|--------------------|------|----------------------|------|------|---------------------------------------------------------------------------------|
| RF Frequency Range | 300  | 315<br>418<br>433.92 | 500  | MHz  | Programmable in steps of 250 Hz                                                 |
| Transmit data rate | 0.3  | 2.4                  | 9.6  | kbps | Manchester code is required. (9.6 kbps equals 19.2 kBaud using Manchester code) |

**Table 4: General Characteristics**

#### 5. RF Receive Section

T<sub>c</sub> = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's **CC400DB** reference design.

| Parameter                                                           | Min.                 | Typ.                | Max. | Unit                 | Condition                                                                                                                                                                                   |
|---------------------------------------------------------------------|----------------------|---------------------|------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Receiver Sensitivity                                                |                      | -110                |      | dBm                  | Measured at 433.92 MHz and a data rate of 1.2 kbps, 60 kHz IF and 20 kHz frequency separation with a bit error rate better than 10 <sup>-3</sup> . For other settings see p.15.             |
| Cascaded noise figure                                               |                      | 3                   |      | dB                   |                                                                                                                                                                                             |
| LO leakage                                                          |                      | -39                 |      | dBm                  | Measured conducted on CC400DB. Radiated LO leakage depends on external components placement.                                                                                                |
| Input impedance                                                     |                      | 39 Ω<br>+4.9 pF     |      |                      | Receive mode, series equivalent.<br>For matching details see "Input/output matching" p. 16.                                                                                                 |
| Turn on time                                                        |                      | 500<br>3<br>5<br>30 |      | μs<br>ms<br>ms<br>ms | With precharging, 9.6 kbps<br>Without precharging, 9.6 kbps<br>With precharging, 1.2 kbps<br>Without precharging, 1.2 kbps<br>See "Demodulator precharging for reduced turn-on time" p. 21. |
| Blocking / Desensitization<br>±1 MHz<br>±2 MHz<br>±5 MHz<br>±10 MHz | 30<br>35<br>50<br>60 |                     |      | dB<br>dB<br>dB<br>dB | Complies with EN 300 220 class 2 receiver requirements.<br>See p. 18 for more details.                                                                                                      |

**Table 5: RF Receive Section**

## 6. RF Transmit Section

T<sub>c</sub> = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's **CC400DB** reference design.

| Parameter                       | Min. | Typ.                    | Max. | Unit | Condition                                                                                                                                                                                                                                                                                                                                                    |
|---------------------------------|------|-------------------------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Binary FSK frequency separation | 0    | 10                      | 200  | kHz  | The frequency corresponding to the digital "0" is denoted $f_0$ , while $f_1$ corresponds to a digital "1". The frequency separation is $f_1 - f_0$ . The RF carrier frequency, $f_c$ , is then given by $f_c = (f_0 + f_1)/2$ . (The frequency deviation is given by $f_d = \pm(f_1 - f_0)/2$ ) The frequency separation is programmable in steps of 1 kHz. |
| Programmable output power       | -5   |                         | 14   | dBm  | Delivered to matched load. The output power is programmable in steps of 1 dB.                                                                                                                                                                                                                                                                                |
| RF output impedance             |      | 400 $\Omega$   <br>3 pF |      |      | Transmit mode, parallel equivalent. For matching details see "Input/ output matching" p.16.                                                                                                                                                                                                                                                                  |
| Harmonics                       |      | -30                     |      | dBc  | When transmitting high output power levels an external LC or SAW filter may be used to reduce harmonics emission to comply with ISM requirements. See p. 17.                                                                                                                                                                                                 |

**Table 6: RF Transmit Section**

## 7. IF Section

| Parameter                   | Min. | Typ.             | Max. | Unit              | Condition                                                                                                                                                                              |
|-----------------------------|------|------------------|------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Intermediate frequency (IF) |      | 60<br>200<br>455 |      | kHz<br>kHz<br>kHz | The IF is programmable. Either 60 kHz, 200 kHz or 455 kHz can be chosen.<br><br>An optional external IF filter can be used if 455 kHz is chosen. The impedance level is 1.5 k $\Omega$ |

**Table 7: IF Section**

## 8. Frequency Synthesiser Section

T<sub>c</sub> = 25°C @ VDD = 3.0 V if nothing else is stated. Measured on Chipcon's **CC400DB** reference design.

| Parameter                                                   | Min. | Typ.        | Max.           | Unit             | Condition                                                                                                                                                                                                                                            |
|-------------------------------------------------------------|------|-------------|----------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Crystal Oscillator Frequency                                | 4    | 12          | 13             | MHz              |                                                                                                                                                                                                                                                      |
| Crystal frequency accuracy requirement                      |      | +/- 50      |                | ppm              | The crystal frequency accuracy and drift (ageing and temperature dependency) will determine the frequency accuracy of the transmitted signal.                                                                                                        |
| Crystal operation                                           |      | Parallel    |                |                  | C151 and C161 are loading capacitors, see page 17.                                                                                                                                                                                                   |
| Crystal load capacitance                                    |      |             | 20<br>16<br>12 | pF<br>pF<br>pF   | 4-6 MHz<br>6-10 MHz<br>10-13 MHz                                                                                                                                                                                                                     |
| Crystal oscillator start-up time                            |      | 3           | 6              | ms               | 12 MHz, 12 pF load                                                                                                                                                                                                                                   |
| Output signal phase noise                                   |      | -70<br>-90  |                | dBc/Hz<br>dBc/Hz | 10 kHz offset from carrier<br>100 kHz offset from carrier<br>Loop filter BW = 16 kHz                                                                                                                                                                 |
|                                                             |      | -81<br>-107 |                | dBc/Hz<br>dBc/Hz | 10 kHz offset from carrier<br>100 kHz offset from carrier<br>Loop filter BW = 3 kHz                                                                                                                                                                  |
| RX / TX turn time                                           |      | 100         |                | µs               |                                                                                                                                                                                                                                                      |
| PLL turn-on time, crystal oscillator off in power down mode |      | 4           |                | ms               |                                                                                                                                                                                                                                                      |
| PLL turn-on time, crystal oscillator on in power down mode  |      | 2           |                | ms               | It is recommended to wait at least 8 ms (6 ms crystal oscillator start-up time and 2 ms PLL turn-on time) before checking the PLL Lock Indicator at the LOCK pin. Please refer to chapter "PLL Lock Indicator" on page 16 for a further description. |

**Table 8: Frequency Synthesiser Section**

## 9. DC Characteristics

The DC Characteristics of **CC400** are listed in Table 10 below. T<sub>c</sub> = 25°C if nothing else stated.

| Parameter                | Min.    | Typ. | Max.    | Unit | Condition                                    |
|--------------------------|---------|------|---------|------|----------------------------------------------|
| Logic "0" input voltage  | 0       |      | 0.3*VDD | V    |                                              |
| Logic "1" input voltage  | 0.7*VDD |      | VDD     | V    |                                              |
| Logic "0" output voltage | 0       |      | 0.4     | V    | Output current -2.5 mA, 3.0 V supply voltage |
| Logic "1" output voltage | 2.5     |      | VDD     | V    | Output current 2.5 mA, 3.0 V supply voltage  |
| Logic "0" input current  | NA      |      | -1      | µA   | Input signal equals GND                      |
| Logic "1" input current  | NA      |      | 1       | µA   | Input signal equals VDD                      |

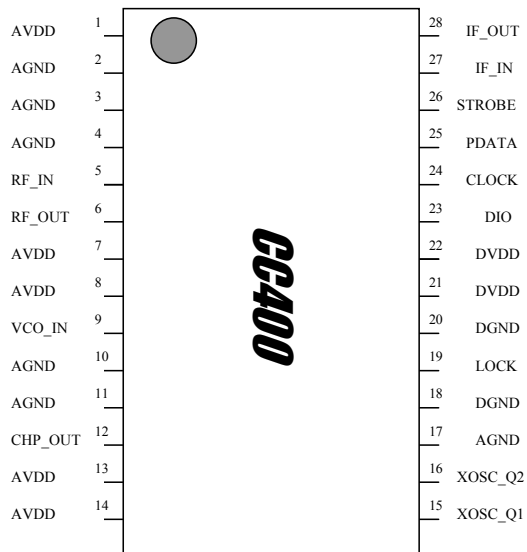
**Table 9: DC Characteristics**

## 10. Pin Assignment

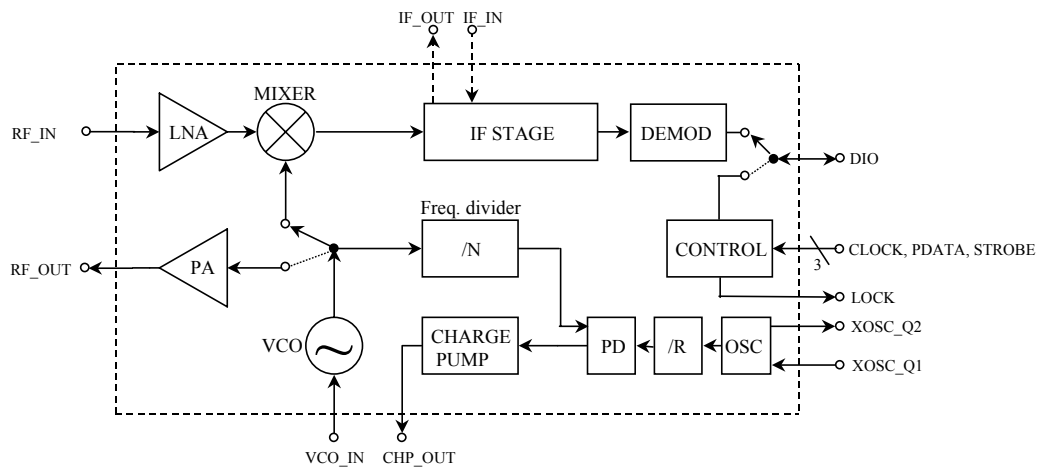
| Pin no. | Pin name | Pin type                              | Description                                                                                                                                                                   |
|---------|----------|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | AVDD     | Power (A)                             | Power supply (3V) for analog modules (Mixer, IF, demodulator)                                                                                                                 |
| 2       | AGND     | Ground (A)                            | Ground connection (0V) for analog modules (substrate)                                                                                                                         |
| 3       | AGND     | Ground (A)                            | Ground connection (0V) for analog modules (Mixer, IF, demodulator)                                                                                                            |
| 4       | AGND     | Ground (A)                            | Ground connection (0V) for analog modules (LNA and PA)                                                                                                                        |
| 5       | RF_IN    | RF Input                              | RF signal input from antenna (external ac-coupling)                                                                                                                           |
| 6       | RF_OUT   | RF output                             | RF signal output to antenna (external bias)                                                                                                                                   |
| 7       | AVDD     | Power (A)                             | Power supply (3V) for analog modules (LNA and PA)                                                                                                                             |
| 8       | AVDD     | Power (A)                             | Power supply (3V) for analog modules (VCO)                                                                                                                                    |
| 9       | VCO_IN   | Analog input                          | External VCO-tank input                                                                                                                                                       |
| 10      | AGND     | Ground (A)                            | Ground connection (0V) for analog modules (VCO)                                                                                                                               |
| 11      | AGND     | Ground (A)                            | Ground connection (0V) for analog modules (Prescaler)                                                                                                                         |
| 12      | CHP_OUT  | Analog output                         | Charge pump current output                                                                                                                                                    |
| 13      | AVDD     | Power (A)                             | Power supply (3V) for analog modules (Prescaler)                                                                                                                              |
| 14      | AVDD     | Power (A)                             | Power supply (3V) for analog modules (XOSC)                                                                                                                                   |
| 15      | XOSC_Q1  | Analog input                          | Crystal, pin 1, or external clock input                                                                                                                                       |
| 16      | XOSC_Q2  | Analog output                         | Crystal, pin 2                                                                                                                                                                |
| 17      | AGND     | Ground (A)                            | Ground connection (0V) for analog modules (XOSC)                                                                                                                              |
| 18      | DGND     | Ground (D)                            | Ground connection (0V) for digital modules (substrate)                                                                                                                        |
| 19      | LOCK     | Digital output                        | PLL Lock Indicator. Output is high when PLL is in lock. Please refer to chapter "PLL Lock Indicator" on page 16 for a further description.                                    |
| 20      | DGND     | Ground (D)                            | Ground connection (0V) for digital modules (Digital)                                                                                                                          |
| 21      | DVDD     | Power (D)                             | Power supply (3V) for digital modules (Digital)                                                                                                                               |
| 22      | DVDD     | Power (D)                             | Power supply (3V) for digital modules (Guard)                                                                                                                                 |
| 23      | DIO      | Digital input/output (bi-directional) | Data input in transmit mode<br>Demodulator output in receive mode                                                                                                             |
| 24      | CLOCK    | Digital input                         | Programming clock for 3-wire bus                                                                                                                                              |
| 25      | PDATA    | Digital input                         | Programming data for 3-wire bus                                                                                                                                               |
| 26      | STROBE   | Digital input                         | Programming strobe (Load) for 3-wire bus                                                                                                                                      |
| 27      | IF_IN    | Analog input                          | Input to IF chain (from external ceramic filter). The input impedance is 1.5 k $\Omega$ so a direct connection to an external ceramic filter is possible                      |
| 28      | IF_OUT   | Analog output                         | Output from first amplifier in IF-chain (to external ceramic filter). The output impedance is 1.5 k $\Omega$ so a direct connection to an external ceramic filter is possible |

A=Analog, D=Digital

**Figure 1: Pin-out top view**



## 11. Circuit Description



**Figure 2: Simplified block diagram of the *CC400*.**

A simplified block diagram of **CC400** is shown in Figure 2. Only signal pins are shown.

In receive mode **CC400** is configured as a traditional heterodyne receiver. The RF input signal is amplified by the low-noise amplifier (LNA) and converted down to the intermediate frequency (IF) by the mixer (MIXER). In the intermediate frequency stage (IF STAGE) this downconverted signal is amplified and filtered before being fed to the demodulator (DEMOD). As an option an external IF filter can be used for improved performance. After demodulation **CC400** outputs the raw digital demodulated data on the pin DIO. Synchronisation and final qualification of the demodulated data is done by the interfacing digital system (microcontroller).

In transmit mode the voltage controlled oscillator (VCO) output signal is fed

directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream fed to the pin DIO. The internal T/R switch circuitry makes the antenna interface and matching very easy.

The frequency synthesiser generates the local oscillator signal which is fed to the MIXER in receive mode and to PA in transmit mode. The frequency synthesiser consists of a crystal oscillator (XOSC), phase detector (PD), charge pump (CHARGE PUMP), VCO, and frequency dividers (/R and /N). An external crystal must be connected to XOSC, and an external LC-tank with a varactor diode is required for the VCO. For flexibility the loop filter is external.

For chip configuration **CC400** includes a 3-wire digital serial interface (CONTROL).

## 12. Configuration Overview

**CC400** can be configured to achieve the best performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

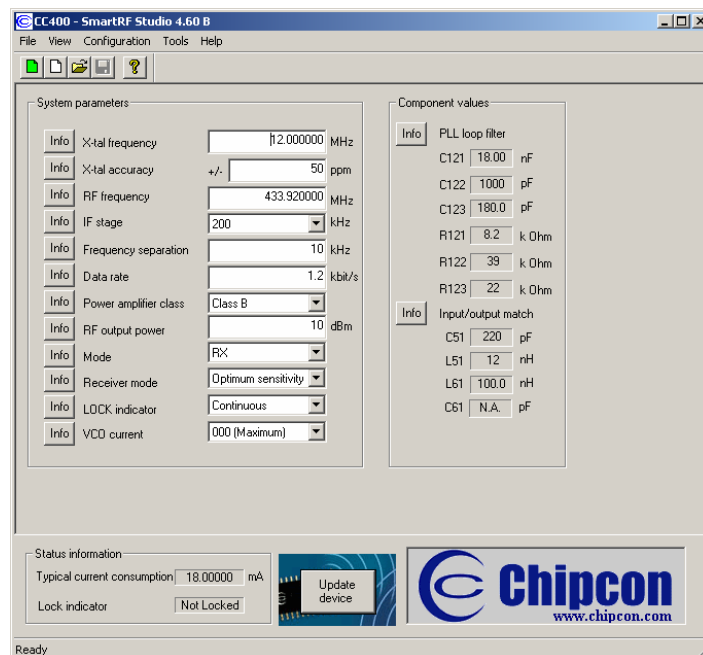
- Receive/Transmit mode.
- RF output power level.
- Power amplifier operation class (A, AB, B or C).
- Frequency synthesiser key parameters: RF output frequency, FSK modulation frequency separation (deviation), crystal oscillator reference frequency.
- Power-down/power-up mode.
- Reference oscillator on or off in power down mode (when on, shorter frequency synthesiser start-up time is achieved).
- The IF (intermediate frequency) can be set to either 60 kHz or 200 kHz using on-chip filters, or 455 kHz using an external filter.
- Data rate can be selected.
- Synthesiser lock indicator mode. The lock detection can be enabled/disabled. When enabled, two lock detection modes can be chosen, either "mono-stable" or continuous.
- In receive mode precharging of the demodulator can be used to achieve faster settling time (see p.21).

## 13. Configuration Software

Chipcon will provide users of **CC400** with a program, SmartRF Studio (Windows interface) that generates all necessary **CC400** configuration data based on the user's selections of various parameters. Based on the selections 8 hexadecimal numbers are generated. These hexadecimal numbers will then be the necessary input to the microcontroller for

configuration of **CC400**. In addition the program will provide the user with the component values needed for the PLL loop filter and the input/output matching circuit.

Figure 3 shows the user interface of the **CC400** configuration software.



**Figure 3: SmartRF Studio user interface.**

## 14. 3-wire Serial Interface

**CC400** is programmed via a simple 3-wire interface (STROBE, PDATA and CLOCK). A full configuration of **CC400** requires sending 8 data frames of 16 bits each. With a clock rate of 2 MHz the time needed for a full configuration will therefore be less than 100  $\mu$ s. Setting the device in power down mode requires sending one frame only and will therefore take less than 10  $\mu$ s.

In each write-cycle 16 bits are sent on the PDATA-line. The three most significant bits of each data frame (*bit15*, *bit14* and *bit13*) are the address-bits. *Bit15* is the MSB of the address and is sent as the first bit. See Figure 4.

A timing diagram for the programming is shown in Figure 5. The clocking of the data on PDATA is done on the negative edge of CLOCK. When the last bit, *bit0*, of the sixteen bits has been loaded, the STROBE-pulse must be brought high and then low to load the data.

The configuration data will be valid after a programmed power-down mode, but not when the power-supply is turned off. When changing mode, only the frames that are different need to be programmed.

The timing specifications are given in Table 10.

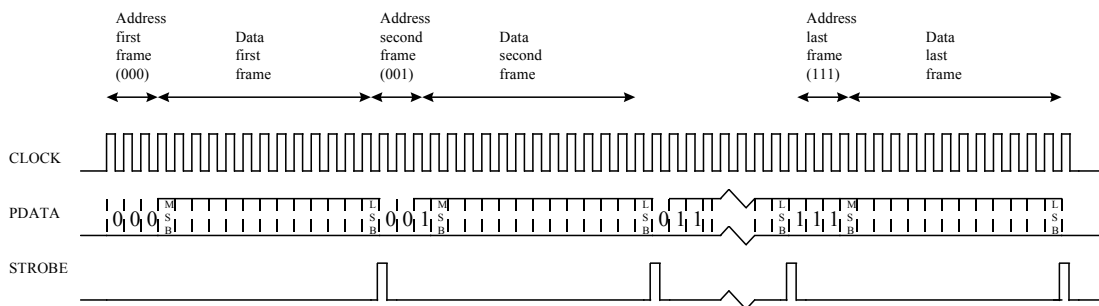


Figure 4: Serial data transfer (full configuration).

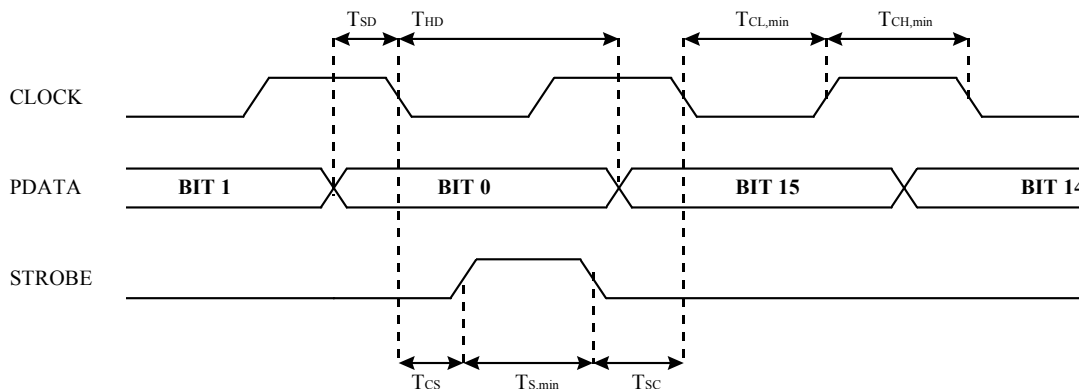


Figure 5: Timing diagram, serial interface.

| Parameter                 | Symbol              | Min | Max | Units | Conditions                                                                        |
|---------------------------|---------------------|-----|-----|-------|-----------------------------------------------------------------------------------|
| CLOCK, clock frequency    | $F_{\text{CLOCK}}$  | -   | 2   | MHz   |                                                                                   |
| CLOCK low pulse duration  | $T_{\text{CL,min}}$ | 50  |     | ns    | The minimum time CLOCK can be low.                                                |
| CLOCK high pulse duration | $T_{\text{CH,min}}$ | 50  |     | ns    | The minimum time CLOCK can be high.                                               |
| PDATA setup time          | $T_{\text{SD}}$     | 5   | -   | ns    | The minimum time data on PDATA must be ready before the negative edge of CLOCK.   |
| PDATA hold time           | $T_{\text{HD}}$     | 5   | -   | ns    | The minimum time data must be held at PDATA, after the negative edge of CLOCK.    |
| CLOCK to STROBE time      | $T_{\text{CS}}$     | 5   | -   | ns    | The minimum time after the negative edge of CLOCK before positive edge of STROBE. |
| STROBE to CLOCK time      | $T_{\text{SC}}$     | 5   | -   | ns    | The minimum time after the negative edge of STROBE before negative edge of CLOCK. |
| STROBE pulse duration     | $T_{\text{S,min}}$  | 50  |     | ns    | The minimum time STROBE can be high.                                              |
| Rise time                 | $T_{\text{rise}}$   |     | 100 | ns    | The maximum rise time for CLOCK and STROBE                                        |
| Fall time                 | $T_{\text{fall}}$   |     | 100 | ns    | The maximum fall time for CLOCK and STROBE                                        |

Note: The set-up- and hold-times refer to 50% of VDD.

**Table 10: Serial interface, timing specification.**

## 15. Microcontroller Interface

Used in a typical system, **CC400** will interface to a microcontroller. This microcontroller must be able to:

- Program the **CC400** into different modes via the 3-wire serial interface (PDATA, STROBE, CLOCK).
- Operate with the bidirectional data pin DIO.
- Perform oversampling of the demodulator output (on pin DIO), recover the clock corresponding to the actual datarate, and perform data qual-

ification (on Manchester encoded data).

- Data to be sent must be Manchester encoded.
- Optionally the microcontroller can monitor the frequency lock status from pin LOCK.
- Optionally the microcontroller can perform precharging of the receiver in order to reduce the turn-on time (see p.21).

### 15.1. Connecting the microcontroller

The microcontroller uses 3 output pins for the serial interface (PDATA, STROBE and CLOCK). A bi-directional pin is used for data to be transmitted and data received (DIO). Optionally another pin can be used to monitor the LOCK signal. This signal is logic level high when the PLL is in lock. See Figure 7.

### 15.2. Data transmission

The data to be sent has to be Manchester encoded (also known as bi-phase-level coding). The Manchester code ensures that the signal has a constant DC component that is necessary for the FSK demodulator. The Manchester code is based on transitions; a "0" is encoded as a low-to-high transition, a "1" is encoded as a high-to-low transition. See Figure 6. When the DIO is logic level high, the upper FSK frequency is transmitted. The lower frequency is transmitted when DIO is low.

Note that the receiver data output is inverted when using low-side LO, which is default using SmartRF Studio.

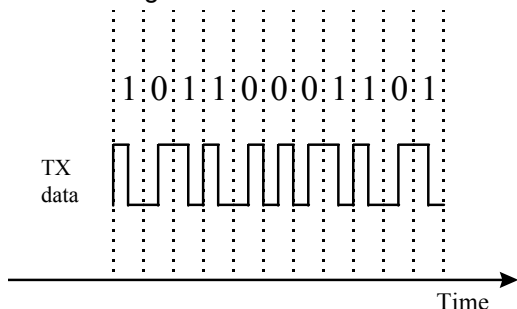


Figure 6: Manchester encoding.

### 15.3. Data reception

The output of the demodulator (DIO) is a digital signal (alternating between 0 V and VDD). For small input signals, there will be some noise on this signal, located at the edges of the digital signal. The datarate of this signal may be up to 9.6 kbps. Due to the Manchester coding, the fundamental frequency of the signal is also 9.6 kHz. An oversampling of 4-8 times the frequency of the demodulator-output is recommended. I.e. the sampling frequency should be at least 40-80 kHz for 9.6 kbps. For a lower datarate the sampling frequency can be reduced.

In a typical application the data output is sampled by the microcontroller, and stored in an accumulating register. The length of this register will typically be 4-8 bits (depending on the oversampling ratio). The qualification of the data (decide whether the signal is "0" or "1") can be based on comparing the number of 0's with the number of 1's. See Application Note AN008 "Oversampling and data decision for the CC400/CC900" for more details.

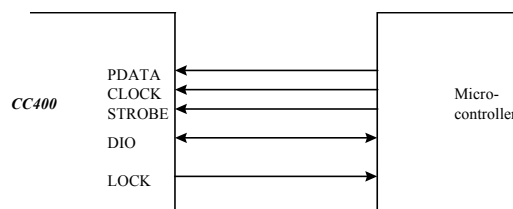


Figure 7: Microcontroller interface.

## 16. Application Circuit

Very few external components are required for operation of **CC400**. A typical application circuit for 433.92 MHz operation is shown in **Figure 8**. 1.2 kbps data rate and 20 kHz FSK separation are used. Typical component values are shown in Table 11.

### 16.1. Input / output matching

L51 and C51 are the input match for the receiver, and L61 and C61 are the output match for the transmitter. An internal T/R switch circuitry makes it possible to connect the input and output together matching to 50Ω. See "Input/output matching" p.16 for details.

### 16.2. Synthesizer loop filter and VCO tank

The PLL loop filter consists of C121-C123 and R121-R123. The Component values are easily calculated using the SmartRF Studio software.

The VCO tank consists of C91-C93, L91 and the varactor (VAR). C91 determines the coupling to the internal VCO amplifier, and thus the VCO loop gain. This loop

gain is also controlled by the 'VCO gain' setting in SmartRF Studio, by changing the amplifier current. C92 together with the varactor's capacitance ratio determines the VCO sensitivity (MHz/V). The sensitivity should be 20 MHz/V. L91 and C93 is used to set the absolute range of the VCO. See Application Note AN012 "VCO fine-tuning CC400 and CC900" for more details.

### 16.3. Additional filtering

Additional external components (e.g. ceramic IF-filter, RF LC or SAW-filter) may be used in order to improve the performance for specific applications. See also "Optional LC filter" p.17 for further information.

### 16.4. Voltage supply decoupling

C10-C12, C24-C25, C210 and C211 are voltage supply de-coupling capacitors. These capacitors should be placed as close as possible to the voltage supply pins of **CC400**. The **CC400DB** should be used as a reference design.

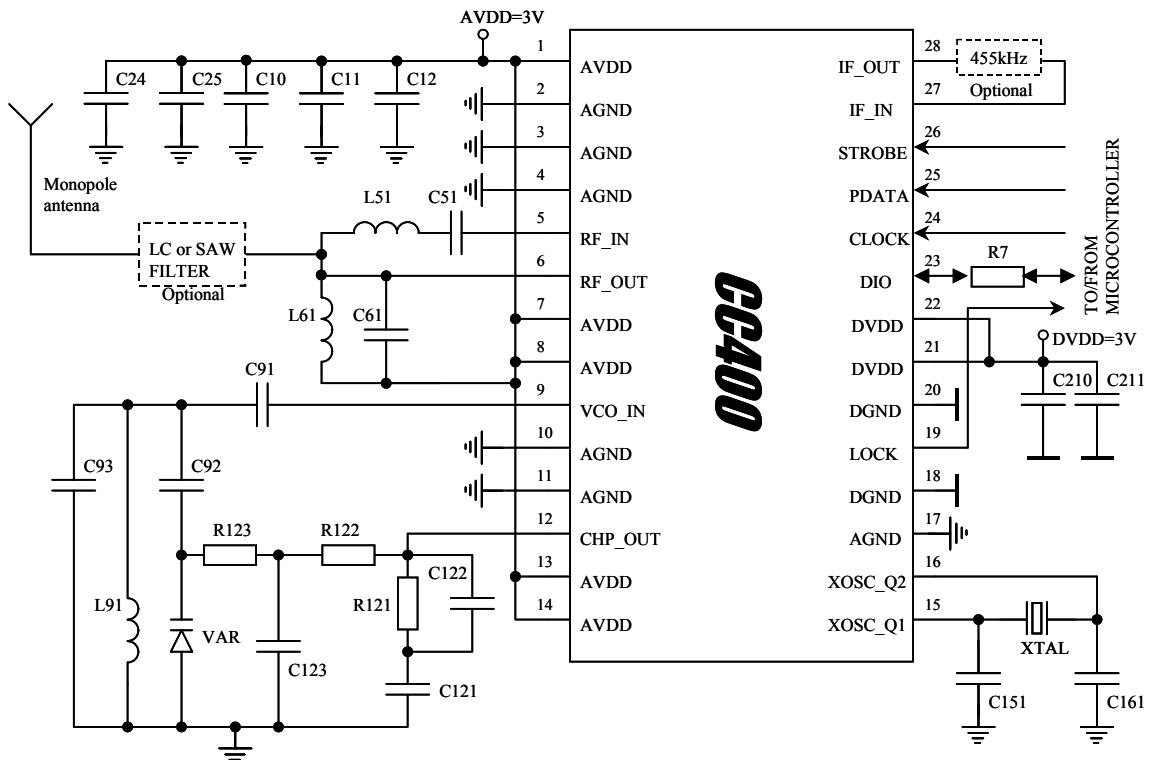


Figure 8: Typical **CC400** application for 433.92 MHz operation.

| Item | Description                     |
|------|---------------------------------|
| C10  | 1 nF, X7R, 0603                 |
| C11  | 33 nF, X7R, 0603                |
| C12  | 4.7 nF, NP0, 1206               |
| C24  | 33 pF, NP0, 0603                |
| C25  | 220 pF, NP0, 0603               |
| C51  | 220 pF, NP0, 0603               |
| C61  | 12 pF, NP0, 0603                |
| C91  | 4.7 pF, NP0, 06035              |
| C92  | 8.2 pF, NP0, 0603               |
| C93  | 3.9 pF, NP0, 0603               |
| C121 | 33 nF, X7R, 0603                |
| C122 | 1.5 nF, X7R, 0603               |
| C123 | 330 pF, NP0, 0603               |
| C161 | 15 pF, NP0, 0603                |
| C151 | 15 pF, NP0, 0603                |
| C210 | 1 nF, X7R, 0603                 |
| C211 | 33 nF, X7R, 0603                |
| L51  | 39 nH, 0805                     |
| L61  | 6.8 nH, 0805                    |
| L91  | 10 nH, 0805                     |
| R7   | 10 k $\Omega$ , 0603 (optional) |
| R121 | 5.6 k $\Omega$ , 0603           |
| R122 | 27 k $\Omega$ , 0603            |
| R123 | 22 k $\Omega$ , 0603            |
| VAR  | KV1837K, TOKO or similar        |
| XTAL | 12 MHz crystal, 12 pF load      |

**Table 11: Bill of materials for the application circuit.**

## 17. Receiver sensitivity

The receiver sensitivity depends on which IF frequency and IF filter that has been selected (60, 200 or 455 kHz). It also depends on the data rate (0.3 – 9.6 kbps) and the FSK frequency separation (0 – 200 kHz). Frequency *separation* is twice

the frequency *deviation* (for example, 20 kHz separation is +/-10 kHz deviation).

Some typical figures are shown in Table 12.

| Data rate | IF frequency | Separation | CC400    |
|-----------|--------------|------------|----------|
| 1.2 kbps  | 60 kHz       | 20 kHz     | -110 dBm |
|           | 200 kHz      | 40 kHz     | -103 dBm |
|           | 455 kHz ext  | 12 kHz     | -108 dBm |
| 2.4 kbps  | 60 kHz       | 30 kHz     | -110 dBm |
|           | 200 kHz      | 40 kHz     | -103 dBm |
|           | 455 kHz ext  | 20 kHz     | -103 dBm |
| 4.8 kbps  | 200 kHz      | 40 kHz     | -101 dBm |
|           | 455 kHz ext  | 20 kHz     | -99 dBm  |
| 9.6 kbps  | 200 kHz      | 40 kHz     | -97 dBm  |

**Table 12: Sensitivity for different IF frequency, data rates and separation.**

In a narrow band system with very low frequency separation (less than 10 kHz) the sensitivity will drop. To insure proper operation the separation should always be larger than 5 kHz (+/- 2.5 kHz deviation). For even smaller separation, or to improve

the sensitivity, an external narrow band demodulator should be used. See Application Note AN005 "Selecting system parameters and system configurations using CC400 / CC900" for more information on narrow band systems.

## 18. Output power

The output power is controlled through several parameters in the configuration

registers. Table 13 shows recommended settings for the different output powers.

| Output power | Class | Register |      |                |
|--------------|-------|----------|------|----------------|
|              |       | E9:8     | F1:0 | C8,A7:6,D12:11 |
| -5           | A     | 00       | 00   | 01011          |
| -4           | AB    | 01       | 00   | 00100          |
| -3           | AB    | 01       | 01   | 00101          |
| -2           | AB    | 01       | 01   | 00110          |
| -1           | AB    | 01       | 01   | 00111          |
| 0            | B     | 10       | 10   | 00011          |
| 1            | B     | 10       | 10   | 00100          |
| 2            | B     | 10       | 10   | 00101          |
| 3            | B     | 10       | 10   | 00110          |
| 4            | B     | 10       | 10   | 00111          |
| 5            | B     | 10       | 10   | 01000          |
| 6            | B     | 10       | 10   | 01001          |
| 7            | B     | 10       | 10   | 01010          |
| 8            | C     | 11       | 11   | 01001          |
| 9            | C     | 11       | 11   | 01010          |
| 10           | C     | 11       | 11   | 01100          |
| 11           | C     | 11       | 11   | 01111          |
| 12           | C     | 11       | 11   | 10001          |
| 13           | C     | 11       | 11   | 10101          |
| 14           | C     | 11       | 11   | 11011          |

Table 13: Output power settings.

## 19. Input / Output Matching

Four passive external components combined with the internal T/R switch circuitry ensures match in both RX and TX mode. The matching network for 433.92 MHz is shown in Figure 9. The component values may have to be optimised to

include layout parasitics. Matching components for other frequencies can be found using the configuration software. See also Application Note AN013 "Matching CC400 CC900" for more details.

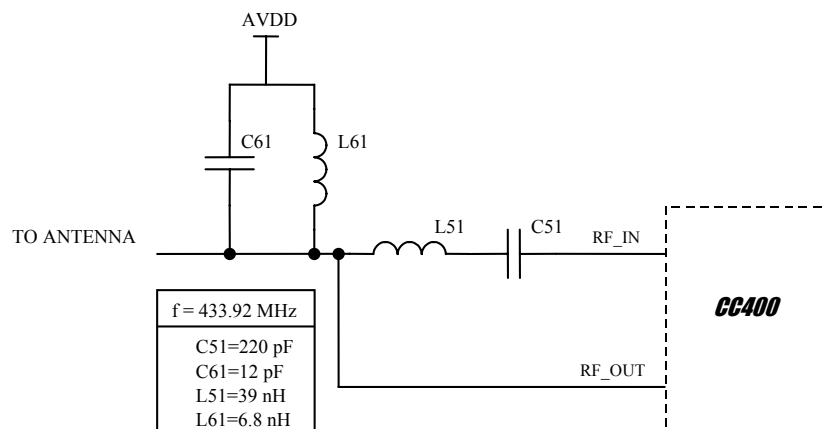


Figure 9: Input/output matching network.

## 20. Optional LC Filter

An optional LC filter may be added between the antenna and the matching network in certain applications. The filter will reduce the emission of harmonics and increase the receiver selectivity.

The filter for use at 433.92 MHz is shown in Figure 10. The component values may have to be optimised to include layout parasitics. The filter is designed for 50Ω terminations.

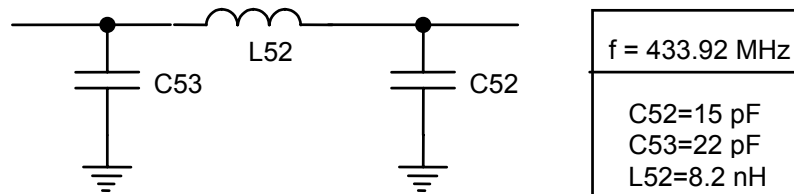


Figure 10: LC filter.

## 21. Crystal oscillator

An external clock signal or the internal crystal oscillator can be used as main frequency reference. An external clock signal should be connected to XOSC\_Q1, while XOSC\_Q2 should be left open. The crystal frequency must be in the range 4 - 13 MHz.

Using the internal crystal oscillator, the crystal must be connected between XOSC\_Q1 and XOSC\_Q2. The oscillator is designed for parallel mode operation of the crystal. In addition loading capacitors (C151 and C161) for the crystal are required. The loading capacitor values depend on the total load capacitance,  $C_L$ , specified for the crystal. The total load capacitance seen between the crystal terminals should equal  $C_L$  for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{151}} + \frac{1}{C_{161}}} + C_{\text{parasitic}}$$

The parasitic capacitance is constituted by the pins input capacitance and PCB stray capacitance. Typically the total parasitic capacitance is 4.5 pF. A trimming capacitor may be placed across C151 for initial tuning if necessary.

The crystal oscillator circuit is shown in Figure 11. Typical component values for different values of  $C_L$  are given in Table 14.

The initial tolerance, temperature drift, ageing and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application. By specifying the *total* expected frequency accuracy in SmartRF Studio together with data rate and frequency separation, the software will calculate the total bandwidth and compare to the available IF bandwidth. The software will report any contradictions and a more accurate crystal will be recommended if required.

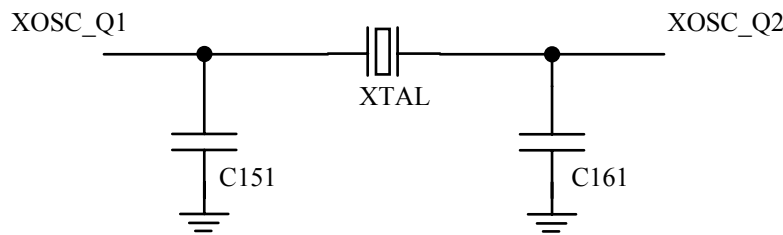


Figure 11: Crystal oscillator circuit.

| Item | $C_L = 12 \text{ pF}$ | $C_L = 16 \text{ pF}$ | $C_L = 22 \text{ pF}$ |
|------|-----------------------|-----------------------|-----------------------|
| C151 | 15 pF                 | 22 pF                 | 33 pF                 |
| C161 | 15 pF                 | 22 pF                 | 33 pF                 |

**Table 14: Crystal oscillator component values.**

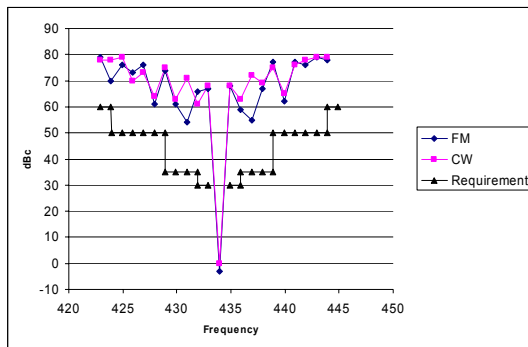
## 22. Loop filter

The loop filter is a lead-lag type of filter. The calculations for the loop filter components are done in the SmartRF Studio software.

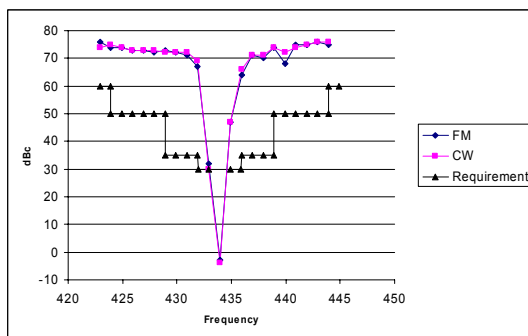
See Application Note AN012 "VCO fine tuning for CC400 and CC900" for more

detailed information. A spreadsheet, CC400\_CC900\_Loop\_Filter\_1\_0.xls, is available from Chipcon that will calculate the loop filter components for a desired bandwidth with different constants than the default values in SmartRF Studio.

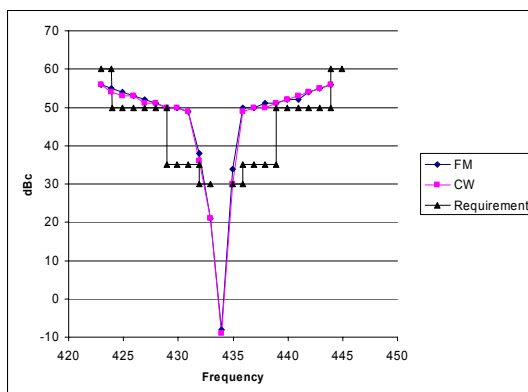
## 23. Blocking



IF = 60 kHz, Separation = 20 kHz. Data rate = 1.2 kbps. Interfering signal is CW (no modulation) or FM modulation.



IF = 200 kHz, Separation = 40 kHz. Data rate = 1.2 kbps. Interfering signal is CW (no modulation) or FM modulation.



IF = 455 kHz external, Separation = 12 kHz. Data rate = 1.2 kbps. Interfering signal is CW (no modulation) or FM modulation.

## 24. PLL Lock Indicator

The **CC400** PLL lock indicator is available on the LOCK pin. The PLL lock signal is not 100% conclusive. That is, if the LOCK signal indicates lock (i.e. a high signal on the LOCK pin) the PLL has locked to the

desired frequency. However, situations might arise where the lock signal does not indicate lock (i.e. a low signal on the LOCK pin) when in fact the PLL has locked to the desired frequency.

## 25. Antenna Considerations

The **CC400** can be used together with various types of antennas. The most common antennas for short-range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength ( $\lambda/4$ ). They are very easy to design and can be implemented simply as a “piece of wire” or integrated into the PCB.

Non-resonant monopole antennas shorter than  $\lambda/4$  can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated into the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimise than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the  $\lambda/4$ -monopole antenna is recommended giving the best range and because of its simplicity.

The length of the  $\lambda/4$ -monopole antenna is given by:

$$L = 7125 / f$$

where  $f$  is in MHz, giving the length in cm. An antenna for 433.92 MHz should be 16.4 cm.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the input pin the antenna should be matched to the feeding transmission line. See Application Note AN003 “Antennas” for more details.

## 26. System Considerations and Guidelines

### 26.1. Low-cost systems

In systems where low cost is of great importance the 200 kHz IF should be used. The oscillator crystal can then be a low cost crystal with 50 ppm frequency tolerance.

### 26.2. Battery operated systems

In low power applications the power down mode should be used when not being active. Depending on the start-up time requirement, the oscillator core can be powered during power down. Precharging of the demodulator may also be used to reduce the receiver turn-on time, see description p.21.

### 26.3. Narrow band systems

**CC400** is also suitable for use in narrow band systems. However, it is then required to use a crystal with low temperature drift and ageing. A trimmer capacitor in the crystal oscillator circuit (in parallel with C151) may also be necessary to set the initial frequency.

It is also possible to include an external IF-filter at 455 kHz. This should be a ceramic filter with 1.5 k $\Omega$  input/output impedance connected between IF\_OUT and IF\_IN. Typical bandwidth is 30 kHz. Due to the high Q of such a filter, a better selectivity can be achieved. See Application Note AN005 "Selecting system parameters and system configurations using CC400 / CC900" for more details.

### 26.4. High reliability systems

Using a SAW filter as a preselector will improve the communication reliability in harsh environments by reducing the probability of blocking.

### 26.5. Spread spectrum frequency hopping systems

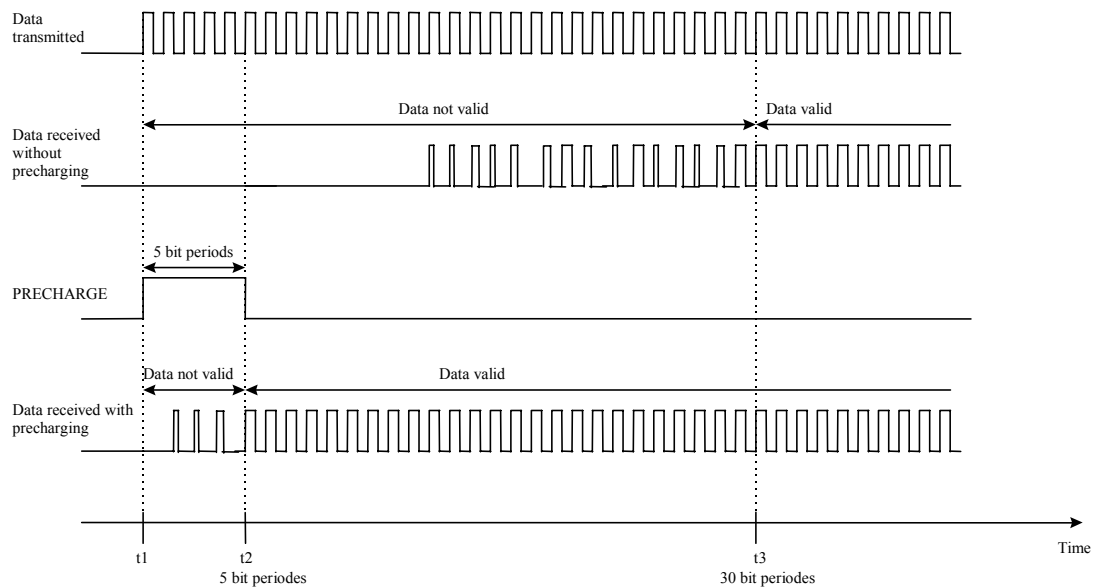
Due to the very fast frequency shift properties of the PLL, the **CC400** may very well be used in frequency hopping systems.

## 27. Demodulator Precharging For Reduced Turn-on Time

The demodulator data slicer has an internal AC coupling giving a time constant of approximately 30 periods of the bit rate period. This means that before proper demodulation can take place, a minimum of 30 start-bits has to be received.

In critical applications where the start-up time should be decreased in order to

reduce the power consumption, this time constant can be reduced to 5 periods using the optional precharging possibility. The precharging is done during data reception by setting the precharging bit in the configuration register active with duration of at least 5 bit periods.



**Figure 12: Demodulation using precharging.**

In the example shown in Figure 12, data is transmitted continuously from the transmitter (all 1's). At  $t=t_1$  the receiver is turned on, and then the precharging is

kept on for about 5 bit periods. At  $t=t_2$  the received data is valid and precharging is turned off. When not using precharging, data is not valid until 30 bit periods, at  $t=t_3$ .

## 28. PCB Layout Recommendations

A two layer PCB is highly recommended. The bottom layer of the PCB should be the “ground-layer”.

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The ground pins should be connected to ground as close as possible to the package pin. The decoupling capacitors should also be placed as close as possible to the supply pins and connected to the ground plane by separate vias.

The external components should be as small as possible and surface mount devices should be used.

Precaution should be used when placing the microcontroller in order to avoid interference with the RF circuitry.

In most applications the ground plane can be one common plane, but in certain applications where the ground plane for the digital circuitry is expected to be noisy, the ground plane may be split in an analogue and a digital part. All AGND pins and AVDD decoupling capacitors should be connected to the analogue ground plane. All DGND pins and DVDD decoupling capacitors should be connected to the digital ground. The connection between the two ground planes should be implemented as a star connection with the power supply ground.

The **CC400DB** reference design is available from Chipcon’s web site, and should be used as a guideline for PCB layout.

## 29. Configuration registers

The configuration of **CC400** is done by programming the 8 13-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF Studio software. A complete description of the registers is given in the following tables.

### REGISTER OVERVIEW

| Address | Register Name | Description              |
|---------|---------------|--------------------------|
| 000     | A             | Main control register    |
| 001     | B             | General control register |
| 010     | C             | General control register |
| 011     | D             | General control register |
| 100     | E             | General control register |
| 101     | F             | General control register |
| 110     | G             | General control register |
| 111     | H             | General control register |

Register A

| REGISTER | NAME     | Default value | Active | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|----------|---------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[12]    | PD       | -             | H      | Power Down<br>0 = Chip Enable<br>1 = Chip Disable (only reference oscillator core on)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| A[11]    | RXTX     | -             |        | Receive/Transmit-mode control<br>0 = Receive mode<br>1 = Transmit mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| A[10:8]  | S[2:0]   | 000           |        | Synthesiser test modes (apply when TDEM2=0)<br><u>Modus (000):</u><br>Normal operation: Rx/Tx.<br><u>Modus (001):</u><br>Divided signal from VCO at PD input monitored at LOCK pin. Modulation (control of A-counter) is disabled.<br><u>Modus (010):</u><br>Divided signal from VCO at PD input monitored at LOCK pin. Modulation (control of A-counter) is enabled.<br><u>Modus (011):</u><br>Output from reference divider monitored at LOCK pin.<br><u>Modus (100):</u><br>Signal at TX_DATA pin used as modulation control overriding the signal from the dual-modulus divider. Output monitored at LOCK pin.<br><u>Modus (101):</u><br>Output from prescaler monitored at LOCK pin. Modulation (A-divider control) disabled.<br><u>Modus (110):</u><br>Output from prescaler monitored at LOCK pin. Modulation (A-divider control) disabled.<br><u>Modus (111):</u><br>Shift register data output monitored at LOCK pin. |
| A[7:6]   | PA[3:2]  | -             |        | PA gain programming. Part of PA4:PA0. (PA1:PA0 is in frame D, PA4 is in frame C)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| A[5:4]   | LNA[1:0] | 10            |        | LNA bias current and gain<br>00 = 0.94mA= $I_0$<br>01 = 1.5* $I_0$ =1.40mA<br>10 = 2* $I_0$ =1.87mA (nominal setting)<br>11 = 3* $I_0$ =2.81mA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| A[3:2]   | MIX[1:0] | 10            |        | MIXER bias current and gain<br>00 = 0.36mA<br>01 = 0.54mA<br>10 = 0.72mA (nominal setting)<br>11 = 1.08mA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| A[1:0]   | LO[1:0]  | 10            |        | LO drive (peak-differential = peak-peak single-ended)<br>00 = 144mV<br>01 = 288mV<br>10 = 432mV (nominal setting)<br>11 = 720mV                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Register B**

| REGISTER | NAME    | Default value | Active | Description                                                                                                                    |
|----------|---------|---------------|--------|--------------------------------------------------------------------------------------------------------------------------------|
| B[12:11] | AB[1:0] | 00            |        | Antibacklash pulse width<br>00 = 0ns (nominal setting)<br>01 = 2.7ns<br>10 = 4.8ns<br>11 = 10.9ns<br>Tolerance (+200% / - 70%) |
| B[10:7]  | A[3:0]  | -             |        | A-counter                                                                                                                      |
| B[6:0]   | M[6:0]  | -             |        | M-counter                                                                                                                      |

**Register C**

| REGISTER | NAME     | Default value | Active | Description                                                                                                                       |
|----------|----------|---------------|--------|-----------------------------------------------------------------------------------------------------------------------------------|
| C[12]    | RESSYN   | 0             |        | Synthesiser reset<br>0 = Normal operation<br>1 = Reset synthesiser                                                                |
| C[11:9]  | V[3:1]   | -             |        | VCO gain programming.<br>LSB-bit VO = "0".<br>000= maximum gain<br>111=minimum gain<br>Reduce gain to reduce LO spurious emission |
| C[8]     | PA[4]    | -             |        | PA gain programming. Part of PA4:PA0                                                                                              |
| C[7]     | FSIG     | -             |        | Charge pump polarity<br>0 = Add charge when VREF leads FVCO (Normal)<br>1 = Sink charge when VREF leads FVCO                      |
| C[6:5]   | CHP[1:0] | 10            |        | Charge pump current:<br>00 = 10µA<br>01 = 20µA<br>10 = 40µA (nominal setting)<br>11 = 80µA                                        |
| C[4]     | PDX      | -             | H      | Reference oscillator power down<br>0 = Power on even during main power down<br>1 = Power down (during main power down)            |
| C[3:0]   | R[3:0]   | -             |        | R-divider                                                                                                                         |

**Register D**

| REGISTER | NAME    | Default value | Active | Description                                                                                 |
|----------|---------|---------------|--------|---------------------------------------------------------------------------------------------|
| D[12:11] | PA[1:0] | -             |        | PA gain programming. Part PA4                                                               |
| D[10:0]  | K[10:0] | -             |        | K-counter<br>K10 er sign bit (0=positive, 1 negative).<br>Negative K must be 2's complement |

**Register E**

| REGISTER | NAME | Default value | Active | Description                                                                                 |
|----------|------|---------------|--------|---------------------------------------------------------------------------------------------|
| E[12]    | LW   | 0             |        | PLL Lock-Window tolerance<br>0 = 21ns (Normal setting)<br>1 = 44ns                          |
| E[11]    | LM   | -             |        | Lock mode<br>(Lock is reset when PLL is reprogrammed).<br>0 = Single shot<br>1 = Continuous |
| E[10]    | LH   | -             |        | Lock detection enable<br>0 = Lock detection enabled<br>1 = Lock detection disabled (LOCK=1) |

| REGISTER | NAME      | Default value | Active | Description                                                                 |
|----------|-----------|---------------|--------|-----------------------------------------------------------------------------|
| E[9:8]   | PACL[1:0] | -             |        | PA "class"<br>00 = Class A<br>01 = Class AB<br>10 = Class B<br>11 = Class C |
| E[7:0]   | D[7:0]    | -             |        | D-counter<br>Frequency separation programming                               |

Register F

| REGISTER | NAME       | Default value | Active | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|------------|---------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F[12:11] | DCLK[1:0]  | -             |        | Demodulator shift register clock selection<br>00 = External clock (25MHz) at TX_DATA.<br>01 = 12.8 MHz from crystal oscillator<br>10 = 25 MHz from prescaler<br>11 = 12.5MHz from prescaler                                                                                                                                                                                                                                                                                                                                                                                                       |
| F[10:9]  | DEMIF[1:0] | -             |        | Demodulator phase shift / IF control<br>00 = 60kHz IF<br>01 = 200kHz IF<br>10 = 455kHz IF<br>11 = Test modes using DCLK1:DCLK0                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| F[8:6]   | TDEM[2:0]  | 000           |        | Test modes for demodulator. Output is monitored at LOCK pin. See also S2:S0 in frame A.<br>TDEM2=0: As described for S2:S0 in frame A<br>TDEM2=1 : Demodulator test modes.<br><u>Modus (000):</u><br>Normal setting.<br><u>Modus (0XX):</u><br>Test as for S2:S0 in frame A monitored at LOCK pin.<br><u>Modus (100):</u><br>Demodulator input monitored at LOCK pin.<br><u>Modus (101):</u><br>Phase shifted signal monitored at LOCK pin.<br><u>Modus (110):</u><br>Phase detector output monitored at LOCK pin.<br><u>Modus (111):</u><br>Demodulator output at LOCK pin. IF input at TX_DATA. |
| F[5:3]   | PAIMP[2:0] | -             |        | PA capacitor array.<br>Array is active in RX or TX depending on INVARRAY.<br>000 = 0pF<br>001 = 1.25pF<br>010 = 2.5pF<br>011 = 3.75pF<br>100 = 5pF<br>101 = 6.25pF<br>110 = 7.5pF<br>111 = 8.75pF                                                                                                                                                                                                                                                                                                                                                                                                 |
| F[2]     | INVARRAY   | -             |        | PA capacitor array activation.<br>0 = Capacitor array active in RX mode<br>1 = Capacitor array active in TX mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| F[1:0]   | PAEC[1:0]  | -             |        | PA buffer amplifier drive level<br>00 = 3mA<br>01 = 5mA<br>10 = 8mA<br>11 = 11mA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

Register G

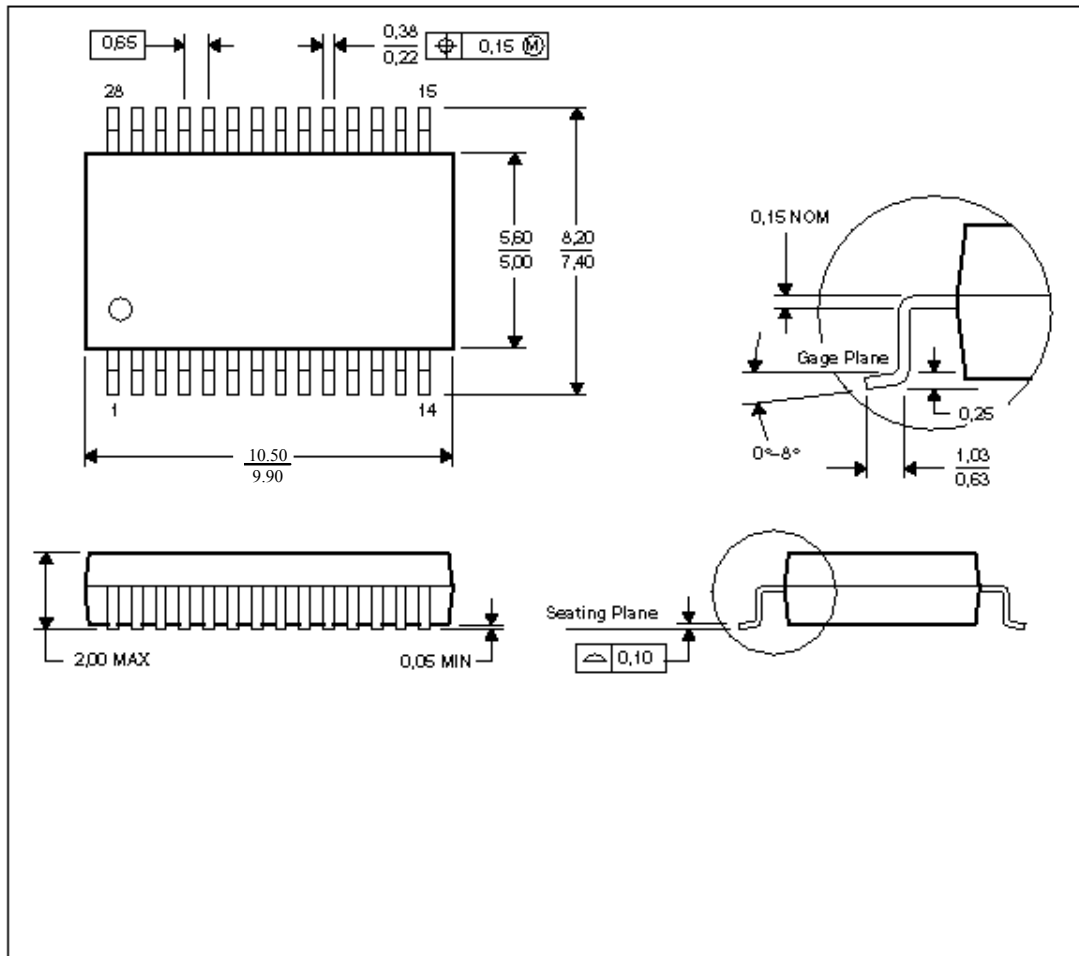
| REGISTER | NAME      | Default value | Active | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|-----------|---------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G[12:11] | IFQ[1:0]  | -             |        | IF filter Q-value<br>00 = low<br>01 =<br>10 =<br>11 = high                                                                                                                                                                                                                                                                                                                                                                       |
| G[10:9]  | IFG[1:0]  | -             |        | IF amplifier gain<br>00 = lowest<br>01 =<br>10 =<br>11 = highest                                                                                                                                                                                                                                                                                                                                                                 |
| G[8:6]   | LPIF[2:0] | -             |        | IF filter low-pass cut-off<br>000 = lowest<br>001 =<br>010 =<br>011 =<br>100 =<br>101 =<br>110 =<br>111 = highest                                                                                                                                                                                                                                                                                                                |
| G[5:3]   | HPIF[2:0] | -             |        | IF filter high-pass cut-off<br>000 = lowest<br>001 =<br>010 =<br>011 =<br>100 =<br>101 =<br>110 =<br>111 = highest                                                                                                                                                                                                                                                                                                               |
| G[2:0]   | MIF[2:0]  | -             |        | IF mode control, external filter selection<br>000 = Differential input, 1. Ceramic filter<br>001 = Single-ended input 1. ceramic filter<br>010 = Differential input, 1. and 2. ceramic filter (NA)<br>011 = Single-ended input, 1. and 2. ceramic filter (NA)<br>100 = Differential input, no ceramic filters filters<br>101 = Single-ended input, no ceramic filters<br>110 = NA<br>111 = Single-ended input, 1. Ceramic filter |

Register H

| REGISTER | NAME       | Default value | Active | Description                                                                                                                                                                       |
|----------|------------|---------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H[12:10] | LPDEM[2:0] | -             |        | Demodulator data filter cut-off (low pass)<br>000 = 5.8kHz<br>001 = 9.3kHz<br>010 = 13.9kHz<br>011 = 19.9kHz<br>100 = 28.0kHz<br>101 = 36.2kHz<br>110 = 64.8kHz<br>111 = 134.2kHz |
| H[9]     | FASTACIDF  | 0             |        | Demodulator datafilter AC coupling time constant (Precharge)<br>0 = Normal/high time constant<br>1 = Low time constant (precharge)                                                |

| REGISTER | NAME         | Default value | Active | Description                                                                                                                                                                 |
|----------|--------------|---------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H[8]     | TOPFILT      | -             |        | Demodulator data filter topology<br>AC coupling by-pass<br>0 = Two AC couplings<br>1 = One AC coupling                                                                      |
| H[7:6]   | HYSTDEM[1:0] | -             |        | Demodulator data slicer comparator hysteresis<br>00 = 0mV<br>01 = 15mV<br>10 = 40mV<br>11 = 100mV                                                                           |
| H[5:4]   | HPDEM[1:0]   | -             |        | Demodulator data filter high-pass cut-off<br>00 = 30Hz<br>01 = 60Hz<br>10 = 120Hz<br>11 = 240Hz                                                                             |
| H[3]     | EXTACDF      | 0             |        | Demodulator external AC-coupling<br>0 = Internal<br>1 = Eksternal (NA)                                                                                                      |
| H[2]     | IFSIGEXT     | 0             |        | IF test mode<br>IF signal input at TX_DATA pin<br>Use LOCK pin as demodulator output<br>0 = Normal<br>1 = Test mode                                                         |
| H[1]     | QUADSWING    | -             |        | Quadrature detector output level<br>0 = VDD (normal setting)<br>1 = Reduced amplitude (VDD/2)                                                                               |
| H[0]     | IFDOFF       | 0             |        | IF and demodulator Power Down (overrided by global power down).<br>0 = IF and demodulator active (if PD=0 and RxTx=0). Normal setting.<br>1 = IF and demodulator power down |

### 30. Package Description (SSOP-28)



**Figure 13: Package Dimensions Drawing**

**NOTES:**

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.1mm.
- D. Falls within JEDEC MO-150.

### 31. Soldering Information

The recommended reflow soldering profiles for SnPb eutectic and Pb-free soldering for Small Body SMD packages are according to IPC/JEDEC J-STD-020C.

### 32. Plastic Tube Specification

SSOP 5.3mm (.208") antistatic tube.

| Tube Specification |            |             |             |                |
|--------------------|------------|-------------|-------------|----------------|
| Package            | Tube Width | Tube Height | Tube Length | Units per Tube |
| SSOP 28            | 10.6       | 4 mm        | 20"         | 47             |

**Table 15: Plastic Tube Specification**

### 33. Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

| Tape and Reel Specification |            |                 |            |               |                |
|-----------------------------|------------|-----------------|------------|---------------|----------------|
| Package                     | Tape Width | Component Pitch | Hole Pitch | Reel Diameter | Units per Reel |
| SSOP 28                     | 24 mm      | 12 mm           | 4 mm       | 13"           | 2000           |

**Table 16: Carrier Tape and Reel Specification**

### 34. Ordering Information

| Ordering part number | Description                                                                                    |
|----------------------|------------------------------------------------------------------------------------------------|
| CC400-STB2           | CC400 8inch wafer, SSOP28 package, standard leaded assembly, tubes with 47 pcs per tube        |
| CC400-STR2           | CC400 8inch wafer, SSOP28 package, standard leaded assembly, T&R with 2000 pcs per reel        |
| CC400-RTB2           | CC400 8inch wafer, SSOP28 package, RoHS compliant Pb-free assembly, tubes with 47 pcs per tube |
| CC400-RTR2           | CC400 8inch wafer, SSOP28 package, RoHS compliant Pb-free assembly, T&R with 2000 pcs per reel |
| CC400DK              | CC400 Development Kit                                                                          |
| CC400SK              | CC400 Sample Kit ( 5 pcs.)                                                                     |

**Table 17: Ordering Information**

## 35. General Information

### 35.1. Document History

| Revision | Date       | Description/Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3.2      | 2005-05-25 | Updated the following performance figures: <ul style="list-style-type: none"> <li>• Power Down current</li> <li>• Receive current</li> <li>• Transmit current</li> <li>• Sensitivity</li> <li>• LO leakage</li> </ul> New varactor component (PB-free) added<br>Soldering information updated<br>New ordering information added<br>Document history added from revision 3.2 of the data sheet<br>Product Status Definitions added<br>Disclaimer updated<br>Address Information updated |

**Table 18: Document History**

### 35.2. Product Status Definitions

| Data Sheet Identification | Product Status                           | Definition                                                                                                                                                                                                                                  |
|---------------------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance Information       | Planned or Under Development             | This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.                                                                                                         |
| Preliminary               | Engineering Samples and First Production | This data sheet contains preliminary data, and supplementary data will be published at a later date. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| No Identification Noted   | Full Production                          | This data sheet contains the final specifications. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                   |
| Obsolete                  | Not In Production                        | This data sheet contains specifications on a product that has been discontinued by Chipcon. The data sheet is printed for reference information only.                                                                                       |

**Table 19: Product Status Definitions**

### 35.3. Disclaimer

Chipcon AS believes the information contained herein is correct and accurate at the time of this printing. However, Chipcon AS reserves the right to make changes to this product without notice. Chipcon AS does not assume any responsibility for the use of the described product.; neither does it convey any license under its patent rights, or the rights of others. The latest updates are available at the Chipcon website or by contacting Chipcon directly.

As far as possible, major changes of product specifications and functionality, will be stated in product specific Errata Notes published at the Chipcon website. Customers are encouraged to sign up to the Developers Newsletter for the most recent updates on products and support tools.

When a product is discontinued this will be done according to Chipcon's procedure for obsolete products as described in Chipcon's Quality Manual. This includes informing about last-time-buy options. The Quality Manual can be downloaded from Chipcon's website.

Compliance with regulations is dependent on complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

#### **35.4. Trademarks**

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All other trademarks, registered trademarks and product names are the sole property of their respective owners.

#### **35.5. Life Support Policy**

This Chipcon product is not designed for use in life support appliances, devices, or other systems where malfunction can reasonably be expected to result in significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Chipcon AS customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Chipcon AS for any damages resulting from any improper use or sale.