System Supervisory Voltage Reset with Watchdog and Manual Reset

HALOGEN FREE LEAD FREE™ RoHS Compliance

FEATURES

- **Automatically restarts microprocessor after Power failure**
- **Monitors pushbutton for external override**
- **Accurate under voltage system monitoring**
- **Brownout detection system reset for use with 3.0, 3.3, and 5.0 volt systems**
- **Pin and function compatible with the MAX823/24/25 products**
- **Operating Range from -40°C to +85°C**
- **Available in TSOT-23 5-lead and SC-70 packages**

For Ordering Information details, see page 13.

APPLICATIONS

- **Microprocessor and Microcontroller based systems**
- **Intelligent Instruments**
- **Control Systems**
- **Critical µP Monitors**
- **Portable Equipment**

DESCRIPTION

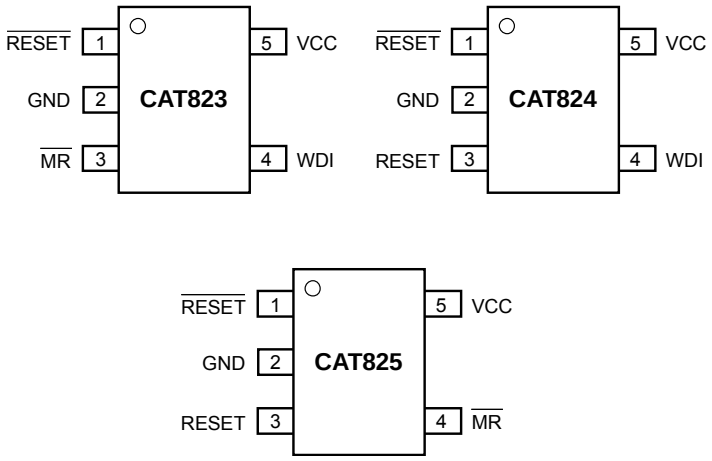
The CAT823, CAT824, and CAT825 provide basic reset and monitoring functions for the electronic systems. Each device monitors the system voltage and maintains a reset output until that voltage reaches the device's specified trip value and then maintains the reset output active condition until the device's internal timer, after a minimum timer of 140ms; to allow the systems power supply to stabilize.

The CAT823 and CAT824 also have a watchdog input which can be used to monitor a system signal and cause a reset to be issued if the signal fails to change state prior to a timeout condition.

The CAT823 and CAT825 also provide a manual reset input which can be used to initiate reset if pulled low. This input can be directly attached to a push-button or a processor signal.

PIN CONFIGURATION

TSOT-23 5-Lead
SC-70 5-Lead

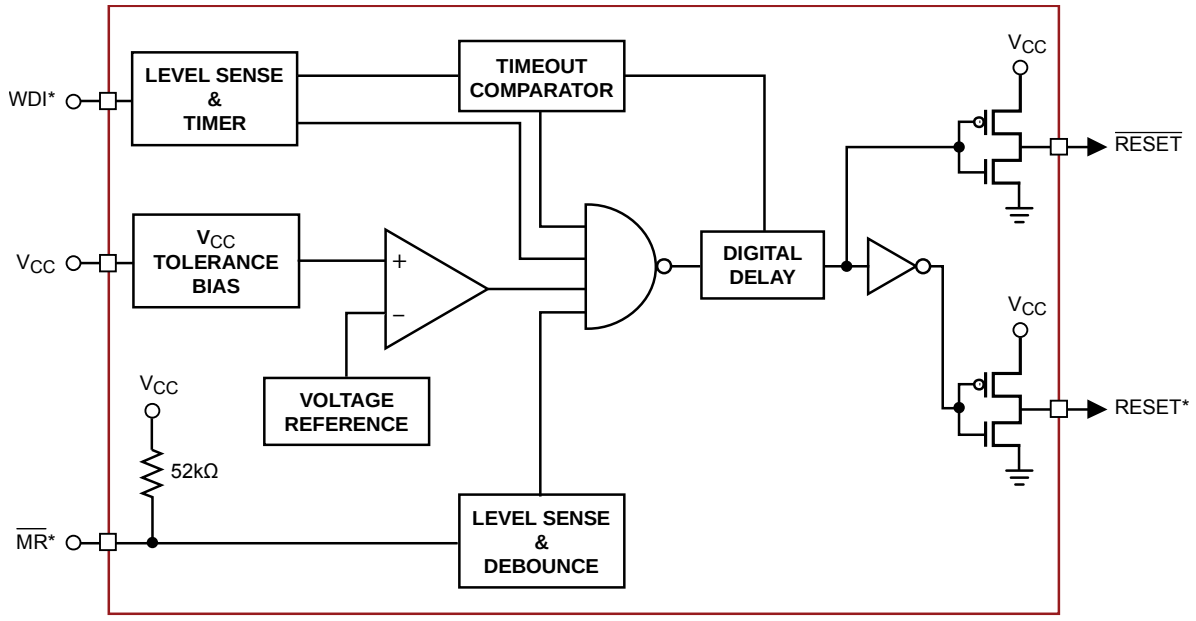


PIN FUNCTIONS

Pin Name	Function
$\overline{\text{RESET}}$	CMOS Push-Pull Active Low Reset Output
GND	Ground
$\overline{\text{MR}}$	Manual Reset input – Pulled high Internally by a 52kΩ resistor designed to be driven low by a mechanical pushbutton, open drain output or CMOS output.
RESET	CMOS Push-Pull Active High Reset Output
WDI	Watchdog Timer Input – Designed to be driven by a processor output or can be disabled by tri-stating or leaving open.
V_{CC}	Power Supply

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BLOCK DIAGRAM



* Functions Available by Device

Device	$\overline{\text{RESET}}$	RESET	$\overline{\text{MR}}$	WDI
CAT823	x		x	x
CAT824	x	x		x
CAT825	x	x	x	

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ABSOLUTE MAXIMUM RATINGS(1)

Parameters	Ratings	Units
Supply Voltage	6	V
All other pins	-0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}	20	mA
Output Current RST, $\overline{RST}$	20	mA
Continuous Power Dissipations (T_A = +70ºC)		
SC-70 5-lead (derate 3.1mW/ºC above +70ºC)	247	mW
TSOT-23 5-lead (derate 7.1mW/ºC above +70ºC)	571	mW
Storage Temperature	-65 to 150	ºC
Operating Ambient Temperature	-40 to +85	ºC
Lead Soldering (10 seconds max)	+300	ºC
ESD Rating: Low Voltage Pins		
Human Body Model	2000	V
Machine Model	200	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Range	Units
V_{CC} (T_A = 0ºC to +70ºC)	1.0 to 5.5	V
V_{CC} (T_A = -40ºC to +85ºC)	1.2 to 5.5	V
All Other Pins	-0.1 to (V_{CC} + 0.1)	V
Ambient Temperature	-40 to +85	ºC

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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ELECTRICAL OPERATING CHARACTERISTICS

DC Characteristics: V_{CC} = 3.0V to 5.5V for L/M versions; V_{CC} = 2.0V to 3.6V for the R/S/T/Y/Z version, -40ºC ≤ T_A ≤ +85ºC unless otherwise noted. Typical Values at T_A = 25ºC and V_{CC} = 5V for L/M versions; V_{CC} = 3.3V for the T/S versions; V_{CC} = 3.0V for the R version; and V_{CC} = 2.5V for the Y/Z versions.(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	CAT823 (L/M Versions) CAT824 (L/M Versions)		6	17	µA
		CAT823 (R/S/T/Y/Z Versions) CAT824 (R/S/T/Y/Z Versions)		4	12	µA
		CAT825 (L/M Versions)		3	8	µA
		CAT825 (R/S/T/Y/Z Versions)		2	6	µA
V_{RST}	Reset Threshold	CAT82_L at -40ºC ≤ T_A ≤ +85ºC	4.50	4.63	4.75	V
		CAT82_M at -40ºC ≤ T_A ≤ +85ºC	4.25	4.38	4.50	V
		CAT82_T at -40ºC ≤ T_A ≤ +85ºC	3.00	3.08	3.15	V
		CAT82_S at -40ºC ≤ T_A ≤ +85ºC	2.85	2.93	3.00	V
		CAT82_R at -40ºC ≤ T_A ≤ +85ºC	2.55	2.63	2.70	V
		CAT82_Z at -40ºC ≤ T_A ≤ +85ºC	2.25	2.32	2.38	V
		CAT82_Y at -40ºC ≤ T_A ≤ +85ºC	2.13	2.19	2.25	V
	Reset Threshold Tempco			40		ppm/ºC
	Reset Threshold Hysteresis	CAT82_L/M		10		mV
		CAT82_R/S/T/Y/Z		5		mV
t_{RD}	V_{CC} to Reset Delay(2)	V_{CC} = V_{TH} to (V_{TH} - 100mV)		20		µs
t_{RP}	Reset Active Timeout Period		140	200	400	ms
V_{OH}	$\overline{\text{RESET}}$ Output High Voltage	CAT82_L/M, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = -120µA	V_{CC} - 1.5V			V
		CAT82_T/S/R/Z/Y, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = -30µA	0.8 x V_{CC}			
V_{OL}	$\overline{\text{RESET}}$ Output Low Voltage	CAT82_L/M, V_{CC} = $V_{RST\ min}$, I_{SINK} = 3.2mA			0.4	
		CAT82_T/S/R/Z/Y, V_{CC} = $V_{RST\ min}$, I_{SINK} = 1.2mA			0.3	
		T_A = 0ºC to +70ºC, V_{CC} = 1V, V_{CC} falling, I_{SINK} = 50µA			0.3	
		T_A = T_{MIN} to T_{MAX}, V_{CC} = 1.2V, V_{CC} falling, I_{SINK} = 100µA			0.3	
I_{SOURCE}	$\overline{\text{RESET}}$ Output Short-Circuit Current	CAT82_L/M, Reset = 0V, V_{CC} = 5.5V			1.5	mA
		CAT82_L/M, Reset = 0V, V_{CC} = 3.6V			0.8	
V_{OH}	Reset Output Voltage	V_{CC} > 1.8V, I_{SOURCE} = -150µA	0.8 x V_{CC}			V
V_{OL}		CAT824L/M & CAT825L/M, V_{CC} = $V_{RST\ max}$, I_{SINK} = 3.2mA			0.4	
		CAT824R/S/T/Y/Z & CAT825R/S/T/Y/Z, V_{CC} = $V_{RST\ max}$, I_{SINK} = 1.2mA			0.3	

Notes:

(1) Over-temperature limits are guaranteed by design and not production tested.

(2) The RESET short-circuit current is the maximum pull-up current when reset is driven low by a bidirectional output.

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ELECTRICAL OPERATING CHARACTERISTICS (continued)

DC Characteristics: V_{CC} = 3.0V to 5.5V for L/M versions; V_{CC} = 2.0V to 3.6V for the R/S/T/Y/Z version, -40ºC ≤ T_A ≤ +85ºC unless otherwise noted. Typical Values at T_A = 25ºC and V_{CC} = 5V for L/M versions; V_{CC} = 3.3V for the T/S versions; V_{CC} = 3.0V for the R version; and V_{CC} = 2.5V for the Y/Z versions.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
WATCHDOG INPUT (CAT823 & CAT824)						
t_{WD}	Watchdog Timeout Period		1.12	1.60	3.20	s
t_{WDI}	WDI Pulse Width	V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}	50			ns
V_{IL}	WDI Input Voltage[3]				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
	WDI Input Current[4]	WDI = V_{CC}, Time Average		120	160	µA
		WDI = 0V, Time Average	-20	-15		
MANUAL RESET INPUT(CAT823 & CAT825)						
V_{IL}	$\overline{MR}$ Input Voltage				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
t_{PB}	$\overline{MR}$ Pulse Width		1			µs
t_{PDLY}	$\overline{MR}$ low to Reset Delay				5	µs
	$\overline{MR}$ Noise Immunity	Pulse Width with No Reset		100		ns
	$\overline{MR}$ Pullup Resistance (internal)		35	52	75	kΩ

Notes:

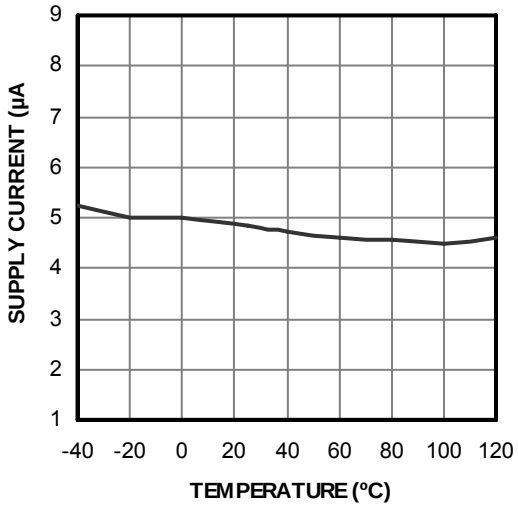
(3) WDI is internally serviced within the watchdog period if WDI is left open.

(4) The WDI input current is specified as an average input current when the WDI input is driven high or low. The WDI input if connected to a three-stated output device can be disabled in the tristate mode as long as the leakage current is less than 10µA and a maximum capacitance of less than 200pF. To clock the WDI input in the active mode the drive device must be able to source or sink at least 200µA when active.

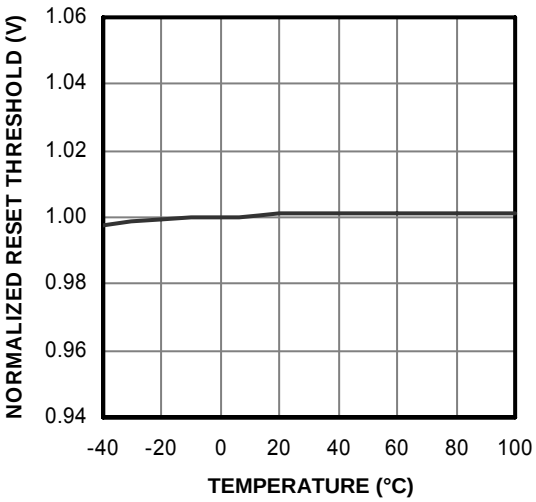
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TYPICAL ELECTRICAL OPERATING CHARACTERISTICS TABLES

V_{CC} Supply Current vs. Temperature



Normalized Reset Threshold Voltage vs. Temperature



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FUNCTIONAL DESCRIPTION

PROCESSOR RESET

The CAT823-825 detect supply voltage (V_{CC}) conditions that are below the specified voltage trip value (V_{RST}) and provide a reset output to maintain correct system operation. On power-up, $\overline{\text{RESET}}$ (and RESET if available) are kept active for a minimum delay t_{RP} of 140ms after the supply voltage (V_{CC}) rises above V_{RST} to allow the power supply and processor to stabilize. When V_{CC} drops below the voltage trip value (V_{RST}), the reset output signals $\overline{\text{RESET}}$ (and RESET) are pulled active. $\overline{\text{RESET}}$ (and RESET if available) is specifically designed to provide the reset input signals for processors. This provides reliable and consistent operation as power is turned on, off or during brownout conditions by maintaining the processor operation in known conditions.

MANUAL RESET

The CAT823 and CAT825 each have a Manual Reset ($\overline{\text{MR}}$) input to allow for alternative control of the reset outputs. The $\overline{\text{MR}}$ input is designed for direct connection to a pushbutton (see Figure 1). The $\overline{\text{MR}}$ input is internally pulled up by 52kΩ resistor and must be pulled low to cause the reset outputs to go active. Internally, this input is debounced and timed such that $\overline{\text{RESET}}$ (and RESET) signals of at least 140ms minimum will be generated. The min 140ms t_{RP} delay commences as the Manual Reset input is released from the low level. (see Figure 2)

Figure 1. Pushbutton RESET

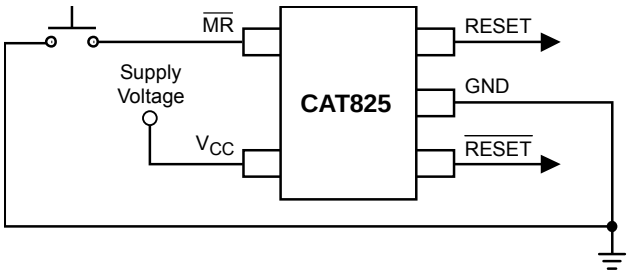
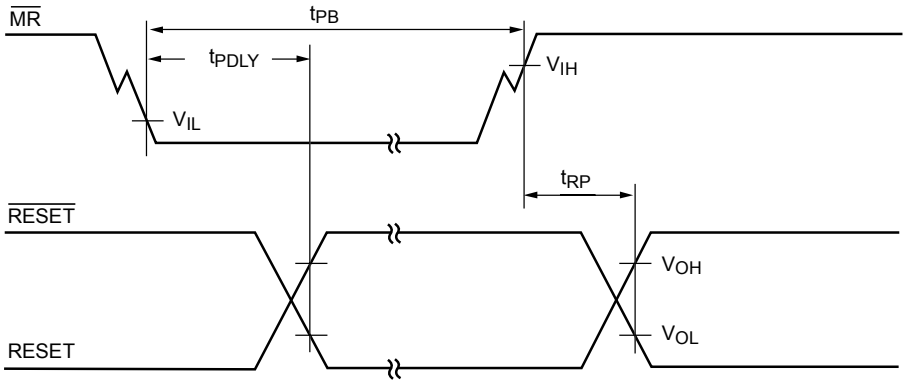


Figure 2. Timing Diagram – Pushbutton RESET



WATCHDOG TIMER

The CAT823 and CAT824 provide a Watchdog input (WDI). The watchdog timer function forces $\overline{\text{RESET}}$ (and RESET in the CAT824) signals active when the WDI input does not have a transition from low-to-high or high-to-low within 1.12 seconds. Timeout of the watchdog starts when $\overline{\text{RESET}}$ (RESET on the CAT824) becomes inactive. If a transition occurs on the WDI input pin prior to the watchdog time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the reset output(s) will go active for t_{RP} and once released will repeat the watchdog timeout process.

Figure 3 below shows a typical implementation of a watchdog function. Any processor signal that repeats dependant on the normal operation of the processor or directed by the software operating on the processor can be used to strobe the watchdog input. The most reliable is a dedicated I/O output transitioned by a specific software instruction.

The watchdog can be disabled by floating (or tri-stating) the WDI input (see Figure 4). If the watchdog is disabled the WDI pin will be pulled low for the first 7/8th's of the watchdog period (t_{WD}) and pulled high for the last 1/8th of the watchdog period. This pulling low of the WDI input and then high is used to detect an open or tri-state condition and will continue to repeat until the WDI input is driven high or low.

For most efficient operation of devices with the watchdog function the WDI input should be held low the majority of the time and only strobed high as required to reset the watchdog timer.

Figure 3. Watchdog Timer

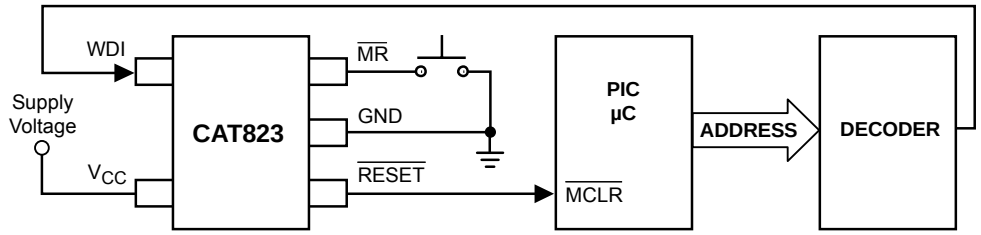
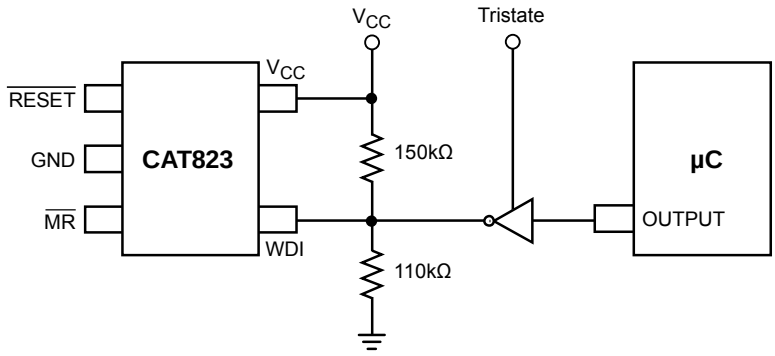


Figure 4. Watchdog Disable Circuit



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Figure 5. Timing Diagram – Strobe Input

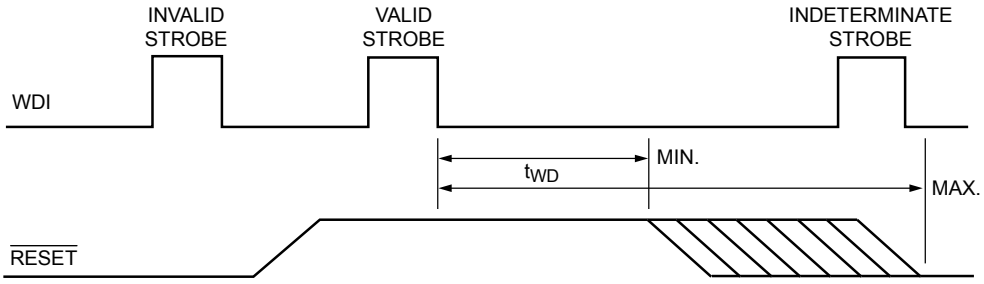


Figure 6. Timing Diagram – Power Down

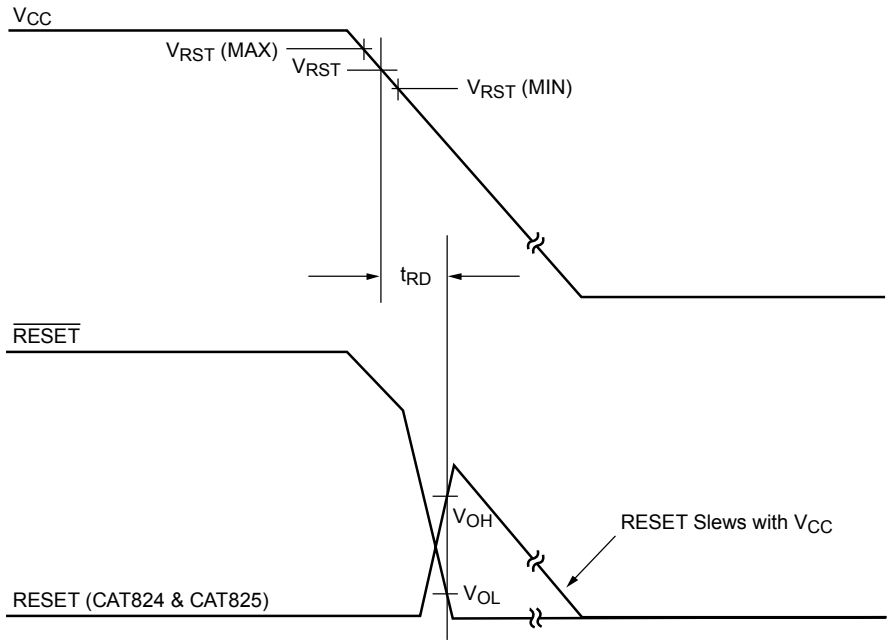
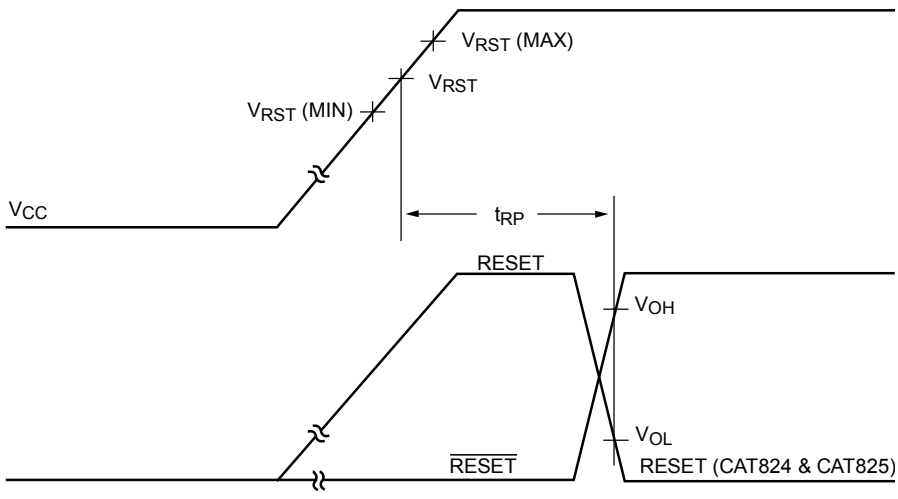


Figure 7. Timing Diagram – Power Up



APPLICATION NOTES

µP's with Bidirectional Reset Pins

The $\overline{\text{RESET}}$ output can be pulled low by processors like the 68HC11 allowing for a system reset issued by the processor. The maximum pullup current that can be sourced by the CAT82_L/M is 1.5mA (and by the CAT82_T/R/S/Z/Y is 800µA) allowing the processor to pull the output low even when the CAT82x is pulling it high.

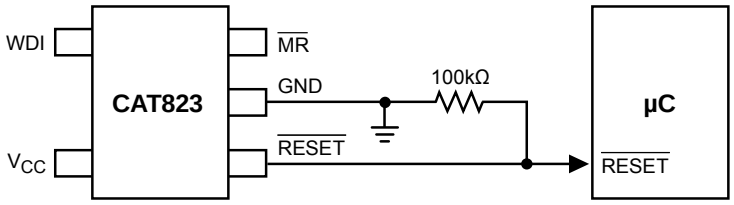
Power Transients

Generally short duration negative-going transients of less than 2µs on the power supply at V_{RST} minimum will not cause a reset condition. However the lower the voltage of the transient the shorter the required time to cause a reset output. These issues can usually be remedied by the proper location of bypass capacitance on the circuit board.

OUTPUT VALID CONDITIONS

The $\overline{\text{RESET}}$ output uses a push-pull output which can maintain a valid output down to a V_{CC} of 1.0 volts. To sink current below 0.8V a resistor can be connected from $\overline{\text{RESET}}$ to Ground (see Figure 8.) This arrangement will maintain a valid value on the $\overline{\text{RESET}}$ output during both power up and down but will draw current when the $\overline{\text{RESET}}$ output is in the high state. A resistor value of about 100kΩ should be adequate in most situations to maintain a low condition valid output down to V_{CC} equal to 0V.

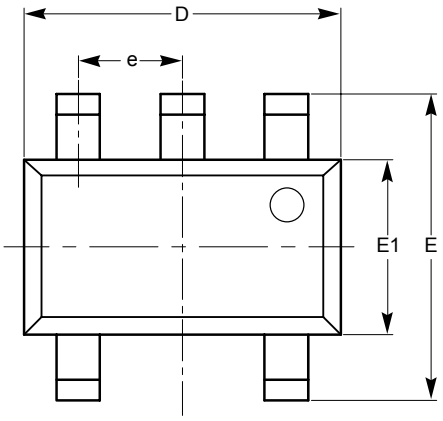
Figure 8. $\overline{\text{RESET}}$ Valid to 0 Volts V_{CC}



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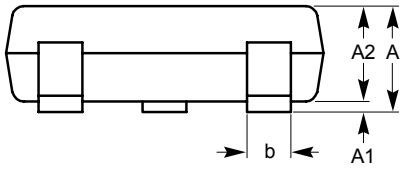
PACKAGE OUTLINE DRAWING

TSOT-23 5-Lead (TD)[1][2]

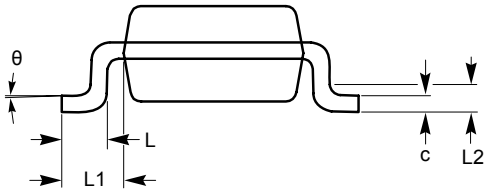


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 TYP	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0°		8°



SIDE VIEW

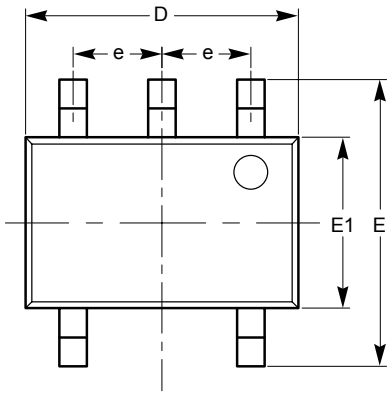


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

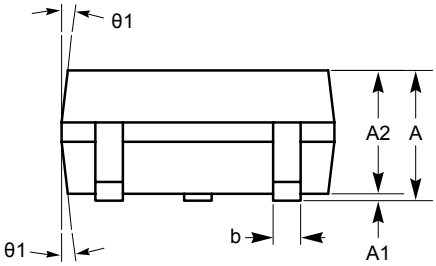
Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

SC-70 5-Lead (SD)(1)(2)

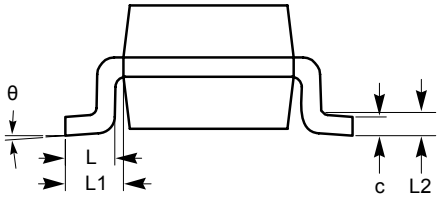


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



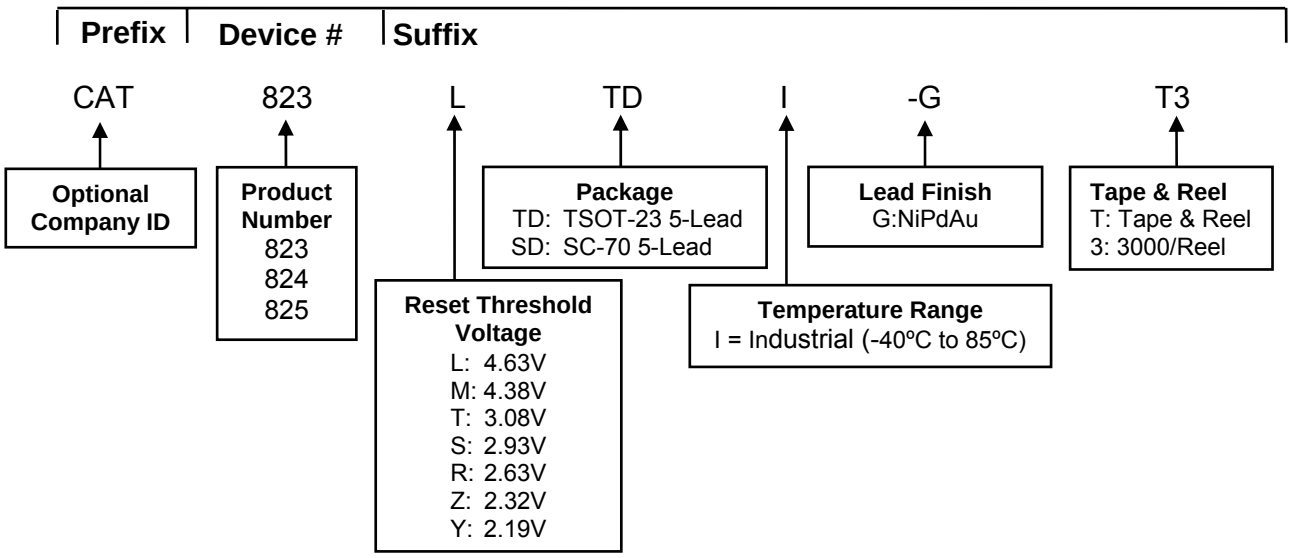
END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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EXAMPLE OF ORDERING INFORMATION



TOP MARKING INFORMATION (For all Thresholds)

NiPdAu Finish (-G)

Device #	Package		Top Marking
CAT823	TSOT-23	SC-70	RG
CAT824	TSOT-23	SC-70	TB
CAT825	TSOT-23	SC-70	TD

ORDERING PART NUMBER

CAT823LTDI-G	CAT824LTDI-G(4)	CAT825LTDI-G
CAT823MTDI-G	CAT824MTDI-G(4)	CAT825MTDI-G
CAT823TTDI-G	CAT824TTDI-G(4)	CAT825TTDI-G
CAT823STDI-G	CAT824TSDI-G(4)	CAT825STDI-G
CAT823RTDI-G	CAT824RTDI-G(4)	CAT825RTDI-G
CAT823ZTDI-G	CAT824ZTDI-G(4)	CAT825ZTDI-G
CAT823YTDI-G	CAT824YTDI-G(4)	CAT825YTDI-G
CAT823LSDI-G	CAT824LSDI-G(4)	CAT825LSDI-G
CAT823MSDI-G	CAT824MSDI-G(4)	CAT825MSDI-G
CAT823TSDI-G	CAT824TSDI-G(4)	CAT825TSDI-G
CAT823SSDI-G	CAT824SSDI-G(4)	CAT825SDI-G
CAT823RSDI-G	CAT824RSDI-G(4)	CAT825RSDI-G
CAT823ZSDI-G	CAT824ZSDI-G(4)	CAT825ZSDI-G
CAT823YSDI-G	CAT824YSDI-G(4)	CAT825YSDI-G

Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

(3) This device used in the above example is a CAT823LTDI -GT3 (4.63V, TSOT-23 5-Lead, Industrial Temperature, NiPdAu, Tape & Reel)

(4) Contact factory for package availability.

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REVISION HISTORY

Date	Rev.	Reason
09/10/2007	A	Initial Release

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Catalyst Semiconductor, Inc.
Corporate Headquarters
2975 Stender Way
Santa Clara, CA 95054
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

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