



# CAT25C128/256

## 128K/256K-Bit SPI Serial CMOS EEPROM

### FEATURES

- 5 MHz SPI Compatible
- 1.8 to 5.5 Volt Operation
- Hardware and Software Protection
- Low Power CMOS Technology
- SPI Modes (0,0 & 1,1)
- Industrial and Automotive Temperature Ranges
- Self-Timed Write Cycle
- 64-Byte Page Write Buffer
- Block Write Protection
  - Protect 1/4, 1/2 or all of EEPROM Array
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- RoHS-compliant packages

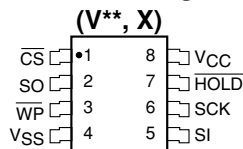
### DESCRIPTION

The CAT25C128/256 is a 128K/256K-Bit SPI Serial CMOS EEPROM internally organized as 16Kx8/32Kx8 bits. Catalyst's advanced CMOS Technology substantially reduces device power requirements. The CAT25C128/256 features a 64-byte page write buffer. The device operates via the SPI bus serial interface and is enabled through a Chip Select ( $\overline{CS}$ ). In addition to the Chip Select, the clock input (SCK), data in (SI) and data out (SO) are required to access the device.

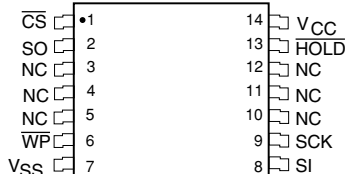
The  $\overline{HOLD}$  pin may be used to suspend any serial communication without resetting the serial sequence. The CAT25C128/256 is designed with software and hardware write protection features including Block Lock protection. The device is available in 8-pin DIP, 8-pin SOIC, 14-pin TSSOP and 20-pin TSSOP packages.

### PIN CONFIGURATION

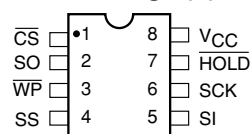
#### SOIC Package



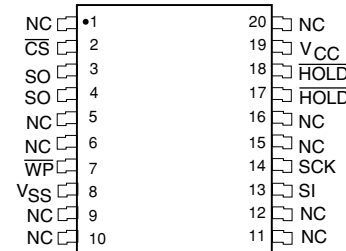
#### TSSOP Package (Y14)\*\*



#### DIP Package (L)



#### TSSOP Package (Y20)\*\*

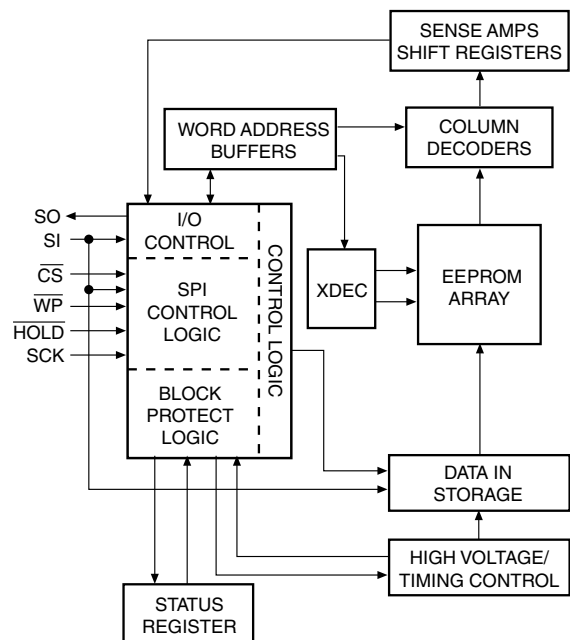


\*\*CAT25C128 only.

### PIN FUNCTIONS

| Pin Name          | Function              |
|-------------------|-----------------------|
| SO                | Serial data Output    |
| SCK               | Serial Clock          |
| $\overline{WP}$   | Write Protect         |
| V <sub>CC</sub>   | Power Supply          |
| V <sub>SS</sub>   | Ground                |
| $\overline{CS}$   | Chip Select           |
| SI                | Serial Data Input     |
| $\overline{HOLD}$ | Suspends Serial Input |
| NC                | No Connect            |

### BLOCK DIAGRAM



For Ordering Information details, see page 11.

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias ..... -55°C to +125°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on any Pin with  
   Respect to  $V_{SS}^{(1)}$  ..... -2.0V to  $V_{CC} + 2.0V$   
 $V_{CC}$  with Respect to  $V_{SS}$  ..... -2.0V to +7.0V  
 Package Power Dissipation  
   Capability ( $T_a = 25^\circ\text{C}$ ) ..... 1.0W  
 Lead Soldering Temperature (10 secs) ..... 300°C  
 Output Short Circuit Current<sup>(2)</sup> ..... 100 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

| Symbol             | Parameter          | Min.    | Max. | Units       |
|--------------------|--------------------|---------|------|-------------|
| $N_{END}^{(3)}$    | Endurance          | 100,000 |      | Cycles/Byte |
| $T_{DR}^{(3)}$     | Data Retention     | 100     |      | Years       |
| $V_{ZAP}^{(3)}$    | ESD Susceptibility | 2000    |      | Volts       |
| $I_{LTH}^{(3)(4)}$ | Latch-Up           | 100     |      | mA          |

**D.C. OPERATING CHARACTERISTICS**

$V_{CC} = +1.8V$  to  $+5.5V$ , unless otherwise specified.

| Symbol         | Parameter                              | Limits              |      |                     | Units   | Test Conditions                                                          |
|----------------|----------------------------------------|---------------------|------|---------------------|---------|--------------------------------------------------------------------------|
|                |                                        | Min.                | Typ. | Max.                |         |                                                                          |
| $I_{CC1}$      | Power Supply Current (Operating Write) |                     |      | 10                  | mA      | $V_{CC} = 5V$ @ 5MHz<br>SO=open; CS= $V_{SS}$                            |
| $I_{CC2}$      | Power Supply Current (Operating Read)  |                     |      | 2                   | mA      | $V_{CC} = 5.0V$<br>$F_{CLK} = 5MHz$                                      |
| $I_{SB}^{(5)}$ | Power Supply Current (Standby)         |                     |      | 1                   | $\mu A$ | $\overline{CS} = V_{CC}$<br>$V_{IN} = V_{SS}$ or $V_{CC}$                |
| $I_{LI}$       | Input Leakage Current                  |                     |      | 2                   | $\mu A$ |                                                                          |
| $I_{LO}$       | Output Leakage Current                 |                     |      | 3                   | $\mu A$ | $V_{OUT} = 0V$ to $V_{CC}$ ,<br>CS = 0V                                  |
| $V_{IL}^{(3)}$ | Input Low Voltage                      | -1                  |      | $V_{CC} \times 0.3$ | V       |                                                                          |
| $V_{IH}^{(3)}$ | Input High Voltage                     | $V_{CC} \times 0.7$ |      | $V_{CC} + 0.5$      | V       |                                                                          |
| $V_{OL1}$      | Output Low Voltage                     |                     |      | 0.4                 | V       | $4.5V \leq V_{CC} < 5.5V$<br>$I_{OL} = 3.0mA$<br>$I_{OH} = -1.6mA$       |
| $V_{OH1}$      | Output High Voltage                    | $V_{CC} - 0.8$      |      |                     | V       |                                                                          |
| $V_{OL2}$      | Output Low Voltage                     |                     |      | 0.2                 | V       | $1.8V \leq V_{CC} < 2.7V$<br>$I_{OL} = 150\mu A$<br>$I_{OH} = -100\mu A$ |
| $V_{OH2}$      | Output High Voltage                    | $V_{CC} - 0.2$      |      |                     | V       |                                                                          |

Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is  $V_{CC} + 0.5V$ , which may overshoot to  $V_{CC} + 2.0V$  for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to  $V_{CC} + 1V$ .
- (5) Maximum standby current ( $I_{SB}$ ) = 10 $\mu A$  for the Automotive and Extended Automotive temperature range.

**PIN CAPACITANCE (1)**

Applicable over recommended operating range from  $T_A=25^{\circ}\text{C}$ ,  $f=1.0\text{ MHz}$ ,  $V_{CC}=\pm 5.0\text{V}$  (unless otherwise noted).

| Symbol    | Test Conditions                                                                      | Max. | Units | Conditions          |
|-----------|--------------------------------------------------------------------------------------|------|-------|---------------------|
| $C_{OUT}$ | Output Capacitance (SO)                                                              | 8    | pF    | $V_{OUT}=0\text{V}$ |
| $C_{IN}$  | Input Capacitance ( $\overline{CS}$ , SCK, SI, $\overline{WP}$ , $\overline{HOLD}$ ) | 6    | pF    | $V_{IN}=0\text{V}$  |

**A.C. CHARACTERISTICS (CAT25C128)**

| SYMBOL                         | PARAMETER                                 | Limits                         |      |                                |      |                                |      | UNITS | Test Conditions       |
|--------------------------------|-------------------------------------------|--------------------------------|------|--------------------------------|------|--------------------------------|------|-------|-----------------------|
|                                |                                           | V <sub>CC</sub> =<br>1.8V-5.5V |      | V <sub>CC</sub> =<br>2.5V-5.5V |      | V <sub>CC</sub> =<br>4.5V-5.5V |      |       |                       |
|                                |                                           | Min.                           | Max. | Min.                           | Max. | Min.                           | Max. |       |                       |
| t <sub>SU</sub>                | Data Setup Time                           | 100                            |      | 70                             |      | 35                             |      | ns    | C <sub>L</sub> = 50pF |
| t <sub>H</sub>                 | Data Hold Time                            | 100                            |      | 70                             |      | 35                             |      | ns    |                       |
| t <sub>WH</sub>                | SCK High Time                             | 250                            |      | 150                            |      | 80                             |      | ns    |                       |
| t <sub>WL</sub>                | SCK Low Time                              | 250                            |      | 150                            |      | 80                             |      | ns    |                       |
| f <sub>SCK</sub>               | Clock Frequency                           | DC                             | 1    | DC                             | 3    | DC                             | 5    | MHz   |                       |
| t <sub>LZ</sub>                | $\overline{\text{HOLD}}$ to Output Low Z  |                                | 50   |                                | 50   |                                | 50   | ns    |                       |
| t <sub>RI</sub> <sup>(1)</sup> | Input Rise Time                           |                                | 2    |                                | 2    |                                | 2    | μs    |                       |
| t <sub>FI</sub> <sup>(1)</sup> | Input Fall Time                           |                                | 2    |                                | 2    |                                | 2    | μs    |                       |
| t <sub>HD</sub>                | $\overline{\text{HOLD}}$ Setup Time       | 250                            |      | 250                            |      | 40                             |      | ns    |                       |
| t <sub>CD</sub>                | $\overline{\text{HOLD}}$ Hold Time        | 250                            |      | 250                            |      | 40                             |      | ns    |                       |
| t <sub>WC</sub>                | Write Cycle Time                          |                                | 10   |                                | 10   |                                | 5    | ms    |                       |
| t <sub>V</sub>                 | Output Valid from Clock Low               |                                | 250  |                                | 250  |                                | 80   | ns    |                       |
| t <sub>HO</sub>                | Output Hold Time                          | 0                              |      | 0                              |      | 0                              |      | ns    |                       |
| t <sub>DIS</sub>               | Output Disable Time                       |                                | 250  |                                | 250  |                                | 100  | ns    |                       |
| t <sub>HZ</sub>                | $\overline{\text{HOLD}}$ to Output High Z |                                | 150  |                                | 150  |                                | 50   | ns    |                       |
| t <sub>CS</sub>                | $\overline{\text{CS}}$ High Time          | 1000                           |      | 250                            |      | 200                            |      | ns    |                       |
| t <sub>CSS</sub>               | $\overline{\text{CS}}$ Setup Time         | 1000                           |      | 250                            |      | 100                            |      | ns    |                       |
| t <sub>CSH</sub>               | $\overline{\text{CS}}$ Hold Time          | 500                            |      | 250                            |      | 100                            |      | ns    |                       |
| t <sub>WPS</sub>               | $\overline{\text{WP}}$ Setup Time         | 50                             |      | 50                             |      | 50                             |      | ns    |                       |
| t <sub>WPH</sub>               | $\overline{\text{WP}}$ Hold Time          | 50                             |      | 50                             |      | 50                             |      | ns    |                       |

NOTE:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

## A.C. CHARACTERISTICS (CAT25C256)

| SYMBOL                         | PARAMETER                                 | Limits         |      |                 |      |                 |      |                |      | UNITS | Test Conditions       |
|--------------------------------|-------------------------------------------|----------------|------|-----------------|------|-----------------|------|----------------|------|-------|-----------------------|
|                                |                                           | Vcc= 1.8V-5.5V |      | Vcc = 2.5V-5.5V |      | Vcc = 2.7V-5.5V |      | VCC= 4.5V-5.5V |      |       |                       |
|                                |                                           | Min.           | Max. | Min.            | Max. | Min.            | Max. | Min.           | Max. |       |                       |
| t <sub>SU</sub>                | Data Setup Time                           | 500            |      | 100             |      | 70              |      | 35             |      | ns    | C <sub>L</sub> = 50pF |
| t <sub>H</sub>                 | Data Hold Time                            | 500            |      | 100             |      | 70              |      | 35             |      | ns    |                       |
| t <sub>WH</sub>                | SCK High Time                             | 2500           |      | 250             |      | 150             |      | 80             |      | ns    |                       |
| t <sub>WL</sub>                | SCK Low Time                              | 2500           |      | 250             |      | 150             |      | 80             |      | ns    |                       |
| f <sub>SCK</sub>               | Clock Frequency                           | DC             | 0.2  | DC              | 2.0  | DC              | 2.5  | DC             | 5    | MHz   |                       |
| t <sub>LZ</sub>                | $\overline{\text{HOLD}}$ to Output Low Z  |                | 100  |                 | 50   |                 | 50   |                | 50   | ns    |                       |
| t <sub>RI</sub> <sup>(3)</sup> | Input Rise Time                           |                | 2    |                 | 2    |                 | 2    |                | 2    | μs    |                       |
| t <sub>FI</sub> <sup>(3)</sup> | Input Fall Time                           |                | 2    |                 | 2    |                 | 2    |                | 2    | μs    |                       |
| t <sub>HD</sub>                | $\overline{\text{HOLD}}$ Setup Time       | 250            |      | 100             |      | 100             |      | 40             |      | ns    |                       |
| t <sub>CD</sub>                | $\overline{\text{HOLD}}$ Hold Time        | 250            |      | 100             |      | 100             |      | 40             |      | ns    |                       |
| t <sub>WC</sub>                | Write Cycle Time                          |                | 10   |                 | 10   |                 | 10   |                | 5    | ms    |                       |
| t <sub>V</sub>                 | Output Valid from Clock Low               |                | 250  |                 | 200  |                 | 200  |                | 80   | ns    |                       |
| t <sub>HO</sub>                | Output Hold Time                          | 0              |      | 0               |      | 0               |      | 0              |      | ns    |                       |
| t <sub>DIS</sub>               | Output Disable Time                       |                | 250  |                 | 200  |                 | 200  |                | 100  | ns    |                       |
| t <sub>HZ</sub>                | $\overline{\text{HOLD}}$ to Output High Z |                | 150  |                 | 100  |                 | 100  |                | 50   | ns    |                       |
| t <sub>CS</sub>                | $\overline{\text{CS}}$ High Time          | 100            |      | 100             |      | 100             |      | 100            |      | ns    |                       |
| t <sub>CSS</sub>               | $\overline{\text{CS}}$ Setup Time         | 100            |      | 100             |      | 100             |      | 100            |      | ns    |                       |
| t <sub>CSH</sub>               | $\overline{\text{CS}}$ Hold Time          | 100            |      | 100             |      | 100             |      | 100            |      | ns    |                       |
| t <sub>WPS</sub>               | $\overline{\text{WP}}$ Setup Time         | 50             |      | 50              |      | 50              |      | 50             |      | ns    |                       |
| t <sub>WPH</sub>               | $\overline{\text{WP}}$ Hold Time          | 50             |      | 50              |      | 50              |      | 50             |      | ns    |                       |

NOTE:

(3) This parameter is tested initially and after a design or process change that affects the parameter.

## FUNCTIONAL DESCRIPTION

The CAT25C128/256 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT25C128/256 to interface directly with many of today's popular microcontrollers. The CAT25C128/256 contains an 8-bit instruction register. (The instruction set and the operation codes are detailed in the instruction set table)

After the device is selected with  $\overline{CS}$  going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

## PIN DESCRIPTION

### SI: Serial Input

SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the 25C32/64. Input data is latched on the rising edge of the serial clock.

### SO: Serial Output

SO is the serial data output pin. This pin is used to transfer data out of the CAT25C128/256. During a read cycle, data is shifted out on the falling edge of the serial clock.

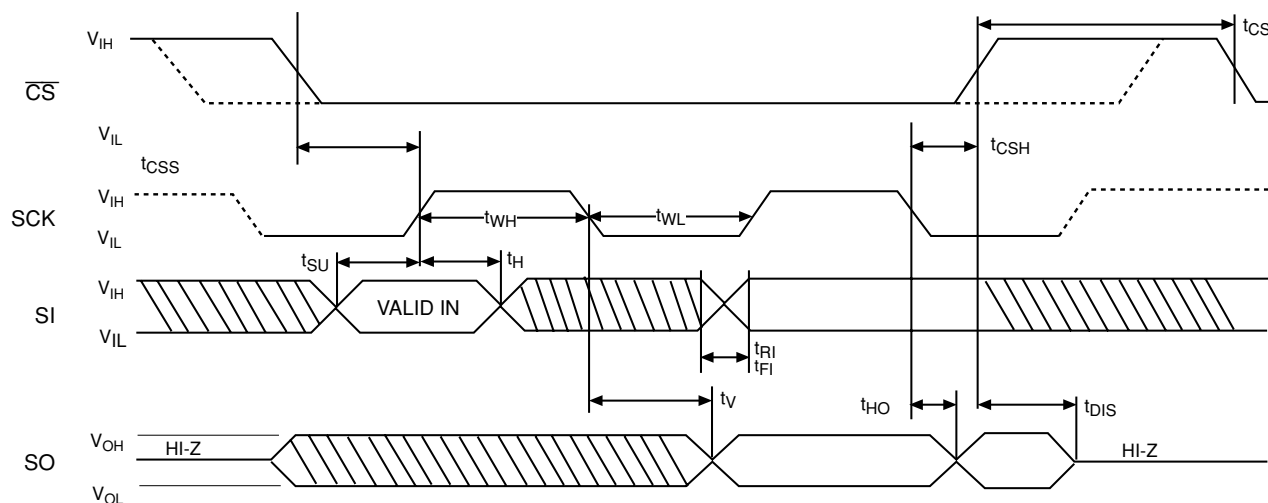
### SCK: Serial Clock

SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the CAT25C128/256. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

### $\overline{CS}$ : Chip Select

$\overline{CS}$  is the Chip select pin.  $\overline{CS}$  low enables the CAT25C128/256 and  $\overline{CS}$  high disables the CAT25C128/256.  $\overline{CS}$  high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway). The CAT25C128/256 draws ZERO current in the Standby mode. A high to low transition on  $\overline{CS}$  is required prior to any sequence being initiated. A low to high transition on  $\overline{CS}$  after a valid write sequence is what initiates an internal write cycle.

**Figure 1. Synchronous Data Timing**



Note: Dashed Line= mode (1, 1) — — — —

## INSTRUCTION SET

| Instruction | Opcode    | Operation                |
|-------------|-----------|--------------------------|
| WREN        | 0000 0110 | Enable Write Operations  |
| WRDI        | 0000 0100 | Disable Write Operations |
| RDSR        | 0000 0101 | Read Status Register     |
| WRSR        | 0000 0001 | Write Status Register    |
| READ        | 0000 0011 | Read Data from Memory    |
| WRITE       | 0000 0010 | Write Data to Memory     |

**WP: Write Protect**

WP is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When WP is tied low and the WPEN bit in the status register is set to "1", all write operations to the status register are inhibited. WP going low while CS is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, WP going low will have no effect on any write operation to the status register. The WP pin function is blocked when the WPEN bit is set to 0.

**HOLD: Hold**

The HOLD pin is used to pause transmission to the CAT25C128/256 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, HOLD must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, HOLD is brought high, while SCK is low. (HOLD should be held high any time this function is not being used.) HOLD may be tied high directly to V<sub>CC</sub> or tied to V<sub>CC</sub> through a resistor. Figure

9 illustrates hold timing sequence.

**STATUS REGISTER**

The Status Register indicates the status of the device.

The RDY (Ready) bit indicates whether the CAT25C128/256 is busy with a write operation. When set to 1 a write cycle is in progress and when set to 0 the device indicates it is ready. This bit is read only.

The WEL (Write Enable) bit indicates the status of the write enable latch. When set to 1, the device is in a Write Enable state and when set to 0 the device is in a Write Disable state. The WEL bit can only be set by the WREN instruction and can be reset by the WRDI instruction.

The BP0 and BP1 (Block Protect) bits indicate which blocks are currently protected. These bits are set by the user issuing the WRSR instruction. The user is allowed to protect quarter of the memory, half of the memory or the entire memory by setting these bits. Once protected the user may only read from the protected portion of the array. These bits are non-volatile.

**STATUS REGISTER**

|      |   |   |   |     |     |     |     |
|------|---|---|---|-----|-----|-----|-----|
| 7    | 6 | 5 | 4 | 3   | 2   | 1   | 0   |
| WPEN | X | X | X | BP1 | BP0 | WEL | RDY |

**BLOCK PROTECTION BITS**

| Status Register Bits |     | Array Address Protected                | Protection               |
|----------------------|-----|----------------------------------------|--------------------------|
| BP1                  | BP0 |                                        |                          |
| 0                    | 0   | None                                   | No Protection            |
| 0                    | 1   | 25C128: 3000-3FFF<br>25C256: 6000-7FFF | Quarter Array Protection |
| 1                    | 0   | 25C128: 2000-3FFF<br>25C256: 4000-7FFF | Half Array Protection    |
| 1                    | 1   | 25C128: 0000-3FFF<br>25C256: 0000-7FFF | Full Array Protection    |

**WRITE PROTECT ENABLE OPERATION**

| WPEN | WP   | WEL | Protected Blocks | Unprotected Blocks | Status Register |
|------|------|-----|------------------|--------------------|-----------------|
| 0    | X    | 0   | Protected        | Protected          | Protected       |
| 0    | X    | 1   | Protected        | Writable           | Writable        |
| 1    | Low  | 0   | Protected        | Protected          | Protected       |
| 1    | Low  | 1   | Protected        | Writable           | Protected       |
| X    | High | 0   | Protected        | Protected          | Protected       |
| X    | High | 1   | Protected        | Writable           | Writable        |

The WPEN (Write Protect Enable) is an enable bit for the  $\overline{WP}$  pin. The  $\overline{WP}$  pin and WPEN bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when  $\overline{WP}$  is low and WPEN bit is set to high. The user cannot write to the status register (including the block protect bits and the WPEN bit) and the block protected sections in the memory array when the chip is hardware write protected. Only the sections of the memory array that are not block protected can be written. Hardware write protection is disabled when either  $\overline{WP}$  pin is high or the WPEN bit is zero.

## DEVICE OPERATION

### Write Enable and Disable

The CAT25C128/256 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when  $V_{CC}$  is applied. WREN instruction will enable writes (set the latch) to the device. WRDI instruction will disable writes (reset the

latch) to the device. Disabling writes will protect the device against inadvertent writes.

### READ Sequence

The part is selected by pulling  $\overline{CS}$  low. The 8-bit read instruction is transmitted to the CAT25C128/256, followed by the 16-bit address (the three Most Significant Bit is don't care for 25C256 and four most significant bits are don't care for 25C128).

After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address (7FFFh for 25C256 and 3FFFh for 25C128) is reached, the address counter rolls over to 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by pulling the  $\overline{CS}$  high.

Figure 2. WREN Instruction Timing

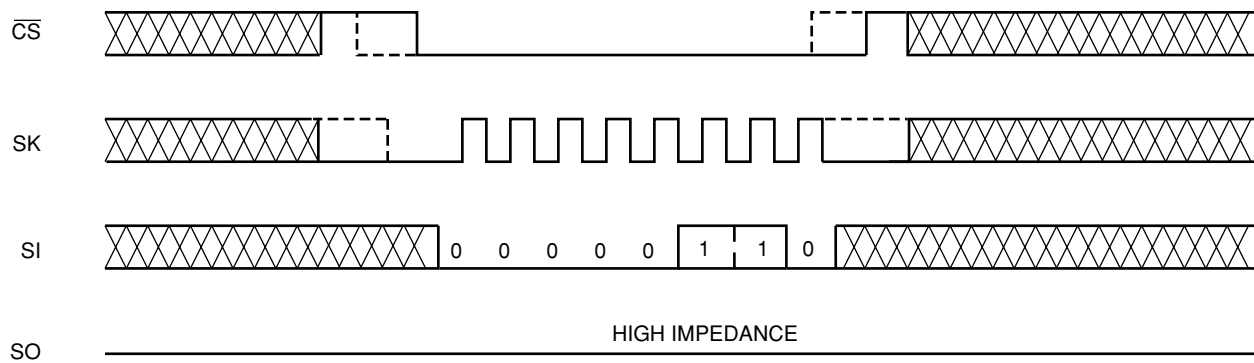
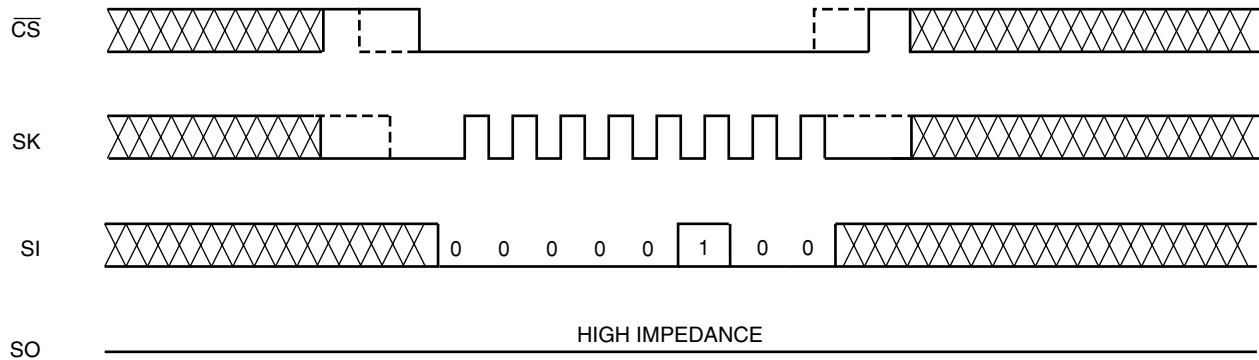


Figure 3. WRDI Instruction Timing



Note: Dashed Line= mode (1, 1) — — — —

To read the status register, RDSR instruction should be sent. The contents of the status register are shifted out on the SO line. The status register may be read at any time even during a write cycle. Read sequence is illustrated in Figure 4. Reading status register is illustrated in Figure 5.

### WRITE Sequence

The CAT25C128/256 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to CAT25C128/256. The device goes into Write enable state by pulling the  $\overline{CS}$  low and then clocking the WREN instruction into CAT25C128/256. The  $\overline{CS}$  must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without  $\overline{CS}$  being brought high, the data will not be written to the array because the write enable latch will not have been

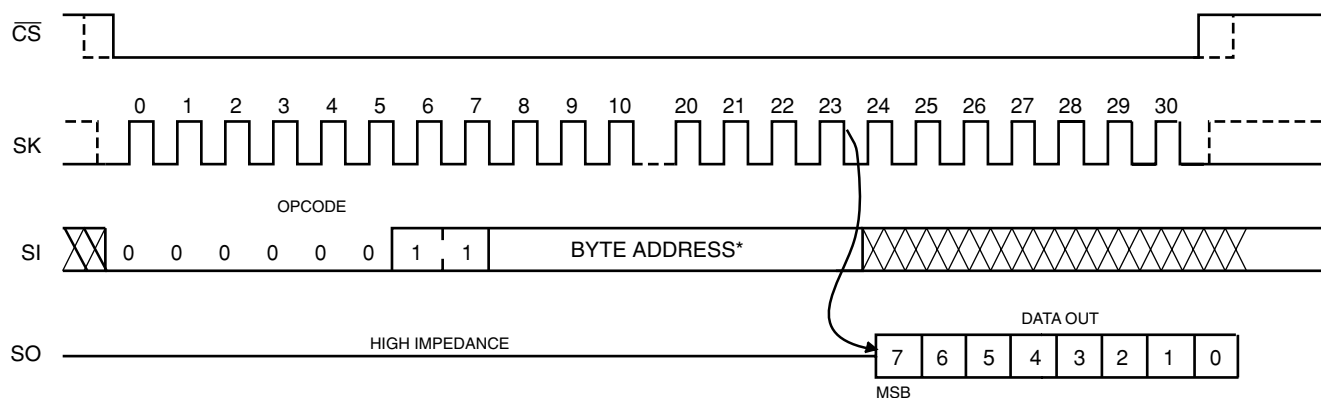
properly set. Also, for a successful write operation the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block protection level.

### Byte Write

Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the  $\overline{CS}$  low, issuing a write instruction via the SI line, followed by the 16-bit address (the three Most Significant Bits are don't care for 25C256 and four most significant bits are don't care for 25C128), and then the data to be written. Programming will start after the  $\overline{CS}$  is brought high. Figure 6 illustrates byte write sequence.

During an internal write cycle, all commands will be ignored except the RDSR (Read Status Register) instruction.

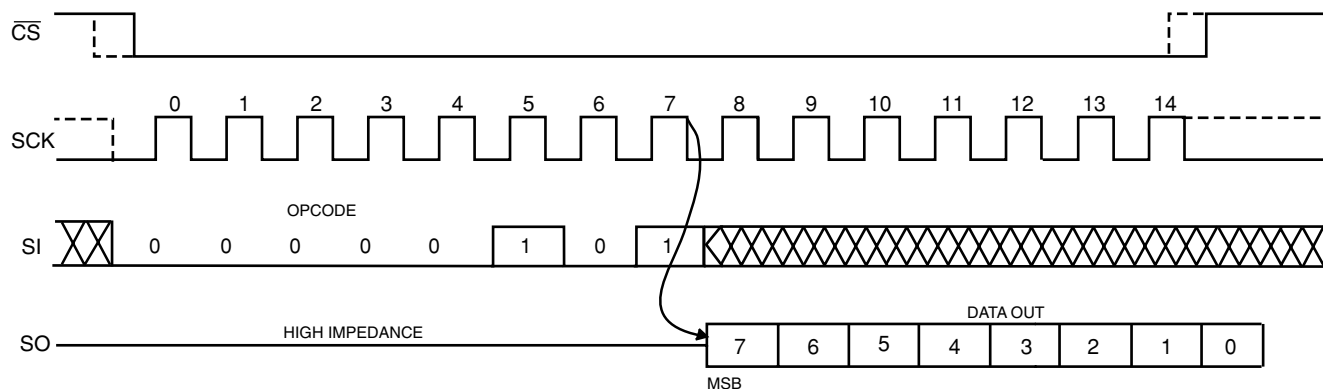
**Figure 4. Read Instruction Timing**



\*Please check the instruction set table for address

Note: Dashed Line= mode (1, 1) — — — —

**Figure 5. RDSR Timing**



Note: Dashed Line= mode (1, 1) — — — —



The Status Register can be read to determine if the write cycle is still in progress. If Bit 0 of the Status Register is set at 1, write cycle is in progress. If Bit 0 is set at 0, the device is ready for the next instruction.

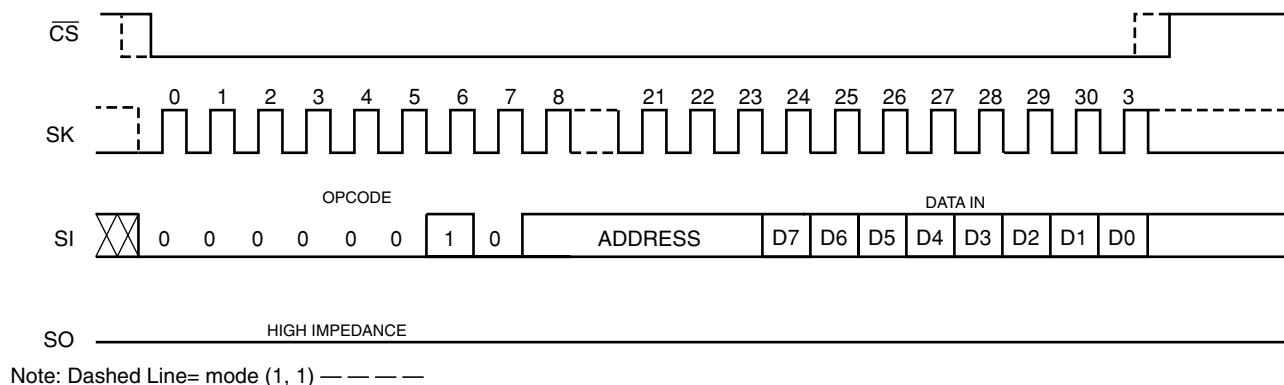
### Page Write

The CAT25C128/256 features page write capability. After the first initial byte the host may continue to write up to 64 bytes of data to the CAT25C128/256. After each byte of data is received, six lower order address bits are internally incremented by one; the high order bits of address will remain constant. The only restriction is that the 64 bytes must reside on the same page. If the

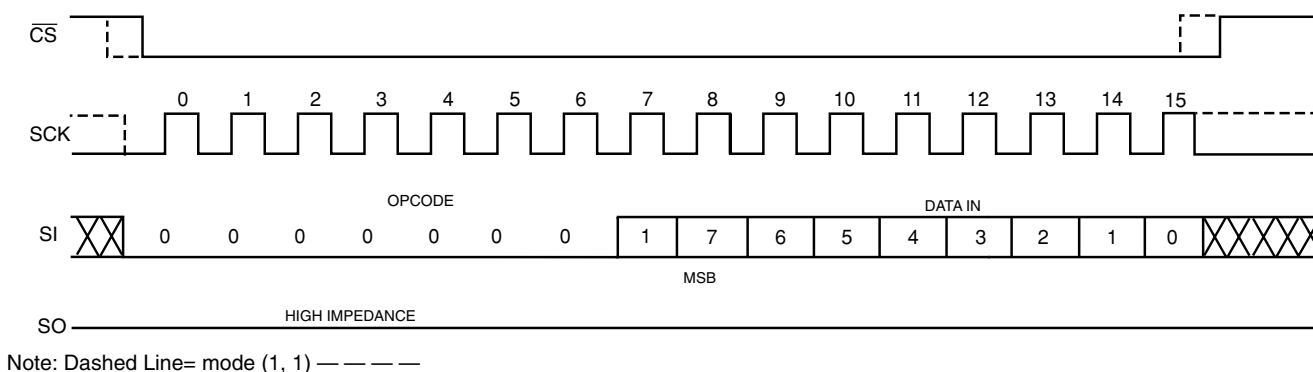
address counter reaches the end of the page and clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been written. The CAT25C128/256 is automatically returned to the write disable state at the completion of the write cycle. Figure 8 illustrates the page write sequence.

To write to the status register, the WRSR instruction should be sent. Only Bit 2, Bit 3 and Bit 7 of the status register can be written using the WRSR instruction. Figure 7 illustrates the sequence of writing to status register.

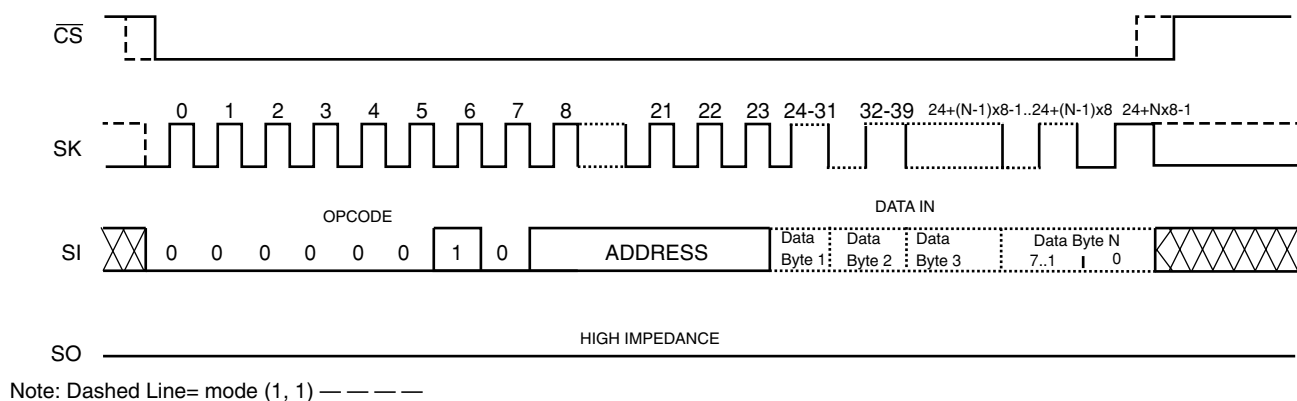
**Figure 6. Write Instruction Timing**



**Figure 7. WRSR Timing**



**Figure 8. Page Write Instruction Timing**



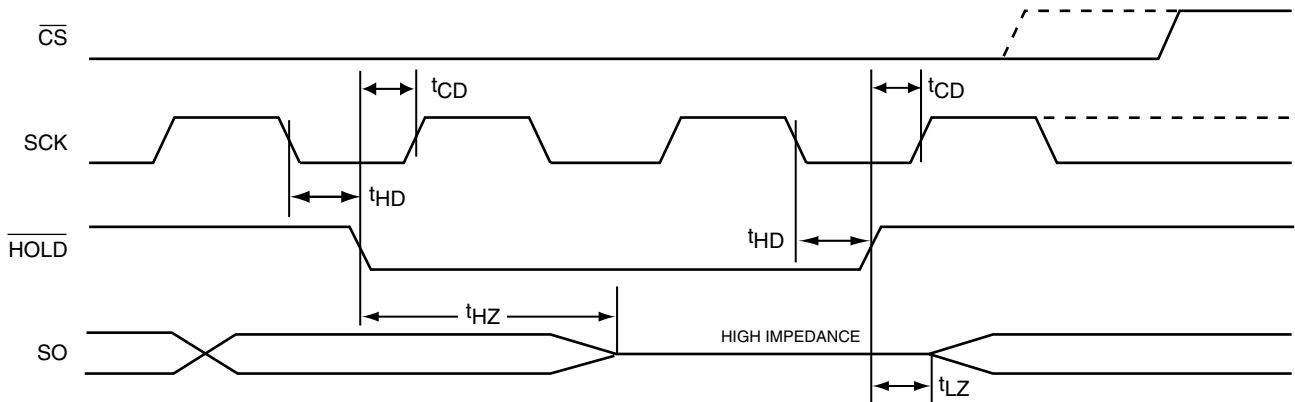
## DESIGN CONSIDERATIONS

The CAT25C128/256 powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued to perform any writes to the device after power up. Also, on power up  $\overline{CS}$  should be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write the CAT25C128/256 goes into a write disable mode.  $\overline{CS}$  must be set high after the proper number of clock cycles to start an internal write cycle. Access to the array during an internal write cycle is ignored and programming is continued. On power up, SO is in a high impedance.

If an invalid op code is received, no data will be shifted into the CAT25C128/256, and the serial output pin (SO) will remain in a high impedance state until the falling edge of  $\overline{CS}$  is detected again.

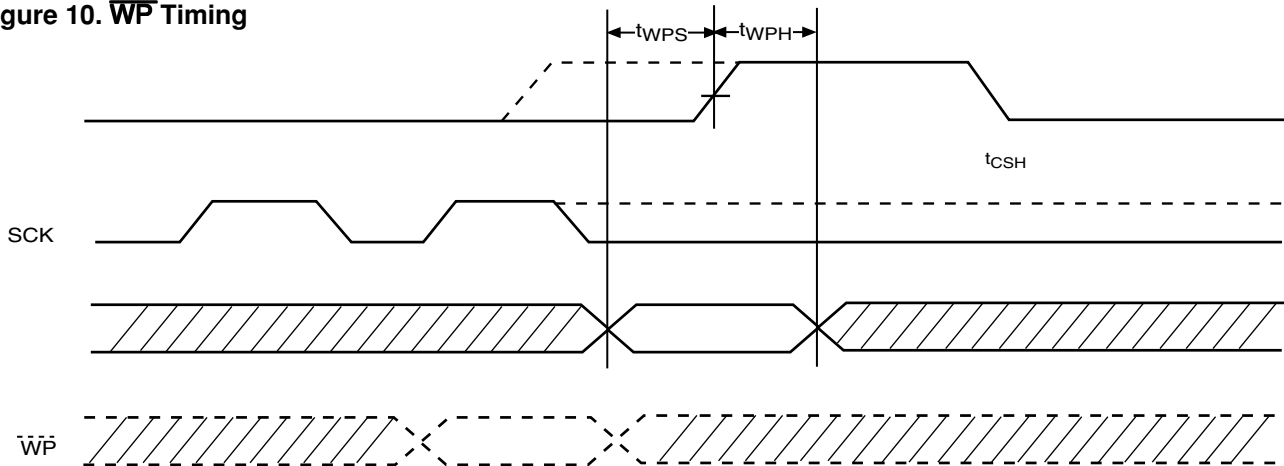
When powering down, the supply should be taken down to 0V, so that the CAT25C128/256 will be reset when power is ramped back up. If this is not possible, then, following a brown-out episode, the CAT25C128/256 can be reset by refreshing the contents of the Status Register (See Application Note AN10).

**Figure 9. HOLD Timing**



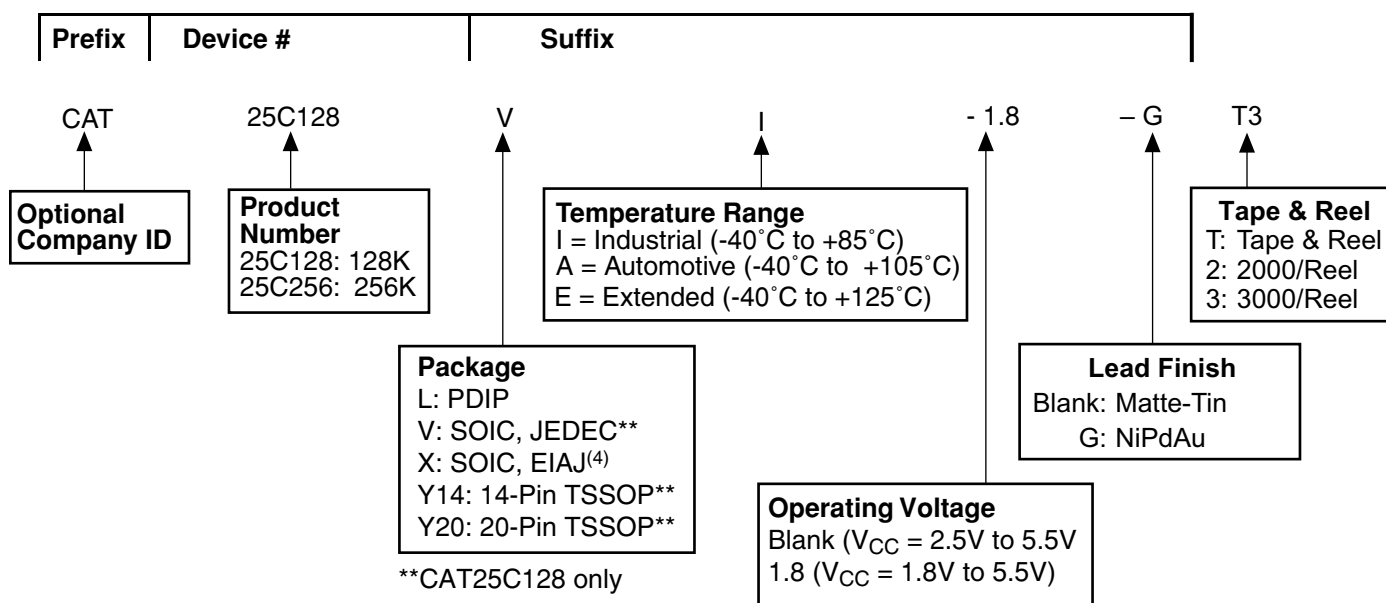
Note: Dashed Line= mode (1, 1) — — — —

**Figure 10. WP Timing**



Note: Dashed Line= mode (1, 1) — — — —

## ORDERING INFORMATION



## Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard finish is NiPdAu pre-plated (PPF).
- (3) The device used in the above example is a CAT25C128VI-1.8-GT3 (SOIC, Industrial Temperature, 1.8V to 5.5V Operating Voltage, NiPdAu, Tape & Reel).
- (4) For SOIC, EIAJ (X) package the standard finish is Matte-Tin. This package is available in 2000 pcs/reel, i.e. CAT25C256XI-T2.
- (5) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

## REVISION HISTORY

| Date       | Rev. | Reason                                                                                                                                                                                                                                      |
|------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8/5/2004   | F    | Updated Features<br>Updated DC Operating Characteristics table & notes                                                                                                                                                                      |
| 2/17/2005  | G    | Updated D.C. Operating Characteristics table                                                                                                                                                                                                |
| 05/23/2005 | H    | Updated Reliability Characteristics table                                                                                                                                                                                                   |
| 10/13/06   | I    | Update Features<br>Update Description<br>Update Pin Configuration<br>Update Pin Functions<br>Update D.C. Operating Characteristics ( $V_{CC}$ Range)<br>Update A.C. Characteristics tables ( $V_{CC}$ Range)<br>Update Ordering Information |

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