CAT25C01, CAT25C02, CAT25C04

1K/2K/4K SPI Serial CMOS EEPROM

Discontinued Parts

FEATURES

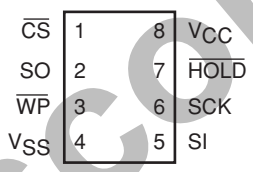
- 10 MHz SPI compatible
- 1.8 to 5.5 volt operation
- 16-byte page write buffer
- Hardware and software protection
- Block write protection
  – Protect 1/4, 1/2 or all of EEPROM array
- Low power CMOS technology
- SPI modes (0,0 & 1,1)
- Industrial temperature range
- 1,000,000 program/erase cycles
- 100 year data retention
- Self-timed write cycle
- *RoHS compliant "Green" & "Gold"*
  8-pin PDIP, SOIC and TSSOP packages

DESCRIPTION

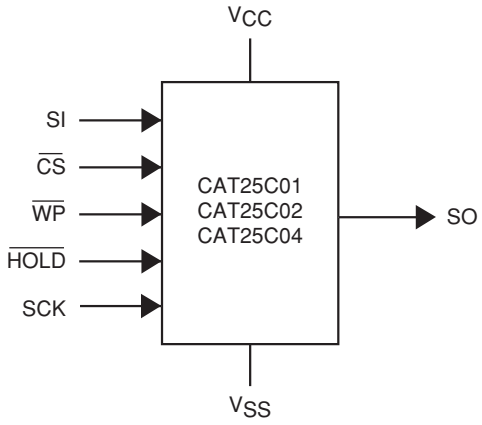
The CAT25C01/02/04 is a 1K/2K/4K Bit SPI Serial CMOS EEPROM internally organized as 128x8/256x8/512x8 bits. Catalyst's advanced CMOS Technology substantially reduces device power requirements. The CAT25C01/02/04 features a 16-byte page write buffer. The device operates via the SPI bus serial interface and is enabled though a Chip Select ($\overline{CS}$). In addition to the Chip Select, the clock input (SCK), data in (SI) and data out (SO) are required to access the device. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence. The CAT25C01/02/04 is designed with software and hardware write protection features including Block Write protection. The device is available in 8-pin DIP, 8-pin SOIC and 8-pin TSSOP packages.

PIN CONFIGURATION

PDIP (L)
SOIC (V)
TSSOP (Y)



FUNCTIONAL SYMBOL



PIN FUNCTIONS

Pin Name	Function
SO	Serial Data Output
SCK	Serial Clock
$\overline{WP}$	Write Protect
V_{CC}	+1.8V to +5.5V Power Supply
V_{SS}	Ground
$\overline{CS}$	Chip Select
SI	Serial Data Input
$\overline{HOLD}$	Suspends Serial Input

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

Doc. No. 1105, Rev. B

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground(1)	-0.5 V to +6.5 V

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS(2)

Symbol	Parameter	Min	Units
N_{END}(*)	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

(*) Page Mode, V_{CC} = 5 V, 25°C

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Supply Current	Read or Write at 5 MHz		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}, $\overline{CS}$ = V_{CC}		2	µA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		2	µA
V_{IL}	Input Low Voltage		-0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} > 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} > 1.8 V, I_{OL} = 1.0 mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

T_A = 25°C, f = 1 MHz, V_{CC} = 5 V

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN}(2)	SDA I/O Pin Capacitance	V_{IN} = 0 V		8	pF
C_{IN}(2)	Input Capacitance (other pins)	V_{IN} = 0 V		6	pF
Z_{WPL}	WP Input Low Impedance	V_{IN} < 0.5 V	5	70	kΩ
I_{LWPH}	WP Input High Leakage	V_{IN} > V_{CC} x 0.7		2	µA

Note:

(1) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	CAT25CXX-1.8 1.8V-5.5V		CAT25CXX 2.5V-5.5V		CAT25CXX 4.5V-5.5V		UNITS	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{SU}	Data Setup Time	50		20		20		ns	
t_H	Data Hold Time	50		20		20		ns	
t_{WH}	SCK High Time	250		75		40		ns	
t_{WL}	SCK Low Time	250		75		40		ns	
f_{SCK}	Clock Frequency	DC	1	DC	5	DC	10	MHz	
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50		50		50	ns	
t_{RI}(1)	Input Rise Time		2		2		2	µs	
t_{FI}(1)	Input Fall Time		2		2		2	µs	
t_{HD}	$\overline{HOLD}$ Setup Time	100		40		40		ns	
t_{CD}	$\overline{HOLD}$ Hold Time	100		40		40		ns	
t_{WC}(4)	Write Cycle Time		5		5		5	ms	C_L = 50pF (note 2)
t_V	Output Valid from Clock Low		250		75		40	ns	
t_{HO}	Output Hold Time	0		0		0		ns	
t_{DIS}	Output Disable Time		250		75		75	ns	
t_{HZ}	$\overline{HOLD}$ to Output High Z		150		50		50	ns	
t_{CS}	$\overline{CS}$ High Time	500		100		100		ns	
t_{CSS}	$\overline{CS}$ Setup Time	500		100		100		ns	
t_{CSH}	$\overline{CS}$ Hold Time	500		100		100		ns	
t_{WPS}	$\overline{WP}$ Setup Time	150		50		50		ns	
t_{WPH}	$\overline{WP}$ Hold Time	150		50		50		ns	

Power-Up Timing(1)(3)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) AC Test Conditions:
Input Pulse Voltages: $0.3V_{CC}$ to $0.7V_{CC}$
Input rise and fall times: ≤10ns
Input and output reference voltages: $0.5V_{CC}$
Output load: current source I_{OL} max/I_{OH} max; C_L=50pF
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

FUNCTIONAL DESCRIPTION

The CAT25C01/02/04 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT25C01/02/04 to interface directly with many of today's popular microcontrollers. The CAT25C01/02/04 contains an 8-bit instruction register. (The instruction set and the operation codes are detailed in the instruction set table)

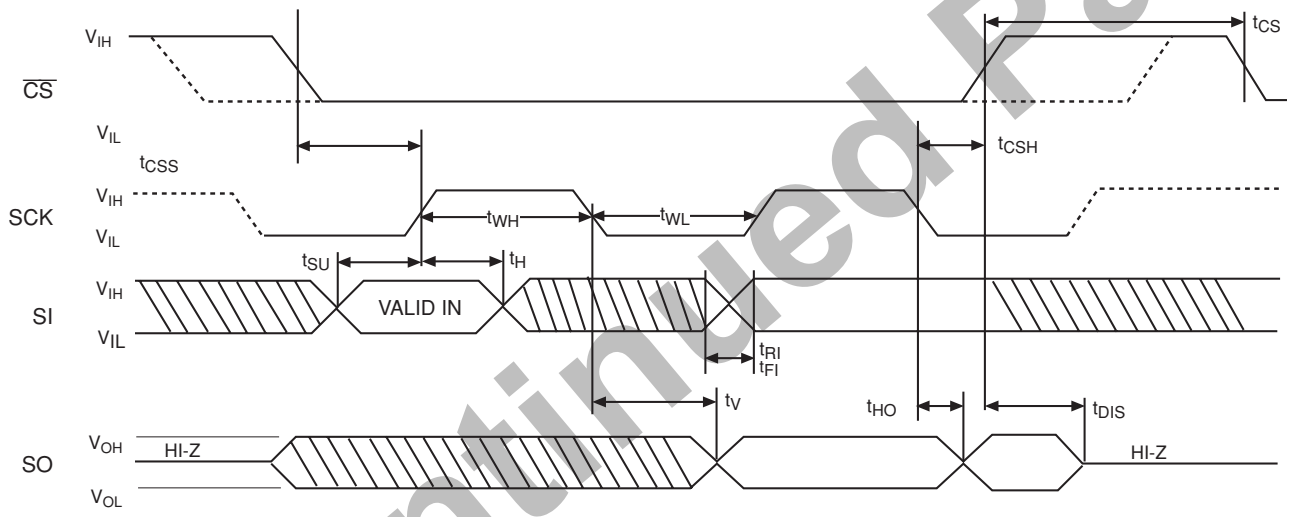
After the device is selected with $\overline{CS}$ going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

PIN DESCRIPTION

SI: Serial Input
SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the CAT25010/20/40. Input data is latched on the rising edge of the serial clock for SPI modes (0, 0 & 1, 1).

SO: Serial Output
SO is the serial data output pin. This pin is used to transfer data out of the CAT25C01/02/04. During a read cycle, data is shifted out on the falling edge of the serial clock for SPI modes (0,0 & 1,1).

Figure 1. Sychronous Data Timing



Note: Dashed Line= mode (1, 1) – – – – –

INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 X011(1)	Read Data from Memory
WRITE	0000 X010(1)	Write Data to Memory

Note:
(1) X=0 for CAT25C01, CAT25C02. X=A8 for CAT25C04.

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

SCK: Serial Clock
SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the CAT25C01/02/04. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK for SPI modes (0,0 & 1,1) .

$\overline{CS}$: Chip Select

$\overline{CS}$ is the Chip select pin. $\overline{CS}$ low enables the CAT25C01/02/04 and $\overline{CS}$ high disables the CAT25C01/02/04. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway) The CAT25C01/02/04 draws ZERO current in the Standby mode. A high to low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

$\overline{WP}$: Write Protect
$\overline{WP}$ is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low and the WPEN bit in the status register is set to "1", all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to 0. Figure 10 illustrates the $\overline{WP}$ timing sequence during a write operation.

$\overline{HOLD}$: Hold

The $\overline{HOLD}$ pin is used to pause transmission to the CAT25C01/20/40 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to V_{CC} or tied to V_{CC} through a resistor. Figure 9 illustrates hold timing sequence.

STATUS REGISTER

7	6	5	4	3	2	1	0
WPEN	1	1	1	BP1	BP0	WEL	$\overline{RDY}$

BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	CAT25C01: 60-7F CAT25C02: C0-FF CAT25C04: 180-1FF	Quarter Array Protection
1	0	CAT25C01: 40-7F CAT25C02: 80-FF CAT25C04: 100-1FF	Half Array Protection
1	1	CAT25C01: 00-7F CAT25C02: 00-FF CAT25C04: 000-1FF	Full Array Protection

WRITE PROTECT ENABLE OPERATION

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

STATUS REGISTER

The Status Register indicates the status of the device. The $\overline{RDY}$ (Ready) bit indicates whether the CAT25C01/02/04 is busy with a write operation. When set to 1 a write cycle is in progress and when set to 0 the device indicates it is ready. This bit is read only. The WEL (Write Enable) bit indicates the status of the write enable latch. When set to 1, the device is in a Write Enable state and when set to 0 the device is in a Write Disable state. The WEL bit can only be set by the WREN instruction and can be reset by the WRDI instruction.

The BP0 and BP1 (Block Protect) bits indicate which blocks are currently protected. These bits are set by the user issuing the WRSR instruction. The user is allowed to protect quarter of the memory, half of the memory or the entire memory by setting these bits. Once protected, the user may only read from the protected portion of the array. These bits are non-volatile.

The WPEN (Write Protect Enable) is an enable bit for the $\overline{WP}$ pin. The $\overline{WP}$ pin and WPEN bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ is low and WPEN bit is set to high. The user cannot write to the status register, (including the block protect bits and the WPEN bit) and the block protected sections in the memory array when the chip is hardware write protected. Only the sections of the memory array that are not block protected can be written. Hardware write protection is disabled when either $\overline{WP}$ pin is high or the WPEN bit is zero.

DEVICE OPERATION

Write Enable and Disable

The CAT25C01/02/04 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when V_{CC} is applied. WREN instruction will enable writes (set the latch) to the device. WRDI instruction will disable writes (reset the latch) to the device. Disabling writes will protect the device against inadvertent writes.

READ Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the CAT25C01/02/04, followed by the 8-bit address for CAT25C01/02/04 (for the CAT25C04, bit 3 of the read data instruction contains address A8).

Figure 2. WREN Instruction Timing

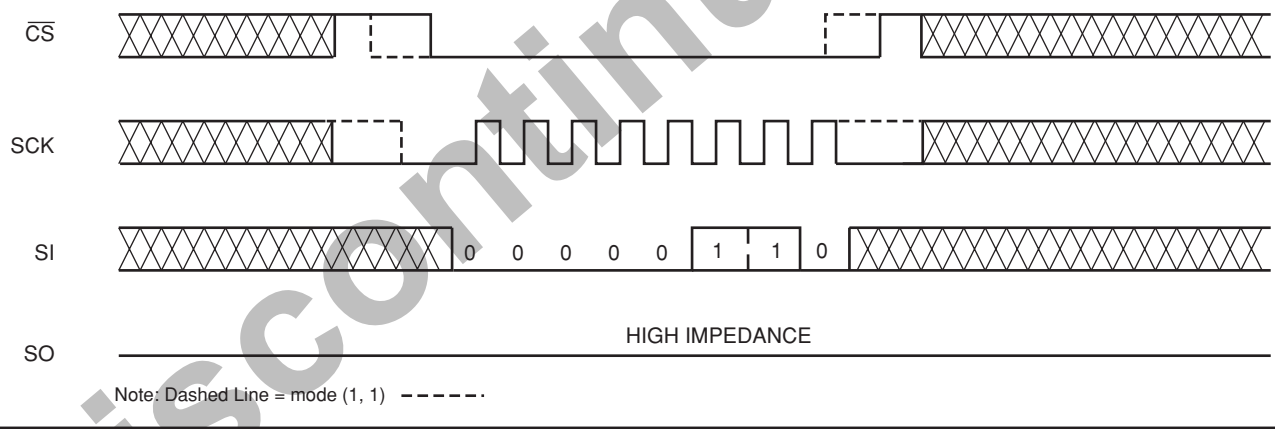
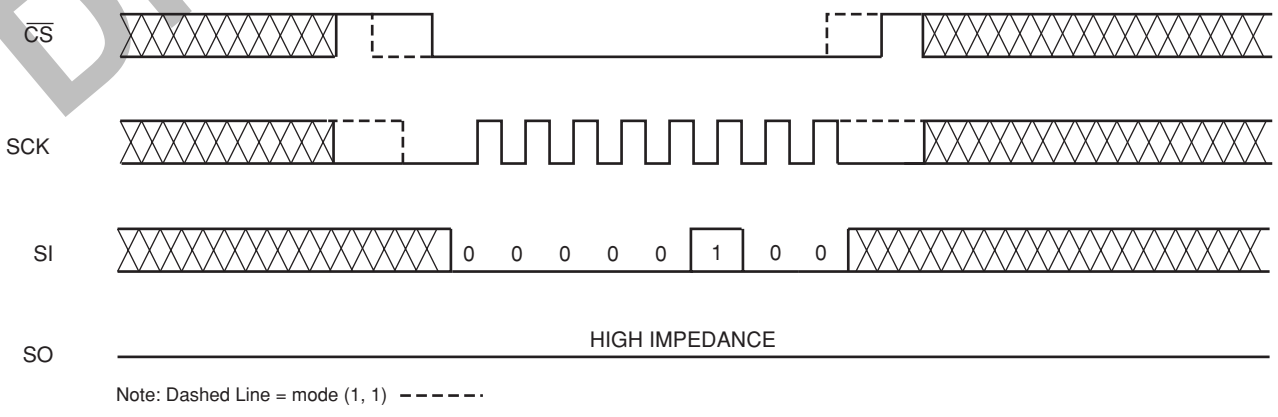


Figure 3. WRDI Instruction Timing



Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by pulling the $\overline{CS}$ high. To read the status register, RDSR instruction should be sent. The contents of the status register are shifted out on the SO line. The status register may be read at any time even during a write cycle. Read sequece is illustrated in Figure 4. Reading status register is illustrated in Figure 5.

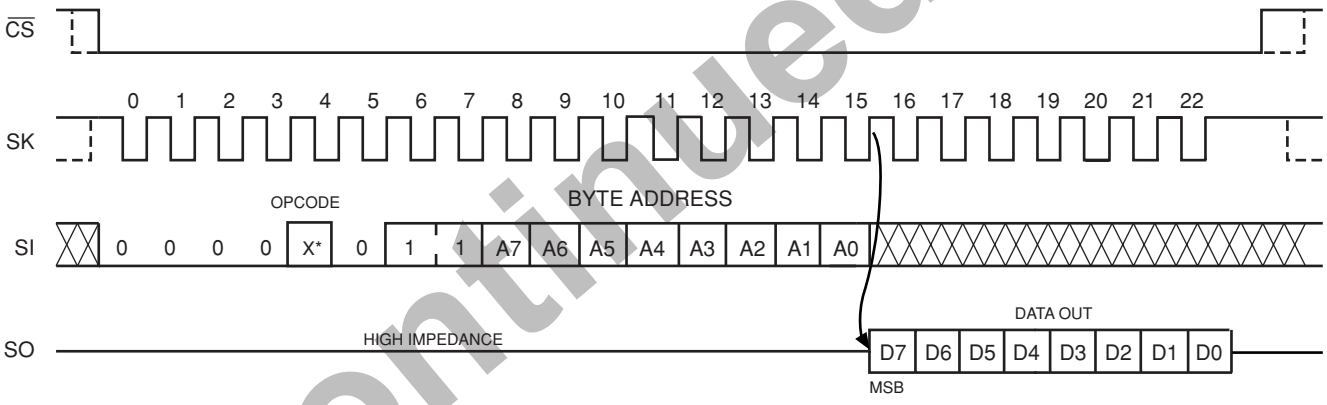
WRITE Sequence

The CAT25C01/02/04 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to CAT25C01/02/04. The device goes into Write enable state by pulling the $\overline{CS}$ low and then clocking the WREN instruction into CAT25C01/02/04. The $\overline{CS}$ must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set. Also, for a successful write operation the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block protection level.

Byte Write

Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the $\overline{CS}$ low, issuing a write instruction via the SI line, followed by the 8-bit address for CAT25C01/02/04 (for the 25C04, bit 3 of the read data instruction contains address A8). Programming will start after the $\overline{CS}$ is brought high. Figure 6 illustrates byte write sequence.

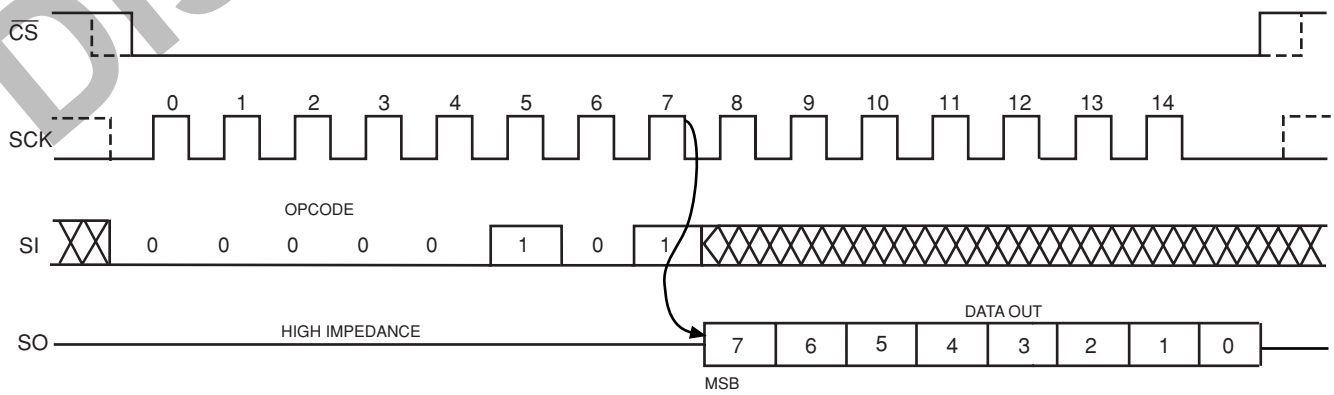
Figure 4. Read Instruction Timing



*Please check the instruction set table for address
X=0 for 25010, 25020 ; X=A8 for 25040

Note: Dashed line = mode (1,1)----

Figure 5. RDSR Instruction Timing



Note: Dashed Line= mode (1, 1) – – – – –

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

During an internal write cycle, all commands will be ignored except the RDSR (Read Status Register) instruction.

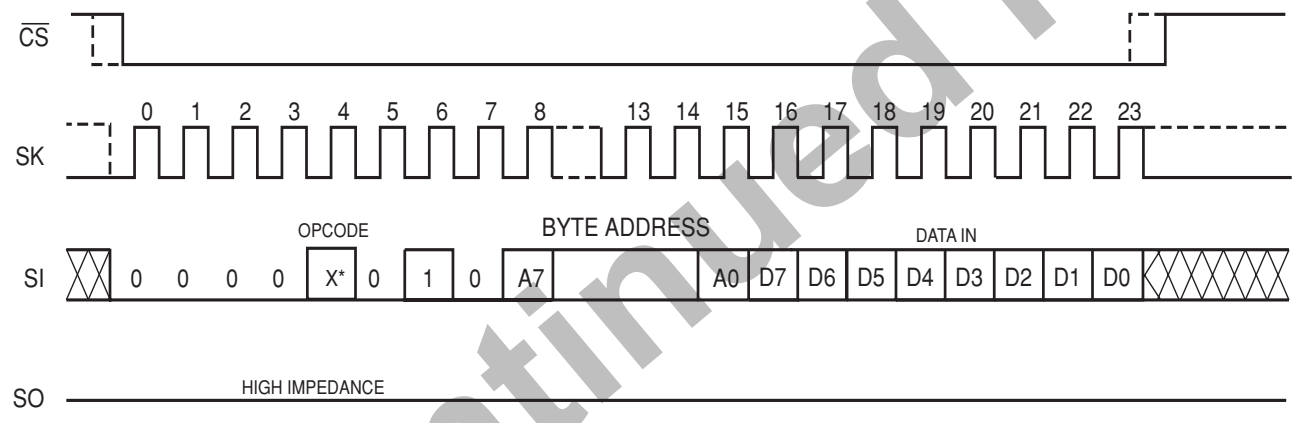
The Status Register can be read to determine if the write cycle is still in progress. If Bit 0 of the Status Register is set at 1, write cycle is in progress. If Bit 0 is set at 0, the device is ready for the next instruction.

Page Write

The CAT25C01/02/04 features page write capability. After the initial byte, the host may continue to write up to 16 bytes of data to the CAT25C01/02/04. After each byte of data received, lower order address bits are internally incremented by one; the high order bits of address will remain constant. The only restriction is that the X (X=16 for CAT25C01/02/04) bytes must reside on the same page. If the address counter reaches the end of the page and clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written. The CAT25C01/02/04 is automatically returned to the write disable state at the completion of the write cycle. Figure 8 illustrates the page write sequence.

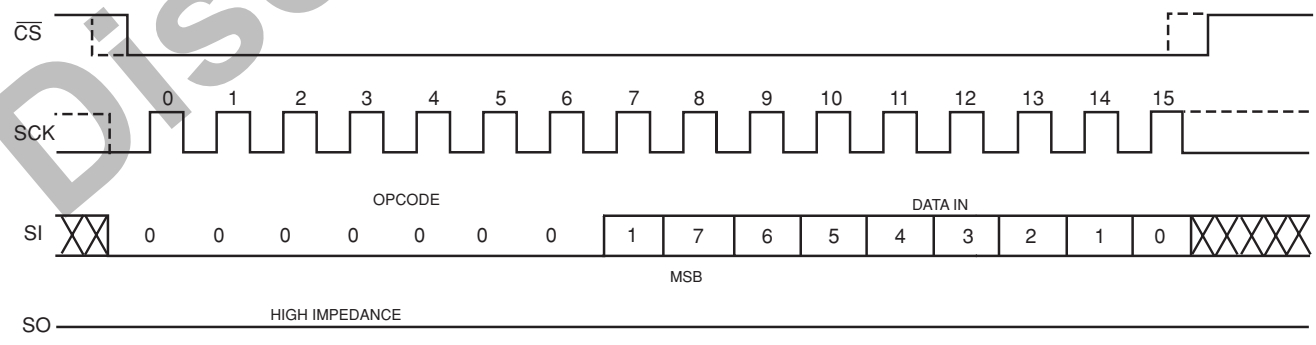
To write to the status register, the WRSR instruction should be sent. Only Bit 2, Bit 3 and Bit 7 of the status register can be written using the WRSR instruction. Figure 7 illustrates the sequence of writing to status register.

Figure 6. Write Instruction Timing



Note: Dashed Line= mode (1, 1) – – – – –
*X=0 for 25010, 25020 ; X=A8 for 25040

Figure 7. WRSR Timing



Note: Dashed Line= mode (1, 1) – – – – –

Discontinued Parts

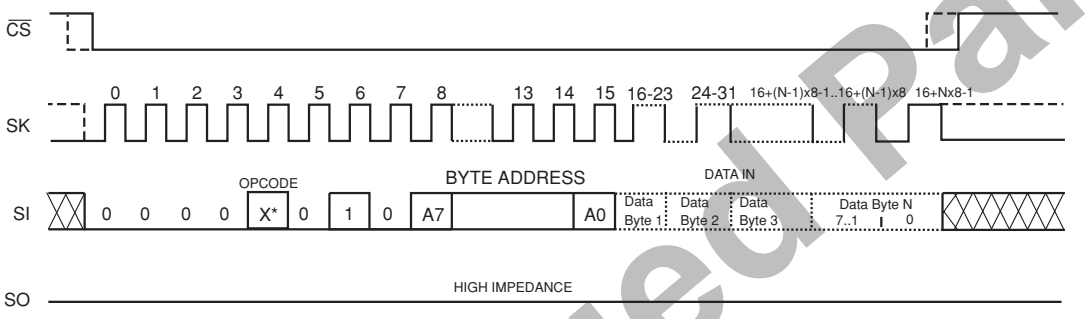
© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

DESIGN CONSIDERATIONS

The CAT25C01/02/04 powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued to perform any writes to the device after power up. Also,on power up $\overline{CS}$ should be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the CAT25C01/02/04 goes into a write disable mode. $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle. Access to the array during an internal write cycle is ignored and programming is continued. On power up, SO is in a high impedance. If an invalid op code is received, no data will be shifted into the CAT25C01/02/04, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again.

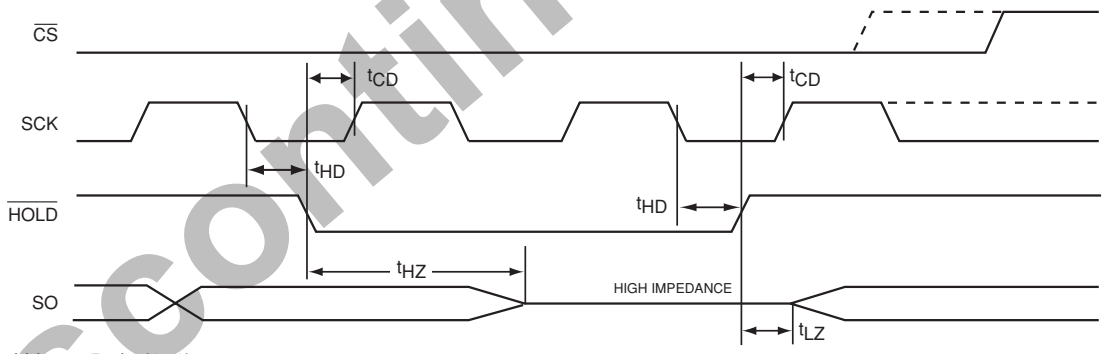
When powering down, the supply should be taken down to 0V, so that the CAT25C01/02/04 will be reset when power is ramped back up. If this is not possible, then, following a brown-out episode, the CAT25C01/02/04 can be reset by refreshing the contents of the Status Register (See Application Note AN10).

Figure 8. Page Write Instruction Timing



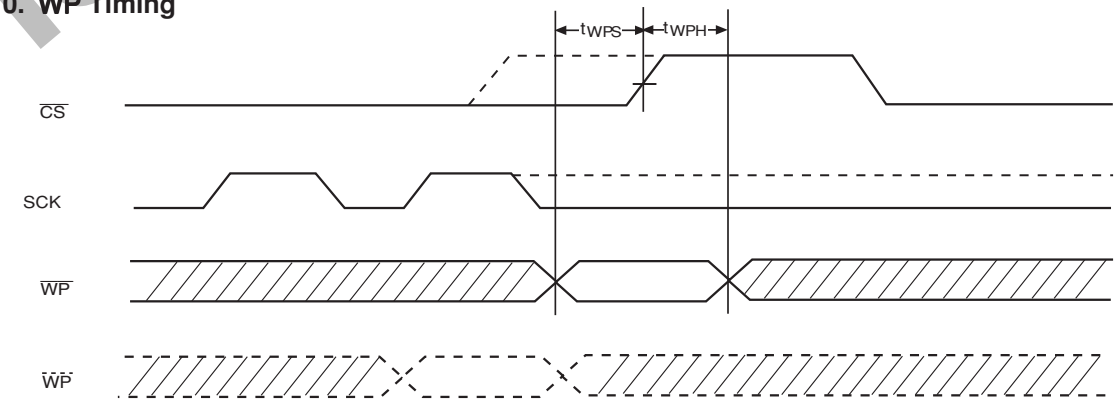
Note: Dashed Line= mode (1, 1) – – – – – *X=0 for CAT25C01, CAT25C02; X=A8 for CAT25C04

Figure 9. $\overline{HOLD}$ Timing



Note: Dashed Line= mode (1, 1) – – – – –

Figure 10. $\overline{WP}$ Timing

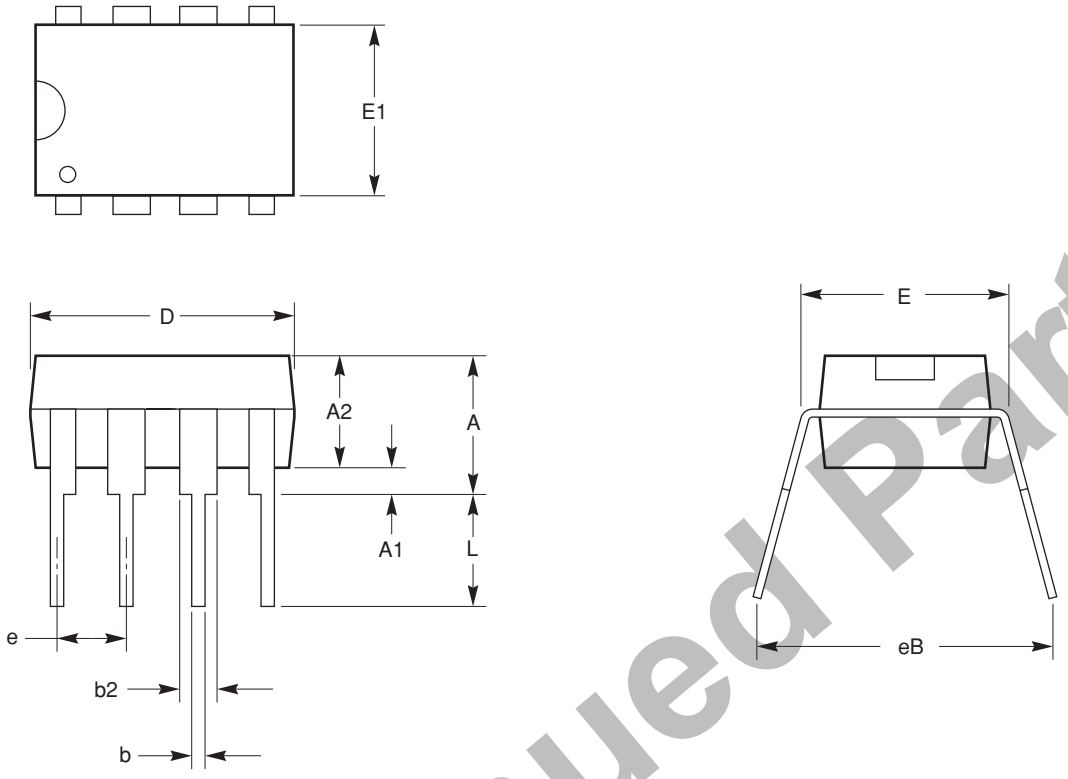


Note: Dashed Line= mode (1, 1) – – – – –

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

8-LEAD 300 MIL WIDE PLASTIC DIP (L)



SYMBOL	MIN	NOM	MAX
A	0.120		0.210
A1	0.015		
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b2	0.045	0.060	0.070
D	0.355	0.365	0.400
D2	0.300		0.325
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 BSC	
eB			0.430
L	0.115	0.130	0.150

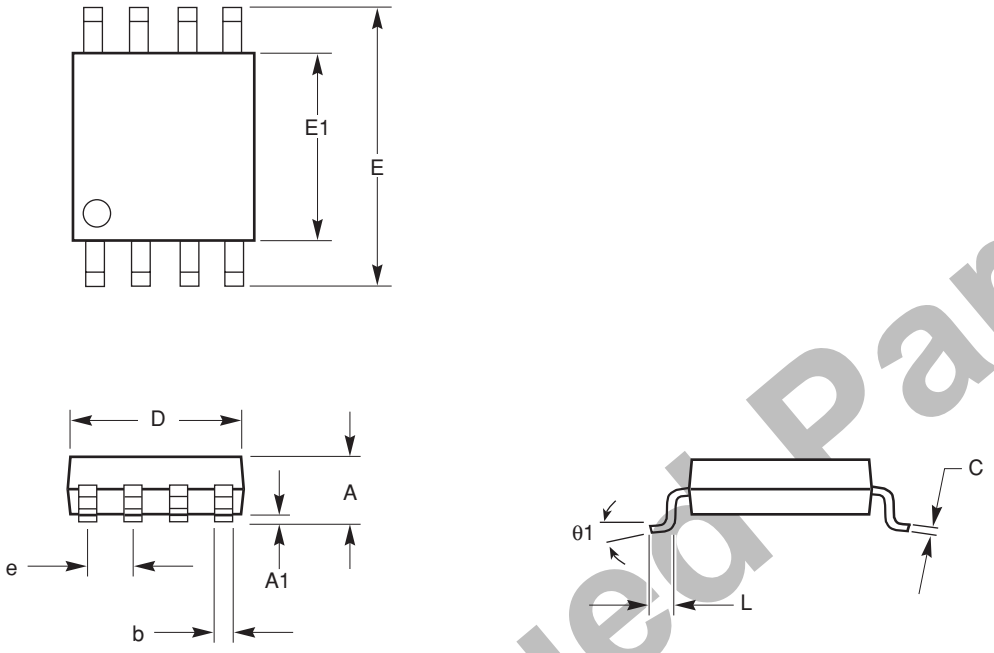
24C02_8-LEAD_DIP_(300P).eps

Discontinued Parts

Notes:
1. Complies with JEDEC Standard MS001.
2. All dimensions are in inches.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

8-LEAD 150 MIL WIDE SOIC (V)



SYMBOL	MIN	NOM	MAX
A1	0.0040		0.0098
A2	0.0532		0.0688
b	0.013		0.020
C	0.0075		0.0098
D	0.1890		0.1968
E	02284		0.2440
E1	0.149		0.1574
e		0.050 BSC	
f	0.0099		0.0196
θ1	0°		8°

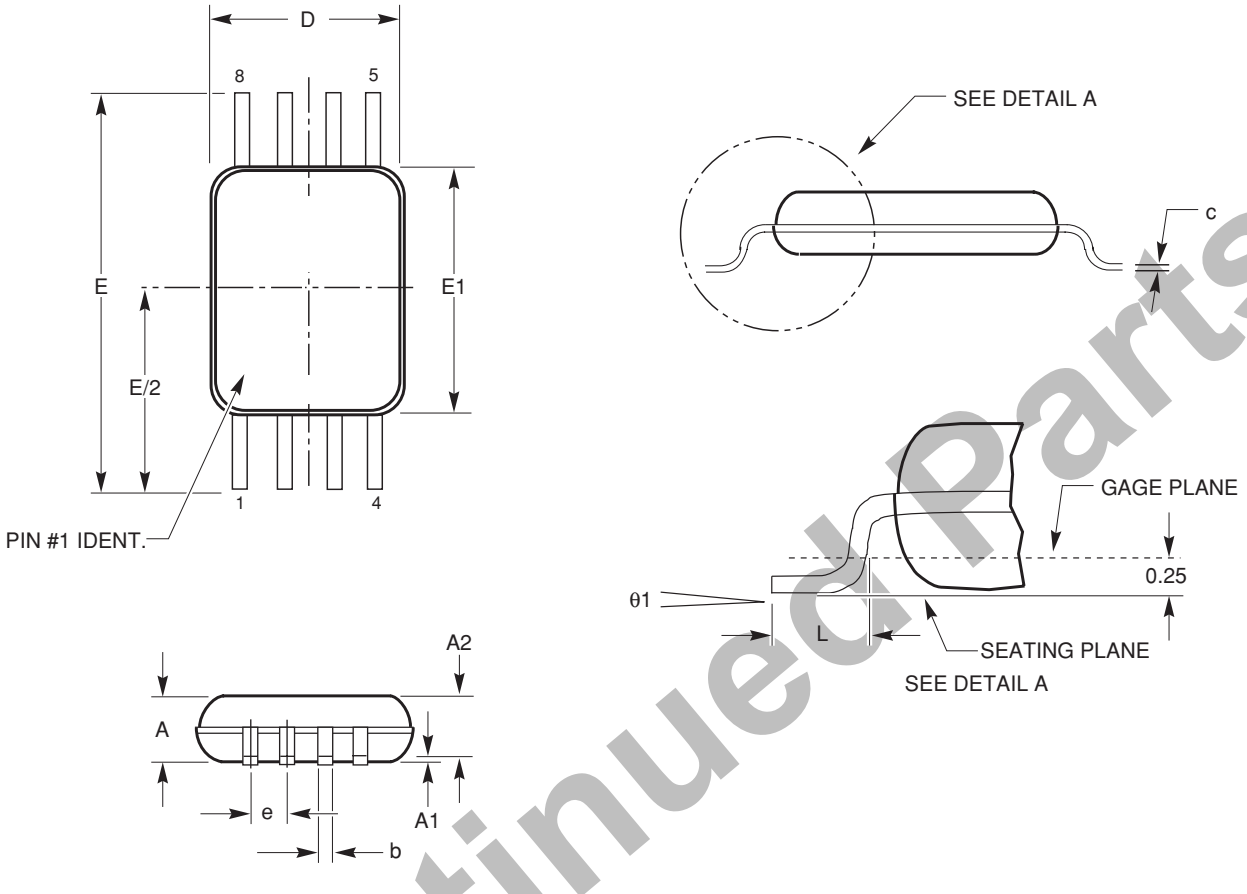
24C02_8-LEAD_SOIC.eps

Discontinued Parts

Notes:
1. Complies with JEDEC specification MS-012 dimensions.
2. All linear dimensions in millimeters.

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

8-LEAD TSSOP (Y)



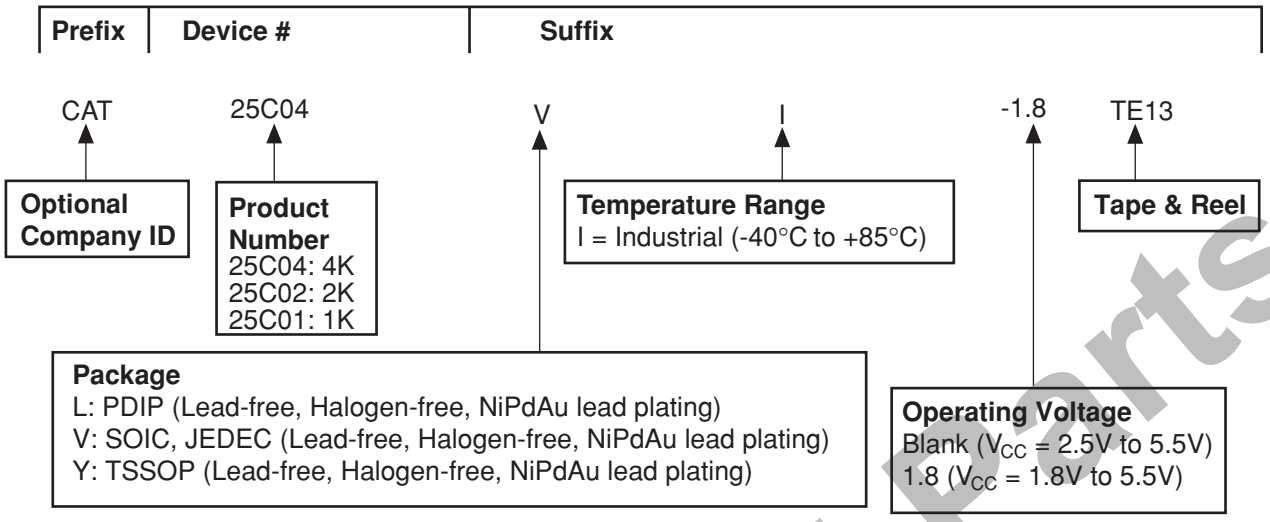
SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.4	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.75
θ1	0.00		8.00

Notes:
1. All dimensions in millimeters.

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

ORDERING INFORMATION



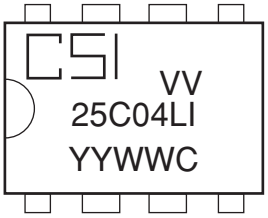
Notes:
(1) The device used in the above example is a CAT25C04VI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 5.5 Volt Operating Voltage, Tape & Reel)

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

PACKAGE MARKING

8-Lead PDIP



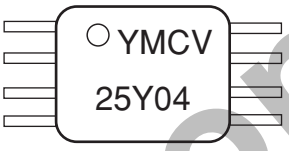
CSI = Catalyst Semiconductor, Inc.
25C04L = Device Code
I = Temperature Range
YY = Production Year
WW = Production Week
C = Product Revision
VV = Voltage Range
1.8V - 5.5V = 18
2.5V - 5.5V = Blank

8-Lead SOIC



CSI = Catalyst Semiconductor, Inc.
25C04V = Device Code
I = Temperature Range
YY = Production Year
WW = Production Week
C = Product Revision
VV = Voltage Range
1.8V - 5.5V = 18
2.5V - 5.5V = Blank

8-Lead TSSOP



Y = Production Year
M = Production Month
C = Die Revision
25Y04 = Device Code
I = Industrial Temperature Range
V = Voltage Range
1.8V - 5.5V = 8
2.5V - 5.5V = Blank

Notes:
(1) The circle on the package marking indicates the location of Pin 1.

Discontinued Parts

© 2005 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

REVISION HISTORY

Date	Rev.	Reason
10/13/05	A	Initial Issue

Discontinued Parts

Copyrights, Trademarks and Patents
Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

DPP ™ AE² ™ MiniPot™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products. For a complete list of patents issued to Catalyst Semiconductor contact the Company's corporate office at 408.542.1000.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.

Catalyst Semiconductor, Inc.
Corporate Headquarters
1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: 408.542.1000
Fax: 408.542.1200
www.catalyst-semiconductor.com

Publication #: 1105
Revison: B
Issue date: 12/23/05