CAT24C208

EEPROM Serial 8-Kb I²C Dual Port

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SOIC−8
W SUFFIX
CASE 751BD

Description

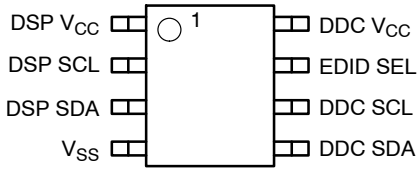
The CAT24C208 is an EEPROM Serial 8−Kb I²C Dual Port internally organized as 4 segments of 256 bytes each. The CAT24C208 features a 16−byte page write buffer and can be accessed from either of two separate I²C compatible ports, DSP (SDA, SCL) and DDC (SDA, SCL).

Arbitration between the two interface ports is automatic and allows the appearance of individual access to the memory from each interface.

Features

- Supports Standard and Fast I²C Protocol
- 2.5 V to 5.5 V Operation
- 16−Byte Page Write Buffer
- Schmitt Triggers and Noise Protection Filters on I²C Bus Input
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- SOIC 8−lead Package
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

PIN CONFIGURATION



SOIC (W)
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

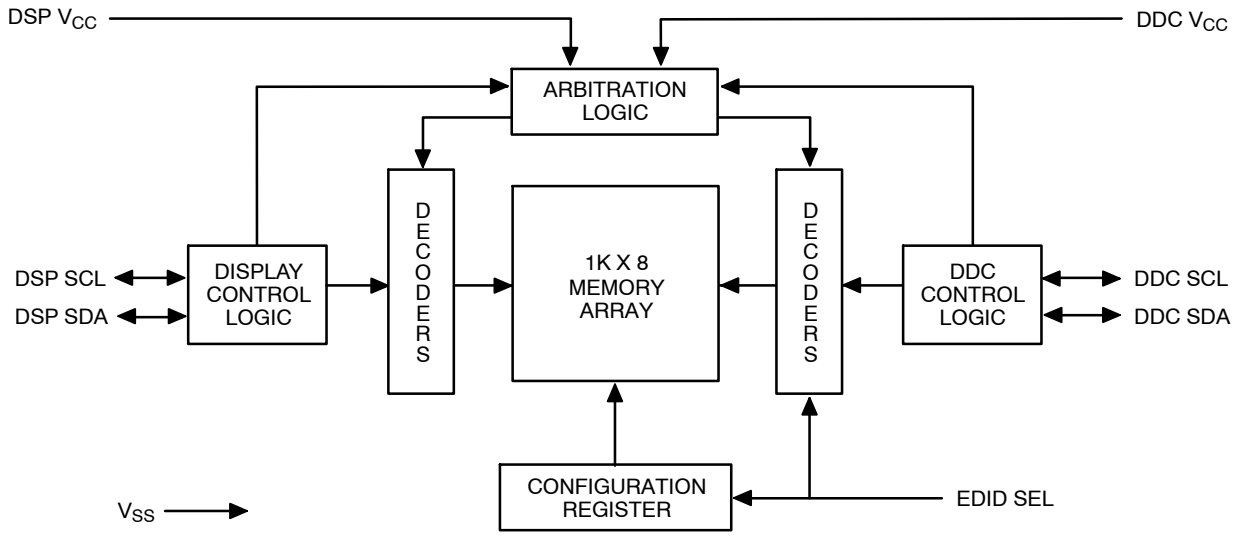


Figure 1. Block Diagram

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Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Function
1	DSP V_{CC}	Device power from display controller
2	DSP SCL	The CAT24C208 DSP serial clock bidirectional pin is used to clock all data transfers into or out of the device DSP SDA pin and is also used to block DSP Port access when DDC Port is active.
3	DSP SDA	DSP Serial Data/Address. The bidirectional DSP serial data/address pin is used to transfer data into and out of the device from a display controller. The DSP SDA pin is an open drain output and can be wireOR'ed with other open drain or open collector outputs.
4	V_{SS}	Device ground.
5	DDC SDA	DDC Serial Data/Address. The bidirectional DDC serial data/address pin is used to transfer data into and out of the device from a DDC host. The DDC SDA pin is an open drain output and can be wire−OR'ed with other open drain or open collector outputs.
6	DDC SCL	The CAT24C208 DDC serial clock bidirectional pin is used to clock all data transfers into or out of the device DDC SDA pin, and is used to block DDC Port for access when DSP Port is active.
7	EDID SEL	EDID select. The CAT24C208 EDID select input selects the active bank of memory to be accessed via the DDC SDA/SCL interface as set in the configuration register.
8	DDC V_{CC}	Device power when powered from a DDC host.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−2.0 to +V_{CC} +2.0	V
V_{CC} with Respect to Ground	−2.0 to +7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 secs)	300	°C
Output Short Circuit Current (Note 2)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
N_{END} (Note 3)	Endurance	MIL−STD−883, Test Method 1033	1,000,000	Cycles/Byte
T_{DR} (Note 3)	Data Retention	MIL−STD−883, Test Method 1008	100	Years
V_{ZAP} (Note 3)	ESD Susceptibility	JEDEC Standard JESD 22	2000	Volts
I_{LTH} (Notes 3 and 4)	Latch−up	JEDEC Standard 17	100	mA

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} +1 V.

Table 4. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{I/O}$ (Note 5)	Input/Output Capacitance (Either DSP or DDC SDA)	$V_{I/O}$ = 0 V			8	pF
C_{IN} (Note 5)	Input Capacitance (EDID, Either DSP or DDC SCL)	V_{IN} = 0 V			6	pF

5. This parameter is tested initially and after a design or process change that affects the parameter.

Table 5. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.5 V to 5.5 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 100 KHz			3	mA
I_{SB}	Standby Current (V_{CC} = 5.0 V)	V_{IN} = GND or either DSP or DDC V_{CC}			50	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to either DSP or DDC V_{CC}			10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to either DSP or DDC V_{CC}			10	μA
V_{IL}	Input Low Voltage		−1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
VHYS	Input Hysteresis		0.05			V
V_{OL1}	Output Low Voltage (V_{CC} = 3 V)	I_{OL} = 3 mA			0.4	V
V_{CCL1}	Leakage DSP V_{CC} to DDC V_{CC}				±100	μA
V_{CCL2}	Leakage DDC V_{CC} to DSP V_{CC}				±100	μA

Table 6. A.C. CHARACTERISTICS (V_{CC} = 2.5 V to 5.5 V, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
READ & WRITE CYCLE LIMITS				
F_{SCL}	Clock Frequency		400	kHz
T_I (Note 6)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		0.9	μs
t_{BUF} (Note 6)	Time the Bus Must be Free Before a New Transmission Can Start	1.3		μs
$t_{HD:STA}$	Start Condition Hold Time	0.6		μs
t_{LOW}	Clock Low Period	1.3		μs
t_{HIGH}	Clock High Period	0.6		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	100		ns
t_R (Note 6)	SDA and SCL Rise Time		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		μs
t_{DH}	Data Out Hold Time	100		ns

Table 7. POWER−UP TIMING (Notes 6 and 7)

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power−up to Read Operation			1	ms
t_{PUW}	Power−up to Write Operation			1	ms

6. This parameter is tested initially and after a design or process change that affects the parameter.
7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 8. WRITE CYCLE LIMITS

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			5	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Functional Description

The CAT24C208 has a total memory space of 1K bytes which is accessible from either of two I^2C interface ports, (DSP_SDA and DSP_SCL) or (DDC_SDA and DDC_SCL), and with the use of segment pointer at address 60h. On power up and after any instruction, the segment pointer will be in segment 00h for DSP and in segment 00h of the bank selected by the configuration register for DDC.

The entire memory appears as contiguous memory space from the perspective of the display interface (DSP_SDA and DSP_SCL), see Figure 4, and Figures 14 to Figure 21 for a complete description of the DSP Interface.

A configuration register at addresses 62/63h is used to configure the operation and memory map of the device as seen from the DDC interface, (DDC_SDA and DDC_SCL).

Read and write operations can be performed on any location within the memory space from the display DSP interface regardless of the state of the EDID SEL pin or the activity on the DDC interface. From the DDC interface, the memory space appears as two 512 byte banks of memory, with 2 segments each 00h and 01h in the upper and lower bank, see Figure 3.

Each bank of memory can be used to store an E−EDID data structure. However, only one bank can be read through the DDC port at a time. The active bank of memory (that is, the bank that appears at address A0h on the DDC port) is controlled through the configuration register at 62/63h and the EDID_SEL pin.

No write operations are possible from the DDC interface unless the DDC Write Enable bit is set (WE = 1) in the device configuration register at device address 62h.

The device automatically arbitrates between the two interfaces to allow the appearance of individual access to the memory from each interface.

In a typical E−EDID application the EDID_SEL pin is usually connected to the “Analog Cable Detect” pin of a VESA M1 compliant, dual−mode (analog and digital) display. In this manner, the E−EDID appearing at address A0h on the DDC port will be either the analog or digital E−EDID, depending on the state of the “Analog Cable Detect” pin (pin C3 of the M1−DA connector). See Figure 2.

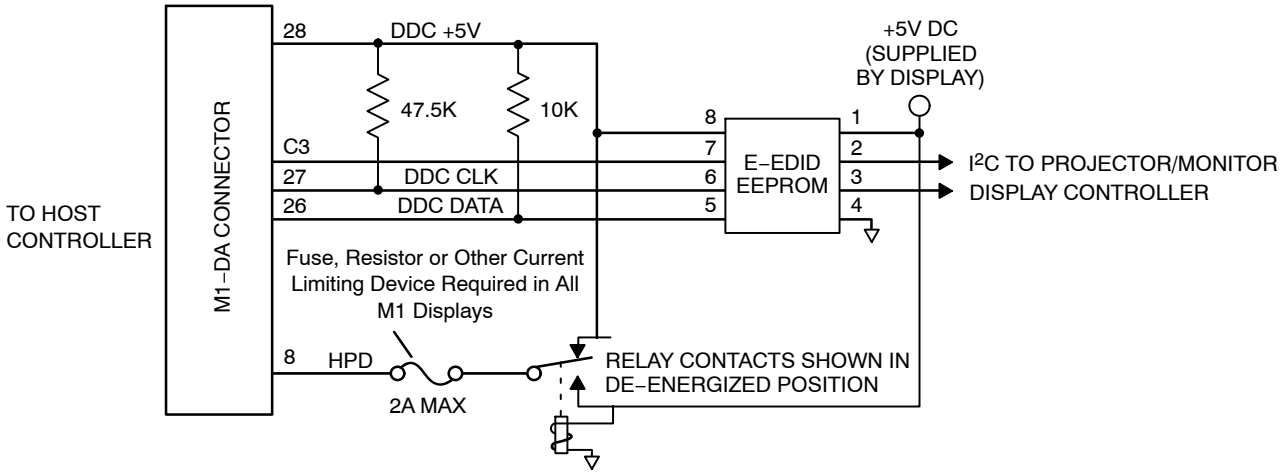


Figure 2.

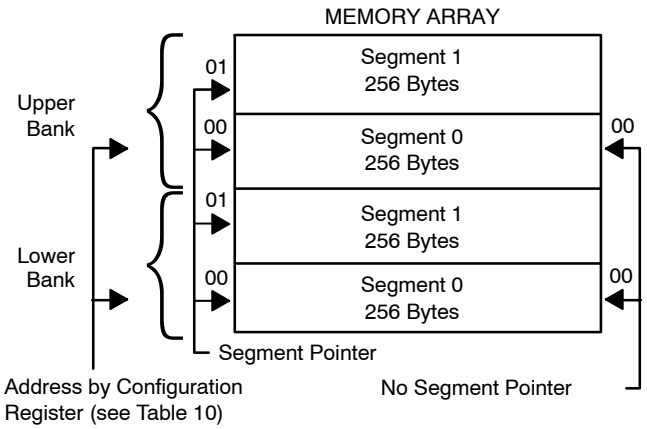


Figure 3. DDC Interface

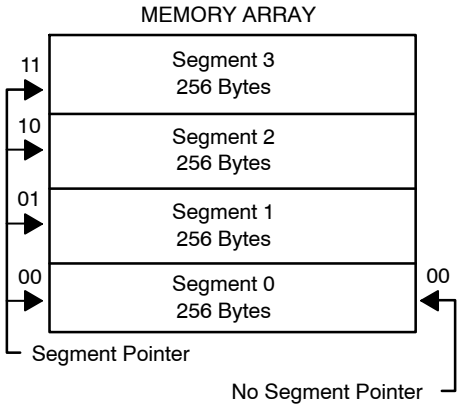


Figure 4. DSP Interface

I²C Bus Protocol

The following defines the features of the I²C bus protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of either SDA when the respective SCL is HIGH. The CAT24C208 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the respective SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24C208 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT24C208 is in a READ mode it transmits 8 bits of data, releases the respective SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C208 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

After an unsuccessful data transfer an acknowledge will not be issued (NACK) by the slave (CAT24C208), and the master should abort the sequence. If continued the device will read from or write to the wrong address in the two instruction format with the segment pointers.

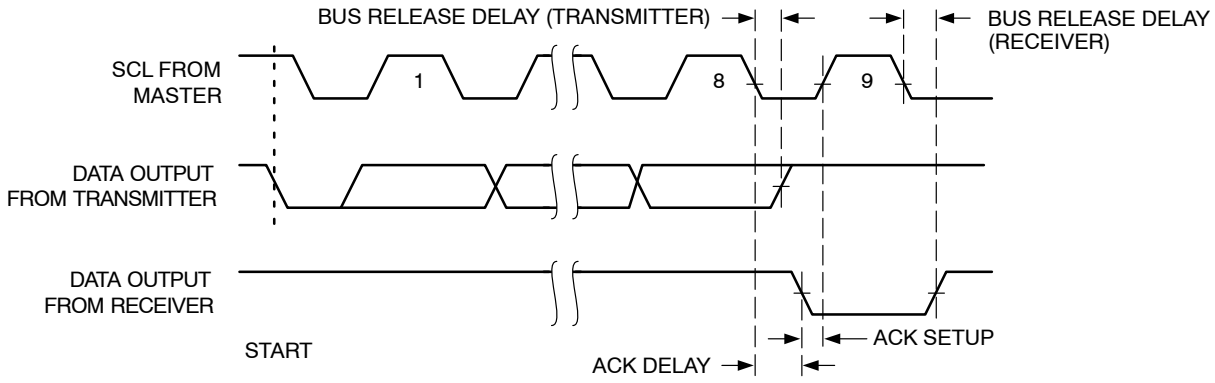


Figure 5. Acknowledge Timing

Device Addressing

DDC Interface

Both the DDC and DSP interfaces to the device are based on the I²C bus serial interface. All memory space operations are done at the A0/A1 DDC address pair. As such, all write operations to the memory space are done at DDC address A0h and all read operations of the memory space are done at DDC address A1h.

Figure 6 shows the bit sequence of a random read from anywhere within the memory space. The word offset determines which of the 256 bytes within segment 00h is being read. Here the segment 00h can be at the lower or upper bank depending on the configuration register.

Sequential reads can be done in much the same manner by reading successive bytes after each acknowledge without generating a stop condition. See Figure 7. The device automatically increments the word offset value (8−bit value) and with wraparound in the same segment 00h to read maximum of 256 bytes.

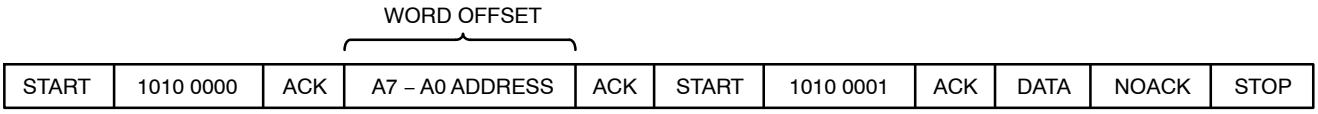


Figure 6. Random Access Read (Segment 00h only)

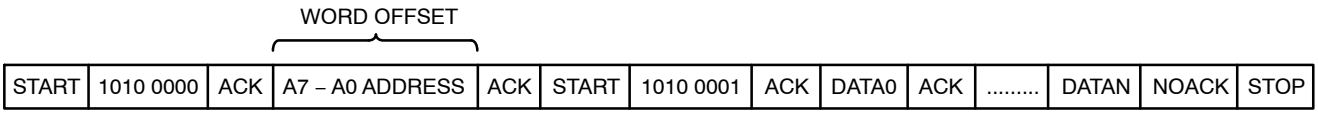


Figure 7. Sequential Read (Segment 00h only)

Figures 8 and 9 show the byte and page write respectively. The configuration register must have the WE bit set to 1 prior to any write on DDC Port. Only the segment 00h can be accessed of either lower or upper bank.

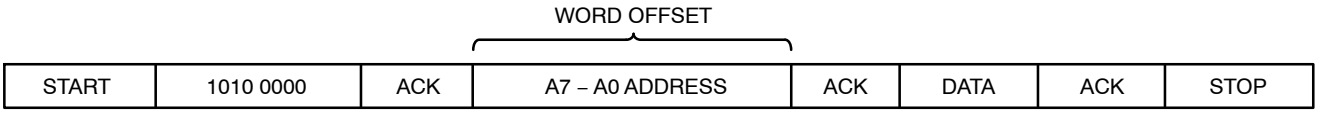


Figure 8. Byte Write (Segment 00h only)

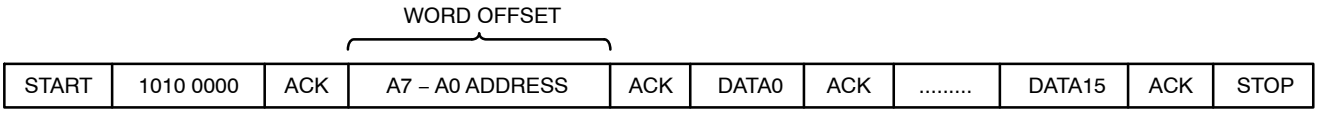


Figure 9. Page Write (Segment 00h only)

The segment pointer is at the address 60h and is write−only. This means that a memory access at 61h will give undefined results. The segment pointer is a volatile register. The device configuration register at 62/63 (hex) is a non−volatile register. The configuration register will be shipped in the erased (set to FFh) state.

The segment pointer is used to expand the available DDC address space while maintaining backward compatibility with older DDC interfaces such as DDC2B. For each value of the 8−bit segment pointer one segment (256 bytes) is available at the A0/A1 pair. The standard DDC 8−bit address is sufficient to address each of the 256 bytes within a segment. Note that if the segment pointer is set to 00h then the device will behave like a standard DDC2B EEPROM.

Read and write with segment pointer can expand the addressable memory to 512 bytes in each bank with wraparound to the next segment in the same bank only. The two banks can be individually selected by the configuration register and EDID Sel pin, as shown in Table 10. The segments are selected by the two bits S_1S_0 = 00 or 01 in the segment address.

Figures 10 to 13 show the random read, sequential read, byte write and page write.

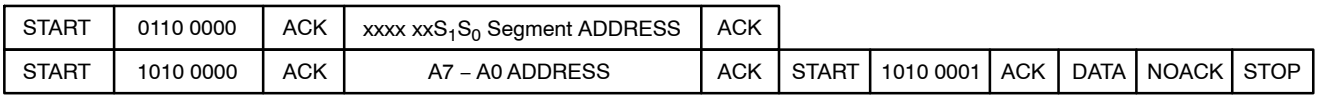


Figure 10. Random Access Read



Figure 11. Sequential Read

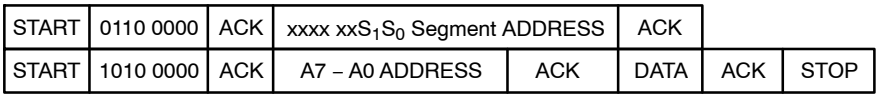


Figure 12. Byte Write

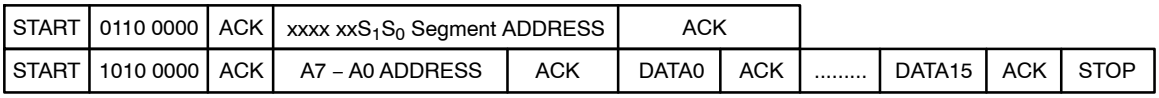


Figure 13. Page Write

DSP Interface

The DSP interface is similar to I^2C bus serial interface. Without the segment pointer, the maximum accessible memory space is 256 bytes of segment 00h only. In the sequential mode the wrap around will be in the same segment also. Figures 14 to 17 show the read and write on the DSP Port.

START	1010 0000	ACK	A7 – A0 ADDRESS	ACK	START	1010 0001	ACK	DATA	NOACK	STOP

Figure 14. Random Access Read

START	1010 0000	ACK	A7 – A0 ADDRESS	ACK	START	1010 0001	ACK	DATA0	ACK	.....	DATAN	NOACK	STOP

Figure 15. Sequential Read

START	1010 0000	ACK	A7 – A0 ADDRESS	ACK	DATA	ACK	STOP

Figure 16. Byte Write

START	1010 0000	ACK	A7 – A0 ADDRESS	ACK	DATA0	ACK	.....	DATA15	ACK	STOP

Figure 17. Page Write

The segment pointer is used to expand the available DSP port addressable memory to 1 k bytes, divided into four segments of 256 bytes each. The four segments are selected by two bits S_1S_0 = 00, 01, 10, 11 in the segment address. Figures 18 to 21 show the random read, sequential read, byte write and page write.

START	0110 0000	ACK	xxxx xxS_1S_0 Segment ADDRESS			ACK						
START	1010 0000	ACK	A7 – A0 ADDRESS		ACK	START	1010 0001	ACK	DATA		NOACK	STOP

Figure 18. Random Access Read

START	0110 0000	ACK	xxxx xxS_1S_0 Segment ADDRESS			ACK							
START	1010 0000	ACK	A7 – A0 ADDRESS	ACK	START	1010 0001	ACK	DATA0	ACK	.....	DATAN	NOACK	STOP

Figure 19. Sequential Read

START	0110 0000	ACK	xxxx xxS_1S_0 Segment ADDRESS			ACK			
START	1010 0000	ACK	A7 – A0 ADDRESS		ACK	DATA	ACK	STOP	

Figure 20. Byte Write

START	0110 0000	ACK	xxxx xxS_1S_0 Segment ADDRESS			ACK				
START	1010 0000	ACK	A7 – A0 ADDRESS	ACK	DATA0	ACK	.....	DATA15	ACK	STOP

Figure 21. Page Write

Arbitration

The device performs a simplistic arbitration between the DDC and DSP ports. While the arbitration scheme described is not foolproof, it does prevent most errors.

Arbitration logic within the device monitors activity on DDC_SCL and DSP_SCL. When both I^2C ports are idle, DDC_SCL and DSP_SCL are both high and the arbitration logic is inactive. When a START condition is detected on either port, the opposite port SCL line is pulled low, holding off activity on that port. When the initiating SCL line has remained high for one full second, the arbitration logic assumes that the initiating devices is finished and releases the other SCL line. If the non−initiating device has been waiting for access, it can now read or write the device.

Table 9. CONFIGURATION REGISTER

Register Function	MSB							LSB
	7	6	5	4	3	2	1	0
Configuration Register	X	X	X	X	WE	AB1	AB0	NB

Function Description

NB:	Number of memory banks in DDC port memory map. 0 = 2 Banks, 1 = 1 Bank
AB0:	Active Bank Control Bit 0 (See Table 10)
AB1:	Active Bank Control Bit 1 (See Table 10)
WE DDC:	Write Enable 0 = Write Disabled, 1= Write Enabled (Note 8)

8. WE affects only write operations from the DDC port, not the display port. The display port always has write access.

Table 10. CONFIGURATION REGISTER TRUTH TABLE

AB1	AB0	NB	EDID Select Pin	Active Bank
0	X	0	0	Lower Bank
0	X	0	1	Upper Bank
1	0	0	X	Lower Bank
1	1	0	X	Upper Bank
X	X	1	X	Lower (only) Bank

The configuration register is a non−volatile register and is available from either DSP or DDC port at address 62h / 63h for write and read resp.

Table 11. READ CONFIGURATION REGISTER

START	0110 0011	ACK	DATA	NO ACK	STOP

Table 12. WRITE CONFIGURATION REGISTER

START	0110 0010	ACK	DUMMY ADDRESS	ACK	XXXX WE AB1 AB0 NB	ACK	STOP

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAT24C208WI−GT3	24C208WI	SOIC−8	Industrial	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. All packages are RoHS−compliant (Lead−free, Halogen−free).
10. The standard lead finish is NiPdAu.
11. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

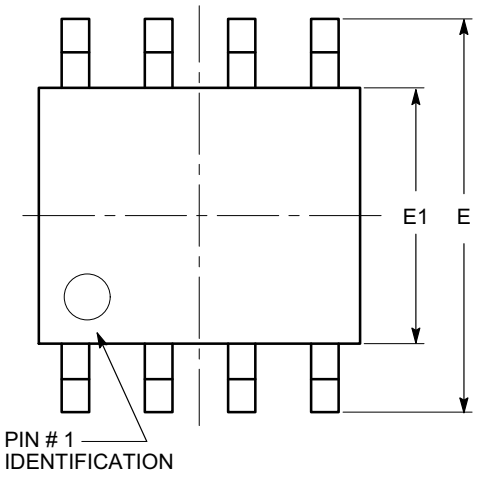
ON Semiconductor is licensed by the Philips Corporation to carry the I^2C bus protocol.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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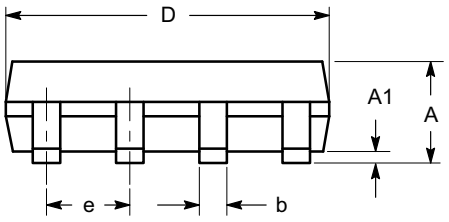
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CASE 751BD–01
ISSUE O

DATE 19 DEC 2008

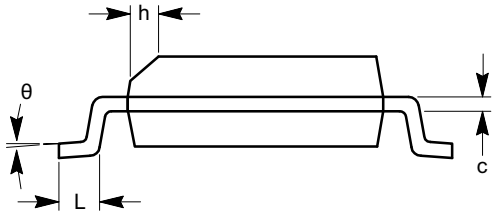


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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