Data Sheet | September 1998 | File Number 1174.4

Dual, 9MHz, Operational Transconductance Amplifier (OTA)

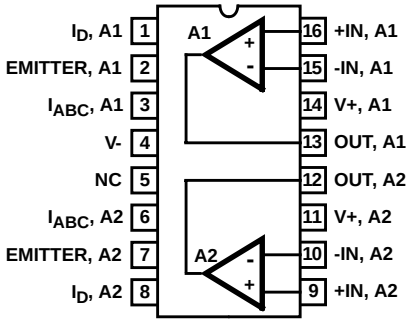
The CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset voltage variation with respect to changes in programming current. This design results in reduced “AGC thump,” an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer characteristics is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced in 1969, and it has since gained wide acceptance as a gateable, gain controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and high speed comparators.

For additional application information on this device and on OTAs in general, please refer to Application Notes: AN6818, AN6668, and AN6077.

Pinout

CA3280
(PDIP, CERDIP)
TOP VIEW



Features

- Low Initial Input Offset Voltage: 500µV (Max) (CA3280A)
- Low Offset Voltage Change vs I_{ABC}: <500µV (Typ) for All Types
- Low Offset Voltage Drift: 5µV/^{O}C (Max) (CA3280A)
- Excellent Matching of the Two Amplifiers for All Characteristics
- Internal Current-Driven Linearizing Diodes Reduce the External Input Current to an Offset Component
- Flexible Supply Voltage Range. . . . . ±2V to ±15V

Applications

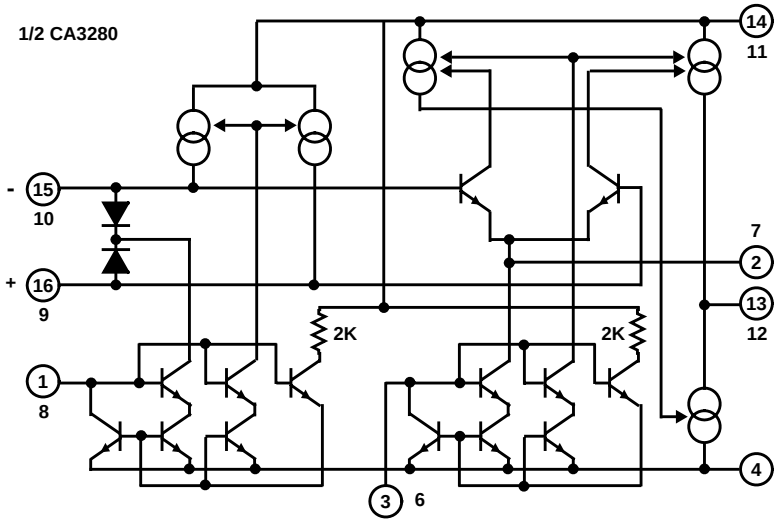
- Voltage Controlled Amplifiers
- Voltage Controlled Oscillators
- Multipliers
- Demodulators
- Sample and Hold
- Instrumentation Amplifiers
- Function Generators
- Triangle Wave-to-Sine Wave Converters
- Comparators
- Audio Preamplifier

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3280AE	-55 to 125	16 Ld PDIP	E16.3
CA3280E	0 to 70	16 Ld PDIP	E16.3
CA3280AF3	-55 to 125	16 Ld CERDIP	F16.3

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Diagram



Absolute Maximum Ratings

Supply Voltage (Between V+ and V-) . . . . . +36V
Differential Input Voltage 5V
Input Voltage Range . . . . . V+ to V-
Input Current at $I_D = 0$ 100µA
Amplifier Bias Current (I_{ABC}) 10mA
Output Short Circuit Duration (Note 1) . . . . . Indefinite
Linearizing Diode Bias Current, I_D 5mA
Peak Input Current with Linearizing Diode . . . . . $\pm I_D$

Operating Conditions

Temperature Range
CA3280 . . . . . 0^oC to 70^oC
CA3280A . . . . . -55^oC to 125^oC
Supply Voltage Range (Typ) . . . . . ±2V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	65	16
PDIP Package	100	N/A

Maximum Junction Temperature (CERDIP Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

For Equipment Design, at $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		CA3280 MIN	CA3280 TYP	CA3280 MAX	CA3280A MIN	CA3280A TYP	CA3280A MAX	UNITS
Input Offset Voltage	V_{IO}	I_{ABC} = 1mA		-	-	3	-	-	0.5	mV
		I_{ABC} = 100µA		-	0.7	3	-	0.25	0.5	mV
		I_{ABC} = 10µA		-	-	3	-	-	0.5	mV
		I_{ABC} = 1mA to 10µA, T_A = Full Temp. Range		-	0.8	4	-	0.8	1.5	mV
Input Offset Voltage Drift	$\lvert\Delta V_{IO}\rvert$	I_{ABC} = 1µA to 1mA		-	0.5	1	-	0.5	1	mV
		I_{ABC} = 100µA, T_A = Full Temperature Range		-	5	-	-	3	5	µV/^oC
Amplifier Bias Voltage	V_{ABC}	I_{ABC} = 100µA		-	1.2	-	-	1.2	-	V
Peak Output Voltage	V_{OM}^+	I_{ABC} = 500mA		12	13.7	-	12.5	13.7	-	V
	V_{OM}^-			12	-14.3	-	-13.3	-14.3	-	V
	V_{OM}^+	I_{ABC} = 5µA		12	13.9	-	12.5	13.9	-	V
	V_{OM}^-			12	-14.5	-	-13.5	-14.5	-	V
Common Mode Input Voltage Range	V_{ICR}	I_{ABC} = 100µA		-13	-	13	-13	-	13	V
Noise Voltage	e_N	I_{ABC} = 500µA	10Hz	-	20	-	-	20	-	nV/$\sqrt{Hz}$
			1kHz	-	8	-	-	8	-	nV/$\sqrt{Hz}$
			10kHz	-	7	-	-	7	-	nV/$\sqrt{Hz}$
Input Offset Current	I_{IO}	I_{ABC} = 500µA		-Z	0.3	0.7	-	0.3	0.7	µA
Input Bias Current	I_{IB}	I_{ABC} = 500µA		-	1.8	5	-	1.8	5	µA
		I_{ABC} = 500µA, T_A = Full Temperature Range		-	3	8	-	3	8	µA
Peak Output Current	I_{OM}^+	I_{ABC} = 500µA	Source	350	410	650	350	410	650	µA
	I_{OM}^-		Sink	-350	-410	-650	-350	-410	-650	µA
	I_{OM}^+	I_{ABC} = 5µA	Source	3	4.1	7	3	4.1	7	µA
	I_{OM}^-		Sink	-3	-4.1	-7	-3	-4.1	-7	µA

Electrical Specifications For Equipment Design, at $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA3280			CA3280A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Peak Output Current Sink and Source	I_{OM}^-, I_{OM}^+	I_{ABC} = 500µA, T_A = Full Temperature Range	350	450	550	350	450	550	µA
Linearization Diodes		I_D = 100µA	-	10	-	-	10	-	µA
Offset Current		I_D = 10µA	-	0.5	1	-	0.5	1	µA
Dynamic Impedance		I_D = 100µA	-	700	-	-	700	-	Ω
Diode Network Supply Current		I_{ABC} = 100µA	250	400	800	250	400	800	µA
Amplifier Supply Current (Per Amplifier)	I+	I_{ABC} = 500µA	-	2	2.4	-	2	2.4	mA
Amplifier Output Leakage Current	I_{OL}	I_{ABC} = 0, V_O = 0V	-	0.015	0.1	-	0.015	0.1	nA
		I_{ABC} = 0, V_O = 30V	-	0.15	1	-	0.15	1	nA
Common Mode Rejection Ratio	CMRR	I_{ABC} = 100µA	80	100	-	94	100	-	dB
Power Supply Rejection Ratio	PSRR	I_{ABC} = 100µA	86	105	-	94	105	-	dB
Open Loop Voltage Gain	A_{OL}	I_{ABC} = 100µA, $R_L = \infty$, $V_O = 20V_{P-P}$	94	100	-	94	100	-	dB
			50	100	-	50	100	-	kV/V
Forward Transconductance	G_M	I_{ABC} = 50µA, Large Signal	-	0.8	1.2	-	0.8	1.2	mS
	g_M	I_{ABC} = 1mA, Small Signal	-	16	22	-	16	22	mS
Input Resistance	R_I	I_{ABC} = 10µA	0.5	-	-	0.5	-	-	MΩ
Channel Separation		f = 1kHz	-	94	-	-	94	-	dB
Open Loop Total Harmonic Distortion	THD	f = 1kHz, I_{ABC} = 1.5mA, R_L = 15kΩ, $V_O = 20V_{P-P}$	-	0.4	-	-	0.4	-	%
Bandwidth	f_T	I_{ABC} = 1mA, R_L = 100Ω	-	9	-	-	9	-	MHz
Slew Rate, Open Loop	SR	I_{ABC} = 1mA	-	125	-	-	125	-	V/µs
Capacitance	C_I	I_{ABC} = 100µA Input	-	4.5	-	-	4.5	-	pF
	C_O	Output	-	7.5	-	-	7.5	-	pF
Output Resistance	R_O	I_{ABC} = 100µA	-	63	-	-	63	-	MΩ

Test Circuits and Waveforms

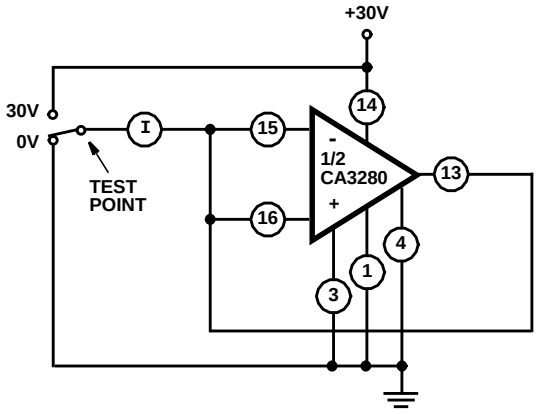


FIGURE 1. LEAKAGE CURRENT TEST CIRCUIT

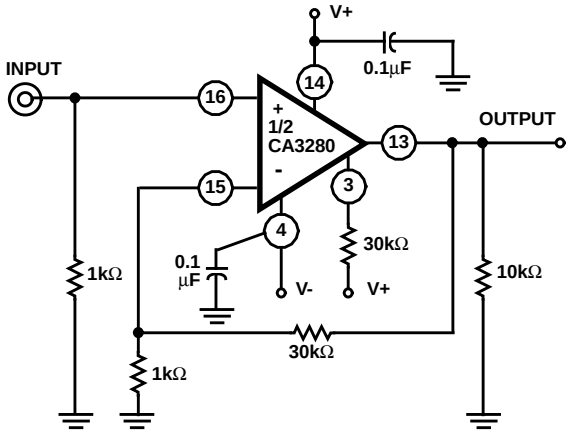
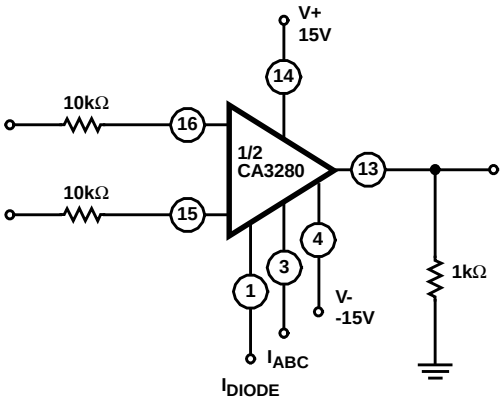
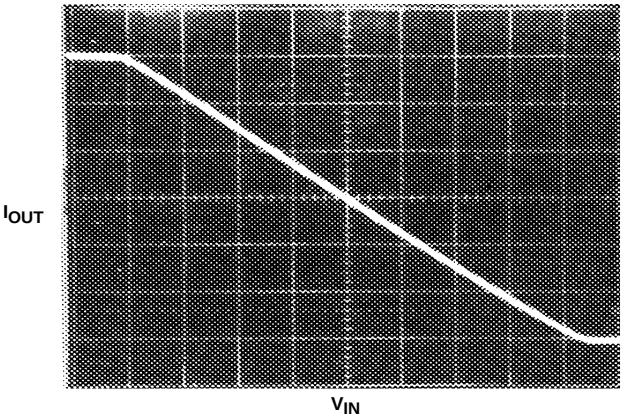


FIGURE 2. CHANNEL SEPARATION TEST CIRCUIT

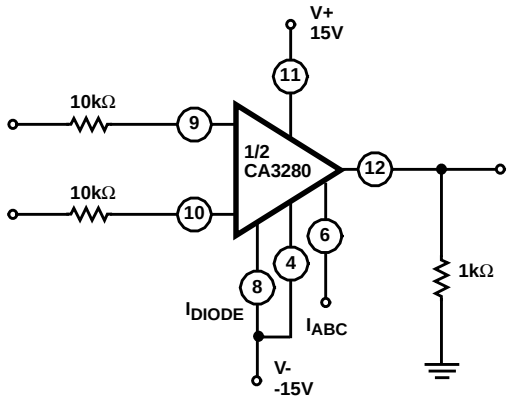
Test Circuits and Waveforms (Continued)

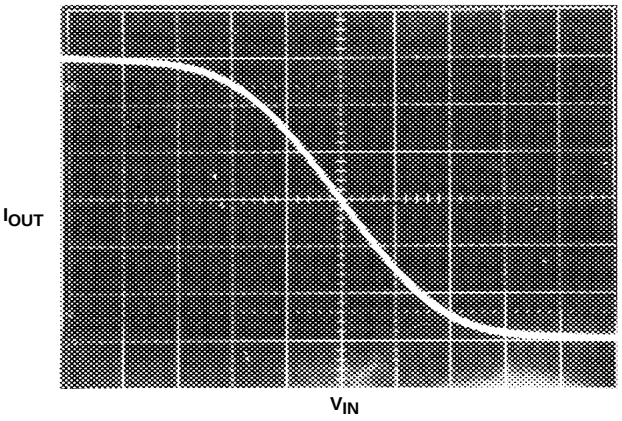




I_{ABC} = 650µA, I_D = 200µA; Vertical = 200µA/Div.; Horizontal = 1V/Div.

FIGURE 3A. EFFECTS OF DIODE LINEARIZATION, WITH DIODE PROGRAMMING TERMINAL ACTIVE





I_{ABC} = 650µA; I_D = 0; Vertical = 200µA/Div.; Horizontal = 25mV/Div.

FIGURE 3B. WITH DIODE PROGRAMMING TERMINAL CUTOFF

FIGURE 3. CA3280 TRANSFER CHARACTERISTICS

Application Information

Figures 4 and 5 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common mode range of the CA3280.

Typical Applications

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single ended converters, as shown in Figure 6. A matched resistor network requires ratio matching of 0.01% or trimming for 80dB of common-mode rejection. The CA3280, with its excellent common mode rejection ratio, is capable of converting a small (±25mV) differential input signal to a single-ended output without the need for a matched resistor network.

Figure 7 shows the CA3280 in a typical gain control application. Gain control can be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely $g_M R_L$. For example, with an I_{ABC} of 1mA, the g_M is approximately 16mS. With the CA3280 operating into a 5kΩ resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance

of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

Figure 10 shows a triangle wave to sine wave converter using the CA3280. Two 100kΩ resistors are connected between the differential amplifier emitters and V+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is appropriately 0.37% for this circuit.

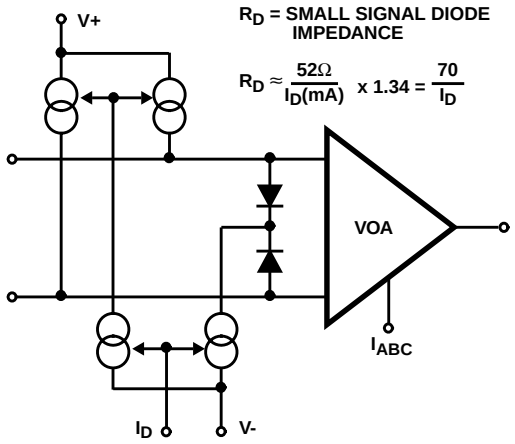


FIGURE 4. VOA SHOWING LINEARIZATION DIODES AND CURRENT DRIVE

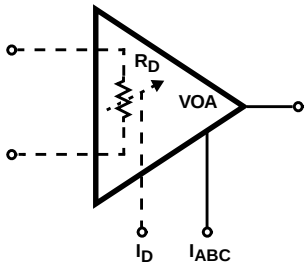


FIGURE 5. BLOCK DIAGRAM OF LINEARIZED VOA

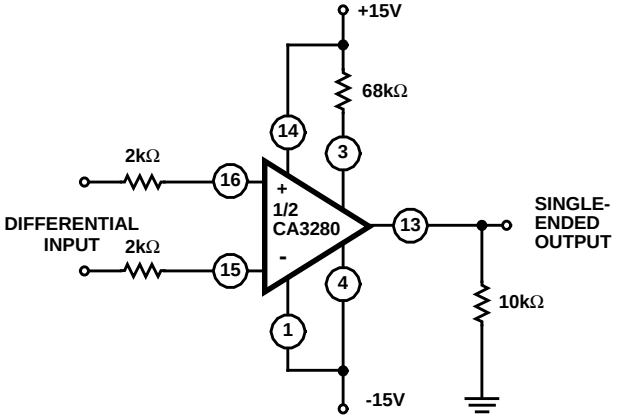


FIGURE 6. DIFFERENTIAL TO SINGLE ENDED CONVERTER

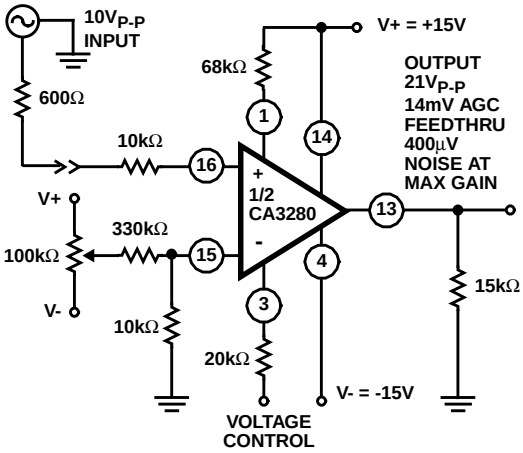


FIGURE 7. TYPICAL GAIN CONTROL CIRCUIT

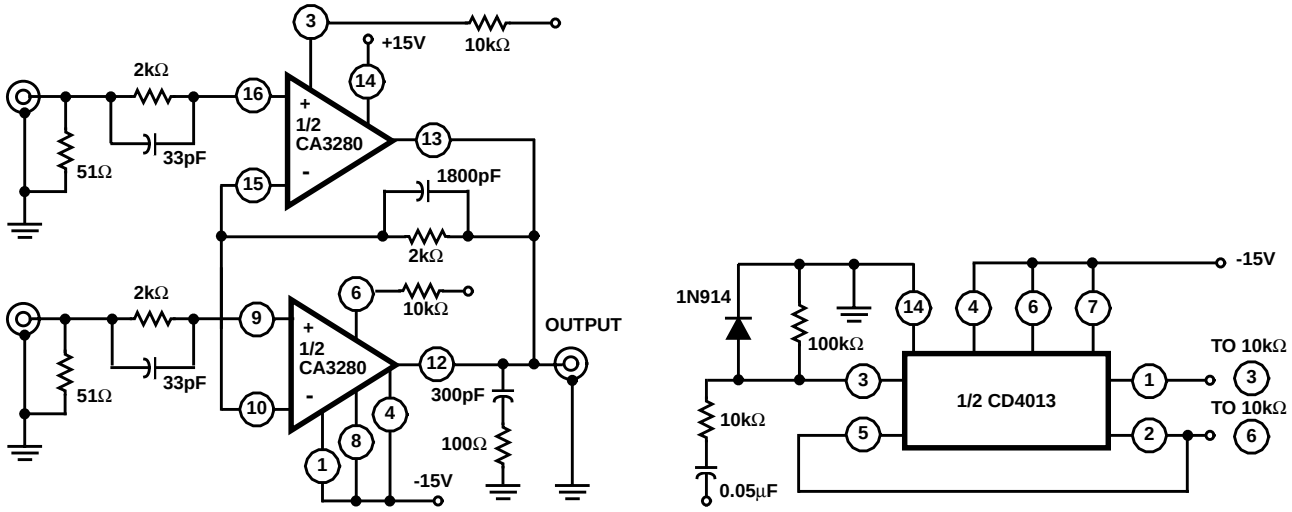


FIGURE 8. TWO CHANNEL LINEAR MULTIPLEXER

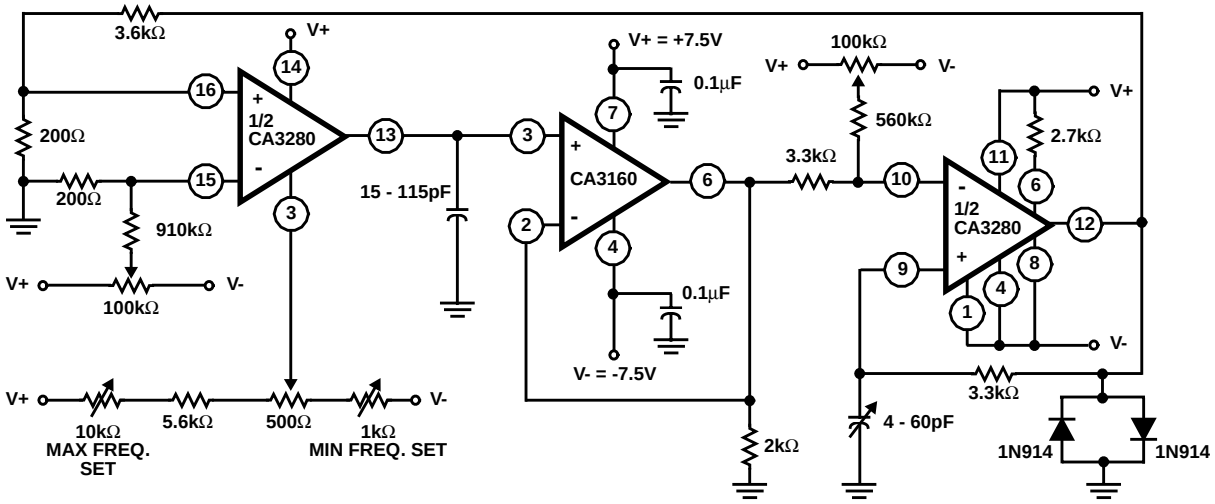


FIGURE 9. CA3280 USED IN CONJUNCTION WITH A CA3160 TO PROVIDE A FUNCTION GENERATOR WITH A TUNABLE RANGE OF 2Hz TO 1MHz

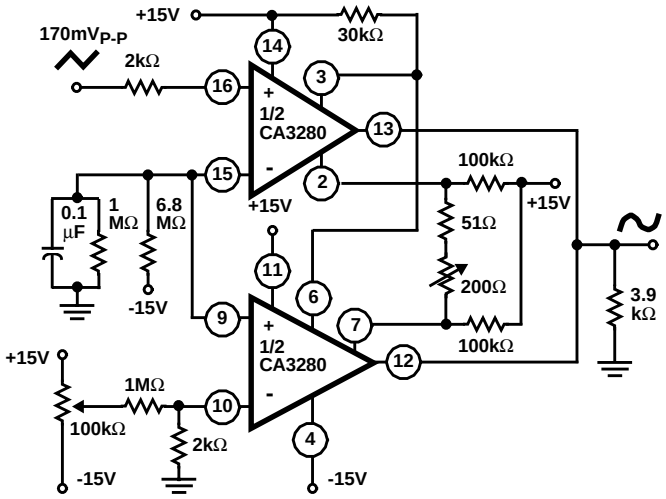


FIGURE 10. TRIANGLE WAVE-TO-SINE WAVE CONVERTER

Typical Performance Curves

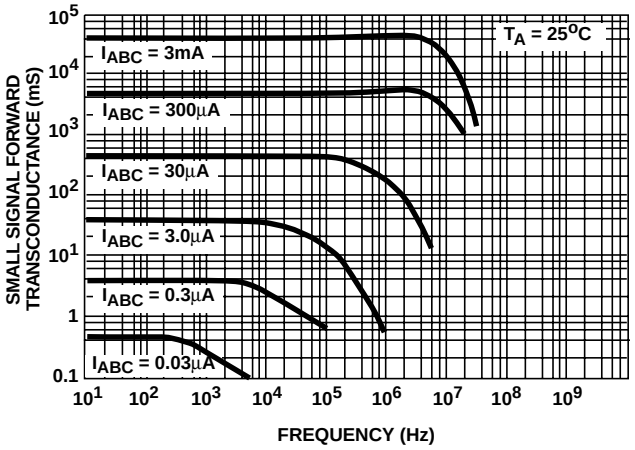


FIGURE 11. AMPLIFIER GAIN vs FREQUENCY

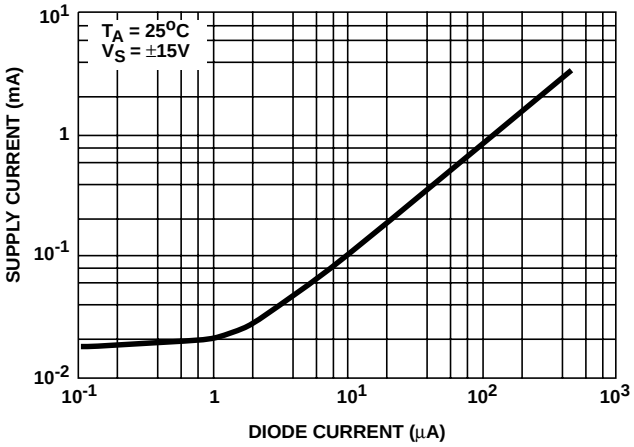


FIGURE 12. SUPPLY CURRENT vs DIODE CURRENT

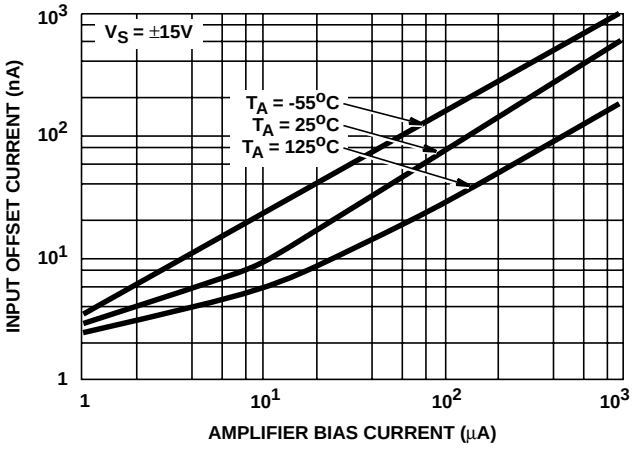


FIGURE 13. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT

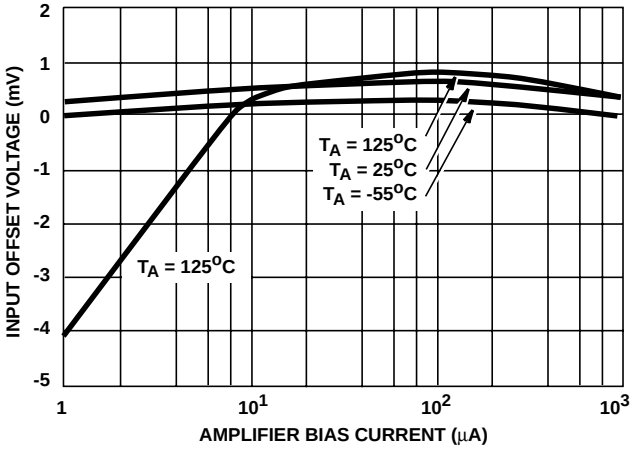


FIGURE 14. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT

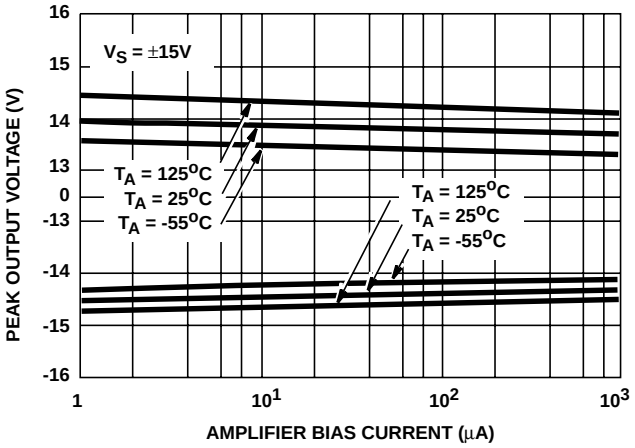


FIGURE 15. PEAK OUTPUT VOLTAGE vs AMPLIFIER BIAS CURRENT

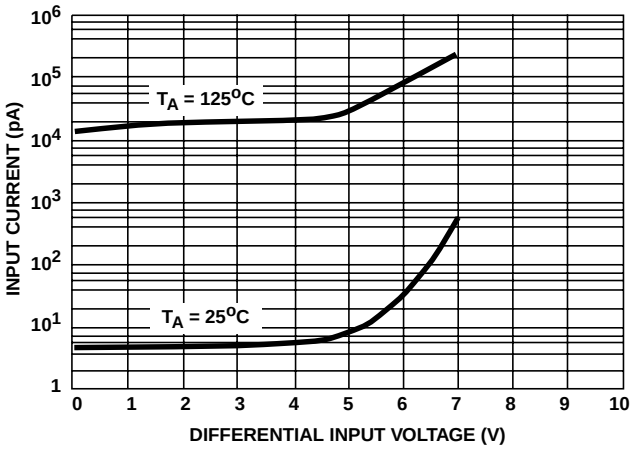


FIGURE 16. INPUT CURRENT vs INPUT DIFFERENTIAL VOLTAGE

Typical Performance Curves (Continued)

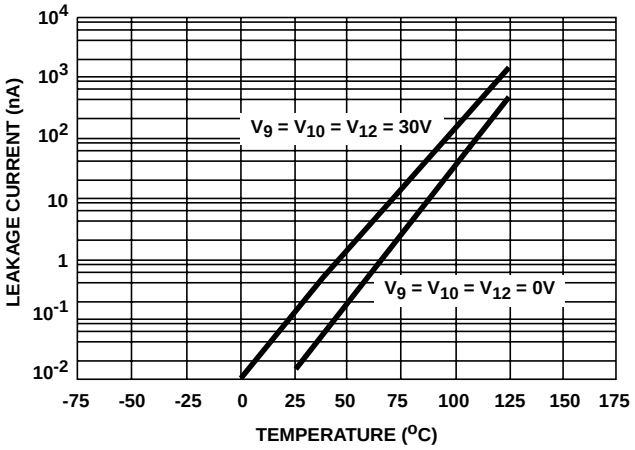


FIGURE 17. LEAKAGE CURRENT vs TEMPERATURE

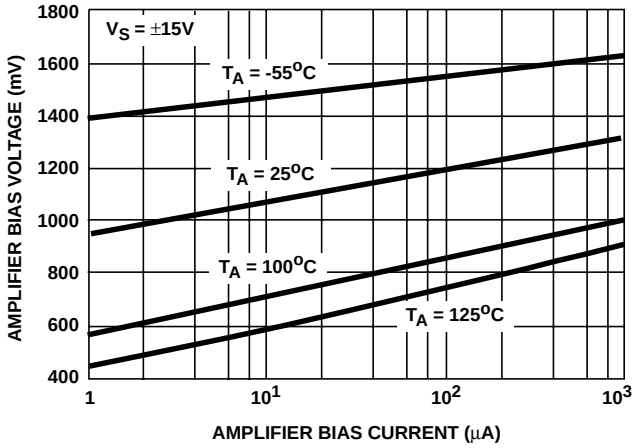


FIGURE 18. AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT

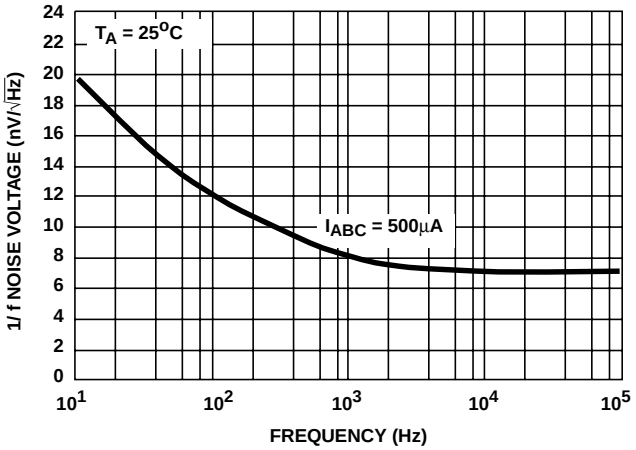


FIGURE 19. 1/f NOISE vs FREQUENCY

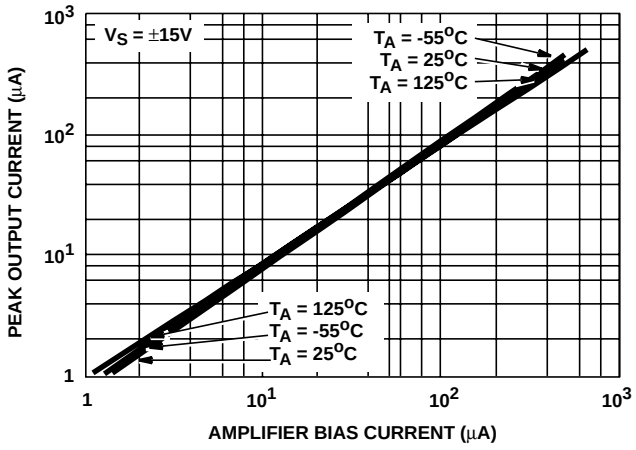


FIGURE 20. PEAK OUTPUT CURRENT vs AMPLIFIER BIAS CURRENT

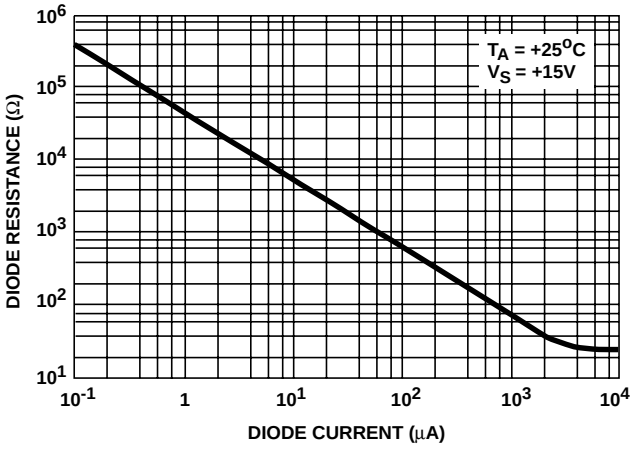


FIGURE 21. DIODE RESISTANCE vs DIODE CURRENT

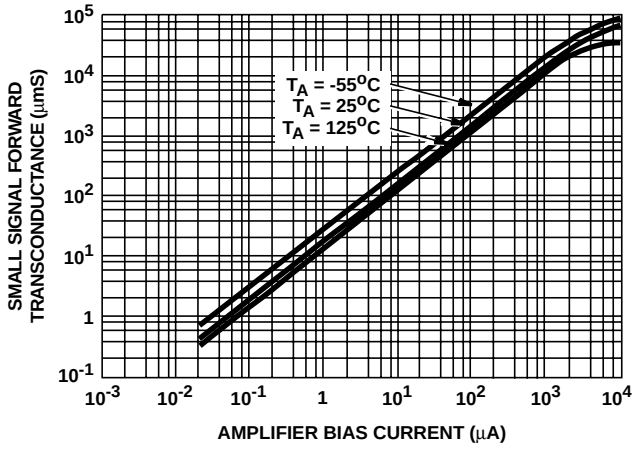


FIGURE 22. AMPLIFIER GAIN vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

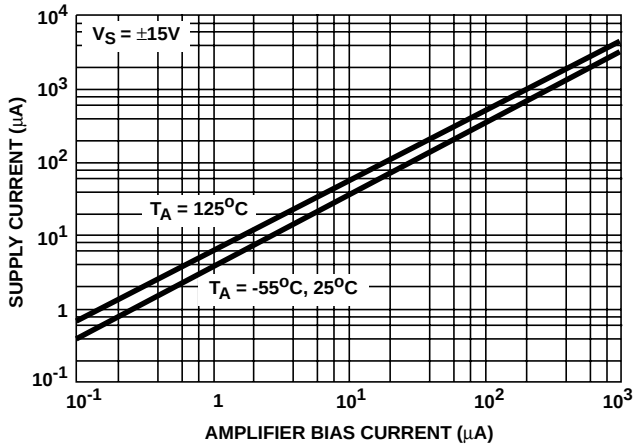


FIGURE 23. SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT

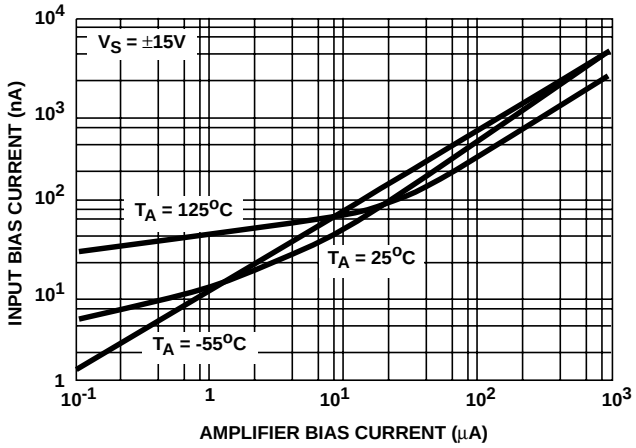
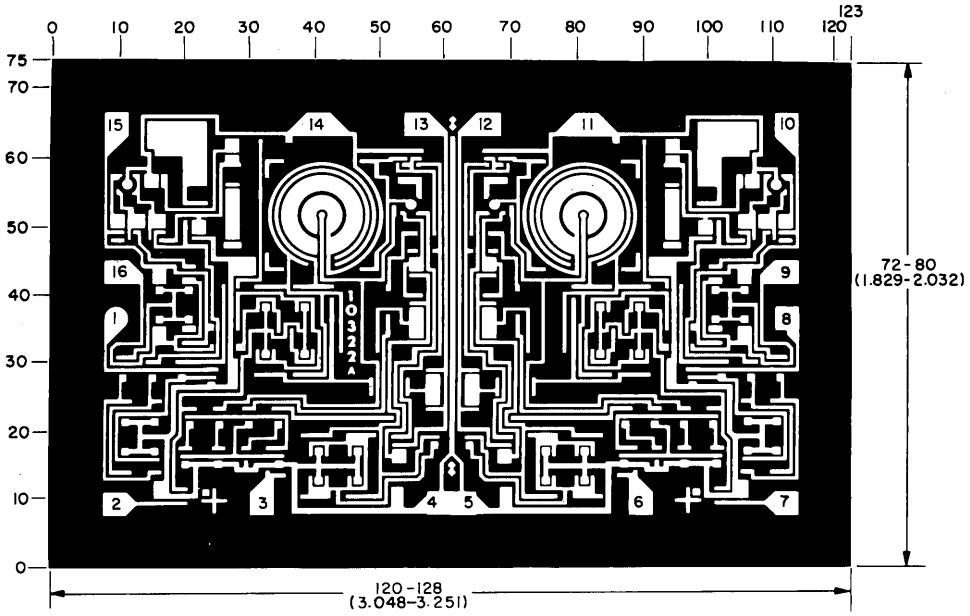


FIGURE 24. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT

Metallization Mask Layout



Dimensions in parentheses are in millimeters and derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^o instead of 90^o with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.