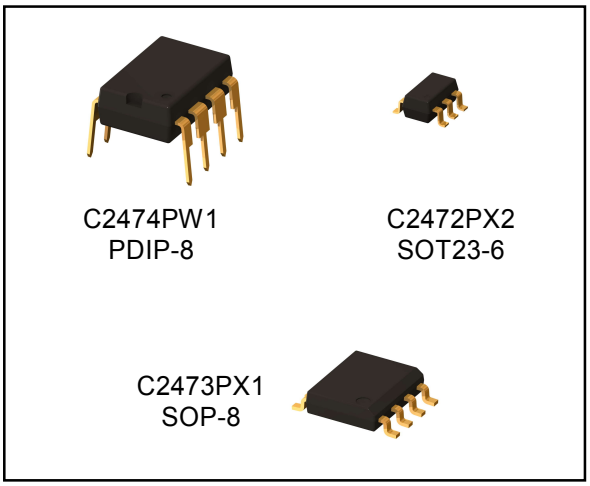
C2472, C2473 and C2474 Datasheet

RDFC Controllers for Offline Applications



ADVANTAGES

- Low system component count
- High average efficiency
- Low standby power consumption
- EMI compliance without extra components
- High isolation & surge voltage withstand
- High power density in very small size

FEATURES

- Highly integrated CMOS controller IC
- Low cost package options
- Drive suitable for low cost bipolar power transistors
- Resonant switching for high efficiency and low EMI
- Frequency optimised for power circuit parasitics
- Protection against overload, over-temperature and under-voltage

APPLICATIONS

External AC/DC charger/adaptor (single voltage input) e.g. cordless phones, portable electric tools.

Embedded PSU (single voltage input) e.g. set-top boxes, DVD players, audio products, domestic appliances.

OVERVIEW

The C2472, C2473 and C2474 controllers use CamSemi's Resonant Discontinuous Forward Converter (RDFC) topology to create a high efficiency, low cost alternative to line-frequency transformer PSUs. By operating in resonant mode, EMI is greatly reduced, enabling the replacement of linear PSUs in demanding applications such as audio products and cordless phone chargers. The C2472, C2473 and C2474 controllers also offer overload protection which is usually associated with more expensive switch mode solutions.

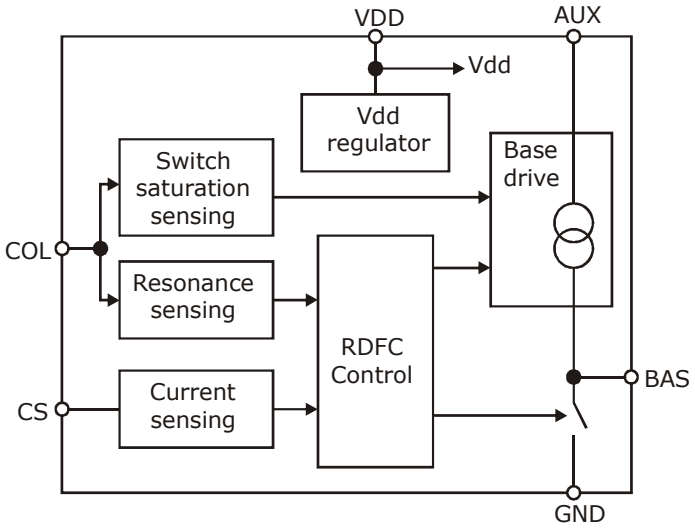


Figure 1: Block Diagram of the C2472, C2473 and C2474 Controller ICs

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PIN DEFINITIONS

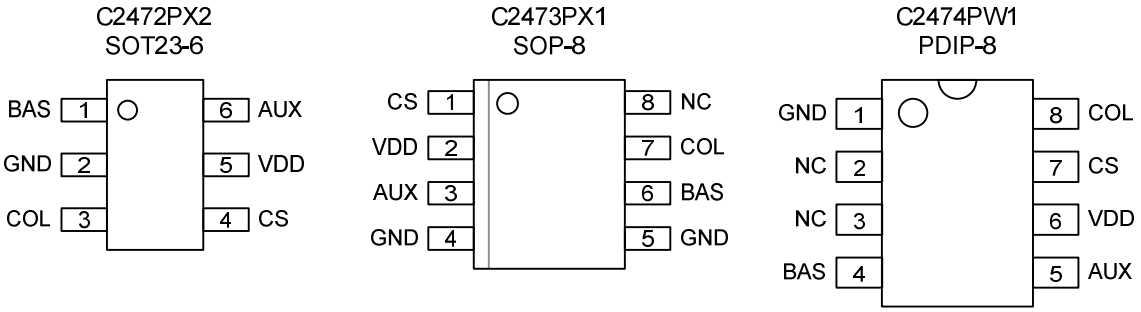


Figure 2: C2472, C2473 and C2474 Pin Assignment
(drawings are not to scale)

VDD Pin

The VDD pin supplies power to the controller and is maintained at the correct voltage (nominally 3.3 V) by an internal shunt regulator.

COL Pin

The COL pin is used to sense the collector voltage of the primary switching transistor, via a c oupling capacitor, to control the timing and current levels of the signals produced on the BAS pin.

CS Pin

The CS pin senses the primary switch current via the current sensing resistor. The voltage sensed on this pin is used to control the operating modes to manage standby and overload protection. Operating characteristics are programmed via two external resistors.

AUX Pin

The AUX pin provides the supply current for the internal base driver block. In most applications, the AUX pin is connected to the external supply rail via an NPN transistor and a current-limiting resistor to set the maximum base current; however, in low power applications the AUX pin can be connected to the VDD pin via the limiting resistor, with some compromise on the standby power consumption.

BAS Pin

The BAS pin switches the external bipolar primary switch transistor on and off. The current supplied to the switch transistor is controlled to minimize the switching losses and thereby help optimize overall system efficiency.

GND Pin

GND pins provide the ground reference. Where the device has multiple GND pins, all must be connected to a common, low impedance path.

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TYPICAL APPLICATION CIRCUIT

The C2472, C2473 and C2474 controllers are intended primarily for single input voltage AC/DC applications, such as replacement of line frequency linear transformer power supplies. These versatile controllers support a wide range of applications at low cost. A typical circuit configuration is shown in Figure 3.

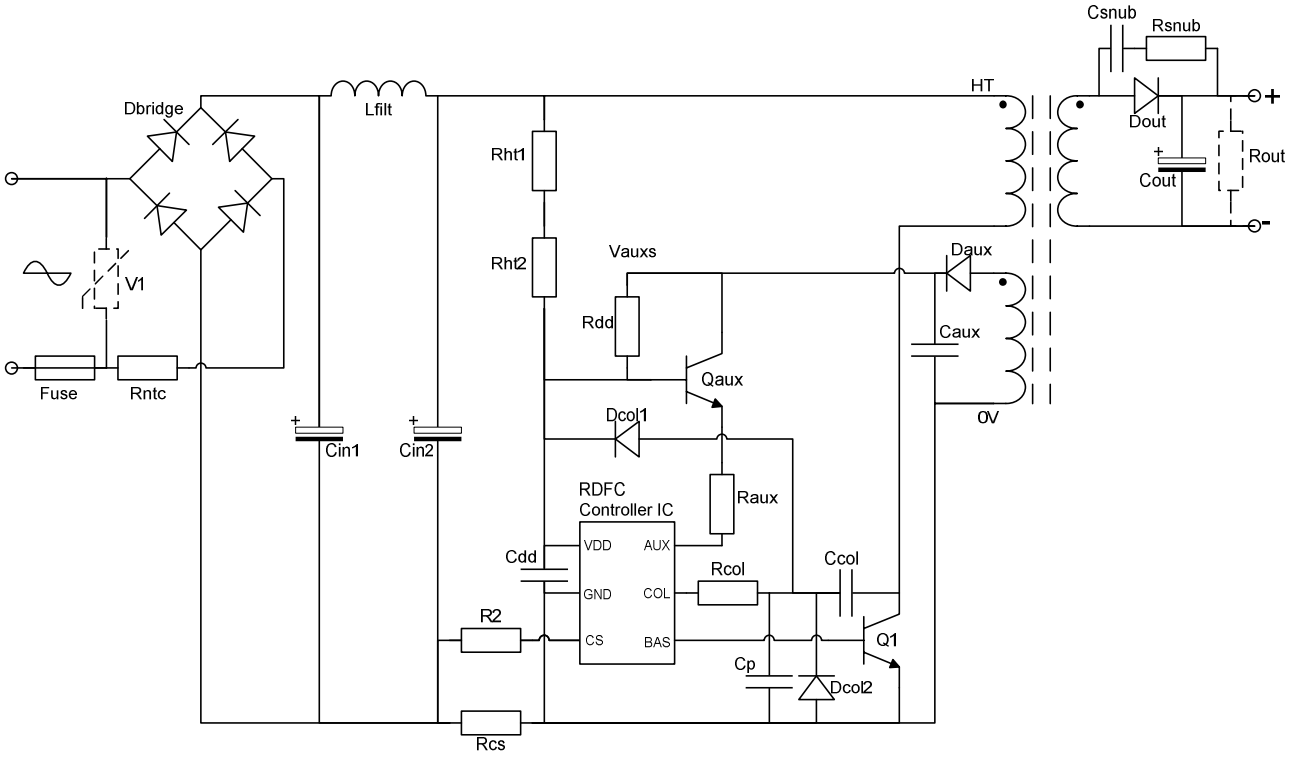


Figure 3: Typical RDFC Application Schematic

Typical 12 W Charger Performance

Input	115 V ac
Output	12 V, 1 A dc
Efficiency	> 80%
No-load power input	< 150 mW

Typical Maximum Application Rated Power

Power Switch (Q1) Gain	115 Vac	230 Vac
Standard	20 W	40 W
High	40 W	60 W

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PRINCIPLE OF OPERATION

Power-Up/Power-Down Sequences

The C2472, C2473 and C2474 controllers are powered via their VDD pins. When mains voltage is first applied, a small amount of current ($I_{DDSLEEP}$) is drawn from the rectified mains input via high value start up resistors (Rht1 and Rht2 in Figure 3). When the voltage on the VDD pin (V_{DD}) reaches a level V_{OVDTHR} the controller wakes up, demands more supply current (I_{DDWAKE}) and enters the Start-up state (see Figure 4). The controller stays in Start-up for a short time during which internal circuit blocks are enabled and then changes to Active operation. In both Start-up and Active states, the controller uses an internal shunt regulator to regulate the V_{DD} rail voltage; the regulator is disabled in Sleep. A higher regulation voltage is applied during Start-up ($V_{DDREG(S)}$) than during Active operation ($V_{DDREG(R)}$) to help provide sufficient V_{DD} before the Auxiliary supply from the transformer rises to maintain V_{DD}.

If the VDD pin voltage drops below V_{UVDTHR} the controller goes back to Sleep, reducing the supply current demand. The system will restart when input power is restored. To achieve a smooth power up sequence the V_{DD} reservoir capacitor needs to be large enough to sustain the supply above V_{UVDTHR} over the Start-up period.

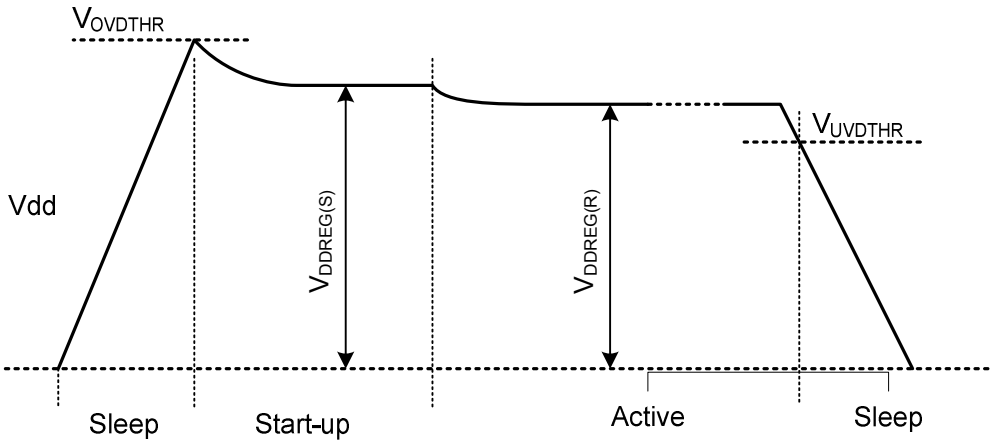


Figure 4: VDD Pin Waveform (V_{DD}) During Initial Power-up and Power-down

State	Description
Sleep	From initial application of power or from Active state if V_{DD} falls below V_{UVDTHR}, the controller changes to Sleep state. Non-essential controller circuits are powered down and the external switching transistor (Q1) is held off. Exit from Sleep state occurs when V_{DD} rises above V_{OVDTHR} and the controller moves to the Start-up state.
Start-up	When the Start-up state is entered, internal controller circuits are activated and power conversion begins (Standby mode – see Table 2). In Start-up the on-chip shunt regulator stabilises V_{DD} to an intermediate value, $V_{DDREG(S)}$. After a preset time, the controller changes from Start-up to Active operation.
Active	Converter operation continues, the shunt regulator controls V_{DD} to the lower $V_{DDREG(R)}$. If V_{DD} falls below V_{UVDTHR} the controller ceases converter operation and reverts to Sleep state.

Table 1: Summary of RDFC Controller States

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Start-up and Active State Power Conversion Modes

In the Start-up and Active states the C2472, C2473 and C2474 ICs have several modes for controlling power conversion that are designed to achieve maximum efficiency and to limit power (current) across a wide range of loads. Refer to Table 2 for a summary of each mode.

Mode	Typical Load Range	Description
Standby	I_{OUT} ≥ 0% to ~20% of rated current	Standby mode reduces power consumption at low loads. It achieves this by progressively reducing the on-time then by increasing the off-time as the load decreases. As load increases, the converter duty is increased until the controller returns to Normal mode. Typically, mains ripple causes change of operating mode during each mains half-cycle, with the converter moving to lower-power modes between peaks of the mains voltage.
Normal	I_{OUT} > ~20% to 100% of rated current	Normal mode is used for steady state power delivery. During Normal mode the power device switches in a fully resonant minimum-voltage-switching waveform, with the off-time determined by the transformer resonance (T_{RES}) and the on-time being equal to 75% of the off time. A low level of primary switch current, sensed via the CS pin voltage, causes the controller to change to Standby mode and a high level to Overload mode.
Overload	I_{OUT} >~100% rated current	Overload mode is activated at high output loads. In this mode the on-time of the primary switch is terminated early (before 75% of T_{RES}) when the primary current exceeds a preset maximum, thereby protecting the primary switch and limiting the output current. This results in reduction of the output voltage. Heavy overload (sensed by the on-period of the primary switch reducing below a preset time) causes Foldback mode to be entered.
Foldback	V_{OUT} < ~70% rated output	Foldback mode is entered from the Overload mode. In this mode the controller reduces the on/off duty cycle to protect the power supply and any connected load by both shortening the on-period and increasing the off-period of the primary switch. Converter cycles continue to maintain auxiliary power to the controller. The controller exits the Foldback mode and enters the Power Burst mode after a fixed number of power conversion cycles.
Power Burst	V_{OUT} < ~70% rated output	Power Burst mode is entered periodically from Foldback mode in order to restart the power supply output. In Power Burst mode, the controller operates at maximum delivered power for a set number of power converter cycles. At the end of the burst, if the load is not excessive, the converter goes to Normal mode; otherwise it reverts to Foldback mode.

Table 2: Summary of Active Operating Modes

When the controller goes from Sleep to Start-up state, its power conversion mode is set to Standby. Typically the converter output voltage is low at this time so the primary switch current is high during the first few converter cycles. This causes the operating mode to change quickly to Normal or Overload mode.

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RDFC Power Supply I-V Characteristic

Figure 5 illustrates a typical RDFC power supply characteristic with the various Active state modes of operation identified. I_{NOM} and V_{NOM} are the nominal output voltage and current drawn by the load at the rated power of the application circuit.

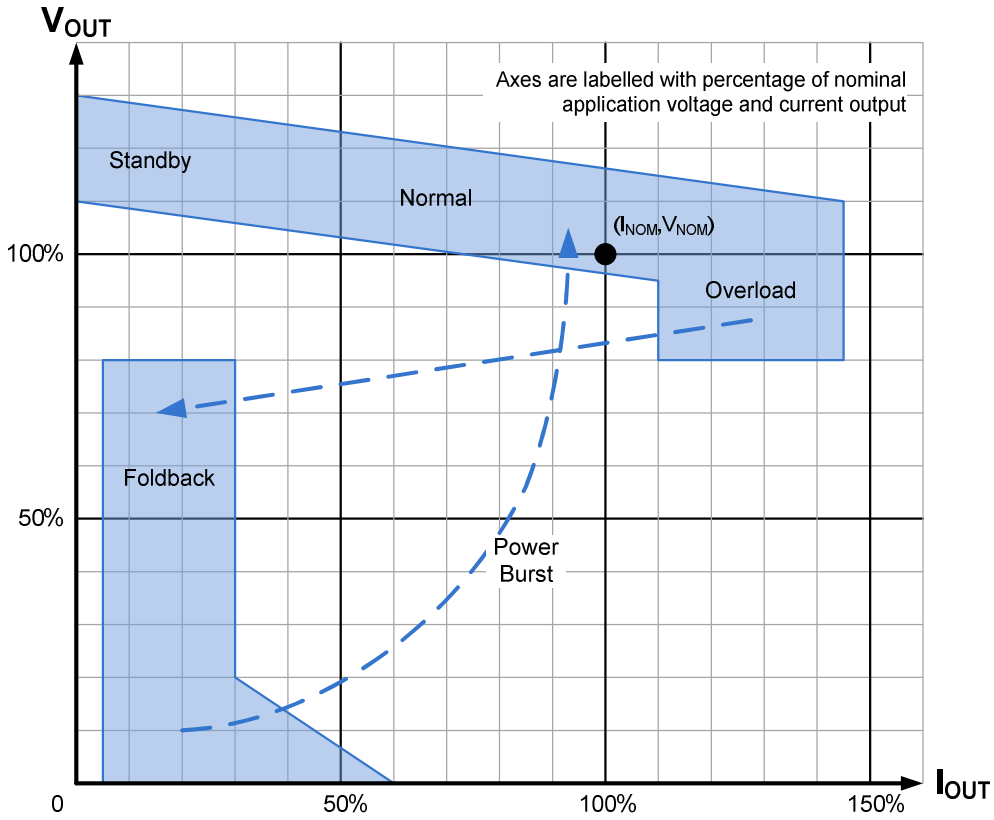


Figure 5: Typical RDFC Power Supply Characteristic Indicating Different Active Modes of Operation

The exact thresholds for transition between modes depend on specific application characteristics, controller internal clock frequency (F_{CLK}) and CS pin thresholds (V_{OCPH} and V_{OCPL}). These parameters and their effects are explained later.

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Switching Waveforms

The collector voltage (V_{CE}) and current (I_C) waveforms of the primary switching transistor (Q1 in Figure 3) are shown in Figure 6. T_{RES} is the duration of the transformer resonance during the off period. Note that in Overload mode, the primary switch Q1 is turned off when the current exceeds the protection level OCPH (sensed by the CS pin voltage).

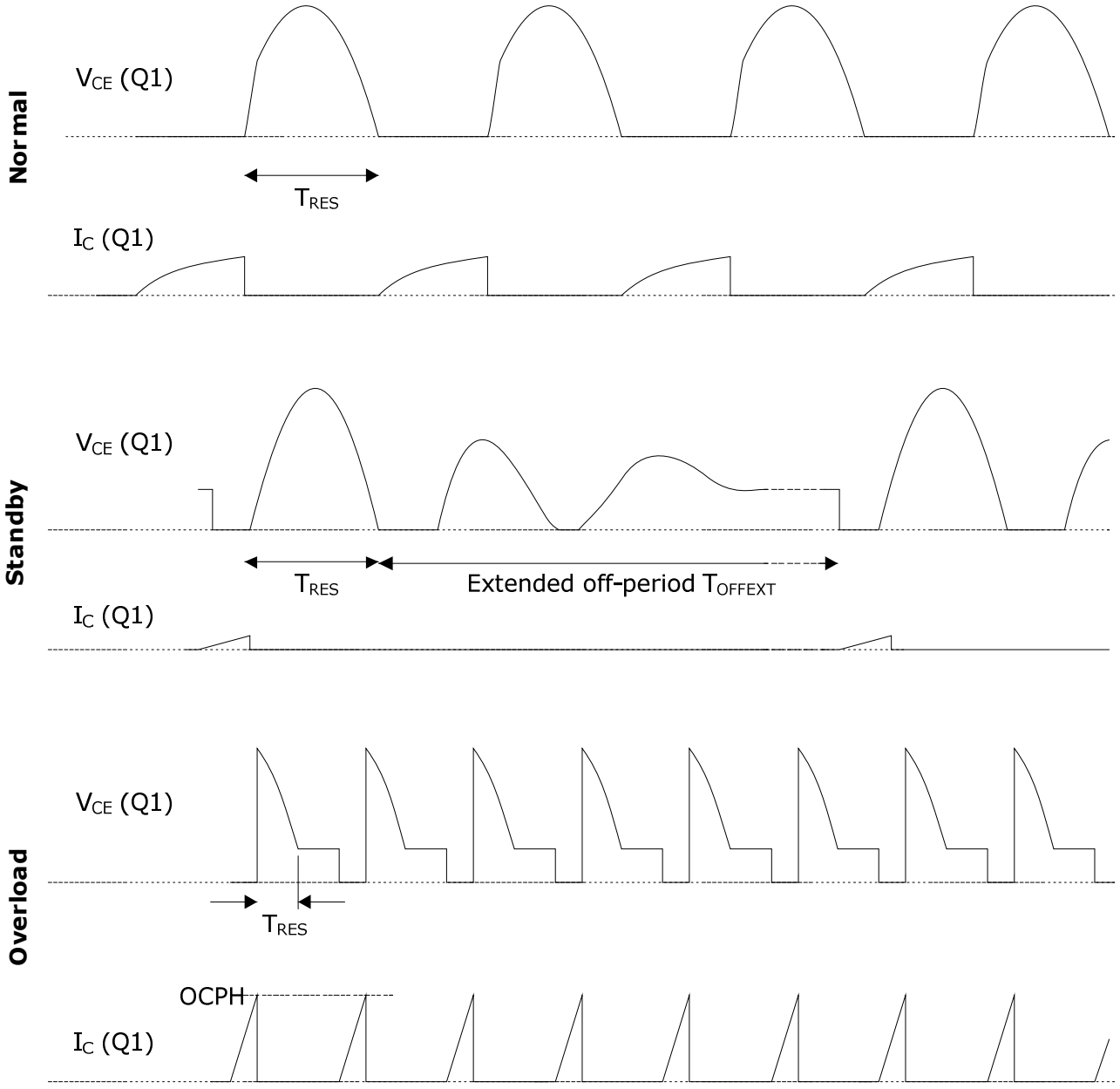


Figure 6: Typical Switch (Q1) Collector Voltage (V_{CE}) and Current (I_C) Waveforms

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Resonance Control

The natural resonance of the transformer and associated components is deduced from the current flowing into and out of the COL pin via the collector coupling capacitor.

The voltage sensed on the COL pin is used to control saturation of the primary switch transistor (Q1 in Figure 3) during the on-period (see "Optimised Base Drive"). During the off-period, timing of the resonance is detected via the current in and out of the pin, which has a low impedance path to GND during this time. Rate of change of voltage at the transformer primary causes current into or out of the COL pin, which is processed to measure the resonance period T_{RES} and to find the optimum turn-on time for the following conversion cycle. The resonant period is also used to determine the maximum on-time of the primary switch transistor, so that

$$T_{ON} = 0.75 \times T_{RES}$$

The maximum duty cycle (D_{NORMAL}) is therefore nominally 43%. On-time of the switch is controlled to manage power delivery and is reduced in both low-load and overload conditions. The minimum on-time in overload is determined by the internal CS blanking, specified as $T_{CSBLANK}$.

At turn-on of the primary switching transistor, its collector voltage can fall very rapidly, with correspondingly large current out of or in to the COL pin via the coupling capacitor (Ccol). An on-chip clamp transistor, controlled by an internal signal called ACTICLAMP, provides a low resistance path to GND. This transistor is turned on shortly before turn-on of the primary switch and remains on until time T_{ACT} after turn-on of the primary switch. It is then turned off during the remainder of the primary switch on-period. In some applications, the current through the coupling capacitor may develop sufficient voltage across the clamp transistor to cause conduction of the ESD protection diodes. This is permissible up to a limit I_{COL} which is specified in ABSOLUTE MAXIMUM RATINGS. If, due to application design, the capacitor current could exceed this level, external protection diodes and a resistor must be provided (Dcol1, Dcol2 and Rcol in Figure 3).

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Optimised Base Drive

To minimize losses in the primary switching transistor (Q1) its base current is carefully controlled. To minimize turn-on losses, the base current is initially forced to a maximum value I_{BASMAX} for a time T_{FON} (the force-on or "FON" pulse). For the remainder of the on-time the base current is reduced to a lower value such that the on-state collector voltage is maintained at a preset target voltage, thereby minimizing turn-off time and consequent losses. During this period, T_{PBD}, the so called "proportional base drive" (PBD) current is referred to as I_{BASPBD}.

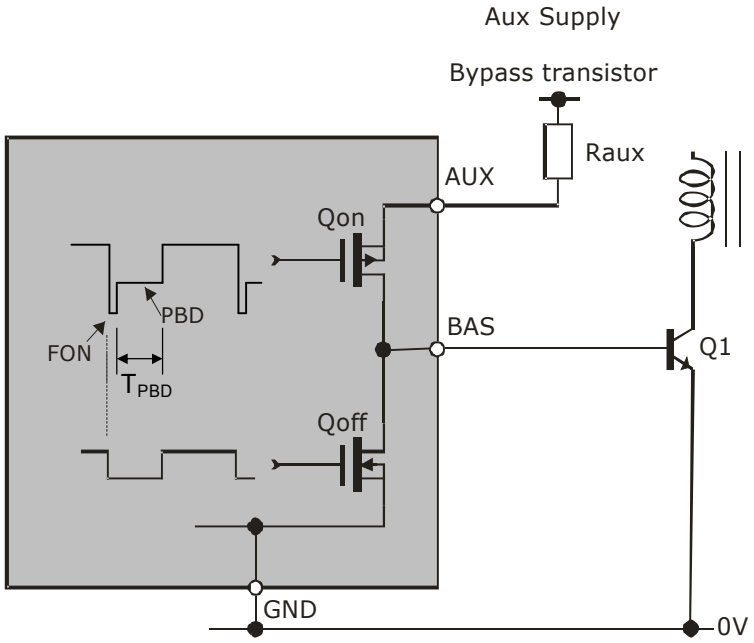


Figure 7: Primary Switch (Q1) Base Drive

The BAS pin (see Figure 7) is driven by two transistors, Qon and Qoff. Qon provides I_{BASMAX} during T_{FON} and I_{BASPBD} during the remainder of the on-period. Transistor Qoff provides a low-resistance ($R_{BASCLAMP}$) path to GND during the off-period to ensure rapid turn-off of the primary switch, Q1. I_{BASPBD} is set by the PBD system within the controller but I_{BASMAX} is determined by the external resistor Raux and the Aux Supply voltage.

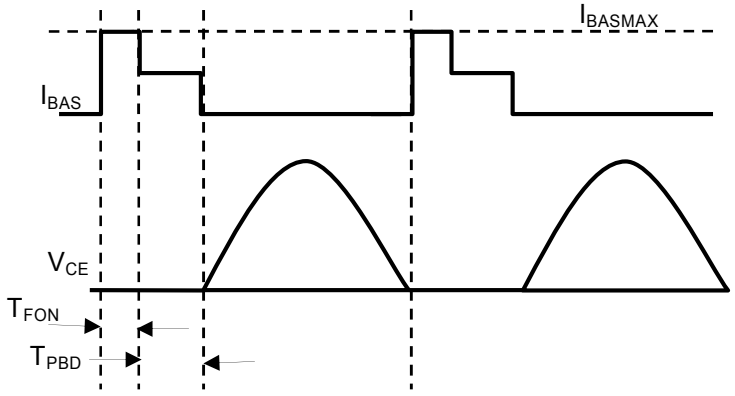


Figure 8: Base Driver Current Waveforms

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I_{BASPBD} is controlled by monitoring the voltage at the COL pin during T_{PBD}; base current is increased progressively as V_{COL} rises above threshold V_{CREF}(see Figure 9). The desired on-state V_{CE} of the switching transistor is set by capacitors Cp and Ccol (see Figure 3), the COL pin capacitance (C_{INCOL}) and V_{CREF}.

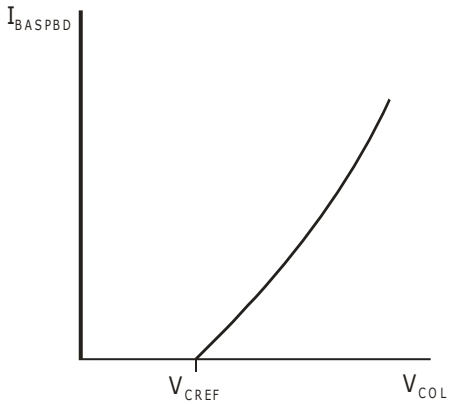


Figure 9: I_{BASPBD} characteristic

Power Control

Load conditions are sensed on a cycle-by-cycle basis via the CS pin. When low levels of output power demand are detected, the controller progressively reduces the switching duty cycle to reduce power consumption and to improve output voltage regulation. Power demand causes increase in duty up to the maximum, or until Overload is detected.

The voltage at the CS pin is compared to two thresholds, one nominally at GND voltage (V_{OCPL}) to generate an internal signal OCPL and the other at a negative threshold (V_{OCPH}) to generate an internal signal OCPH. The controller samples OCPL a short time (T_{OCPL}) after turn-on of the primary switch. A negative voltage at the CS pin indicates power demand so the controller increases the switching duty up to the maximum; conversely a positive voltage causes a decrease in duty.

Excessive primary switch current, detected via OCPH, terminates the on-period of the primary switch to limit power delivery (Overload mode). High levels of overload (when the converter output voltage held is low by the load) causes OCPH to trigger soon after turn-on of the primary switch. This condition is detected by the controller sampling OCPH at time T_{FBTHR} after turn-on. If OCPH triggers within this time, the controller changes to Foldback mode. To prevent mis-triggering, OCPH is blanked for a short period $T_{CSBLANK}$ after turn-on.

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The effective thresholds for current through the primary switch for both power reduction (OCPL) and overload (OCPH) are programmed by the current-sense resistors connected to the CS pin as shown in Figure 10.

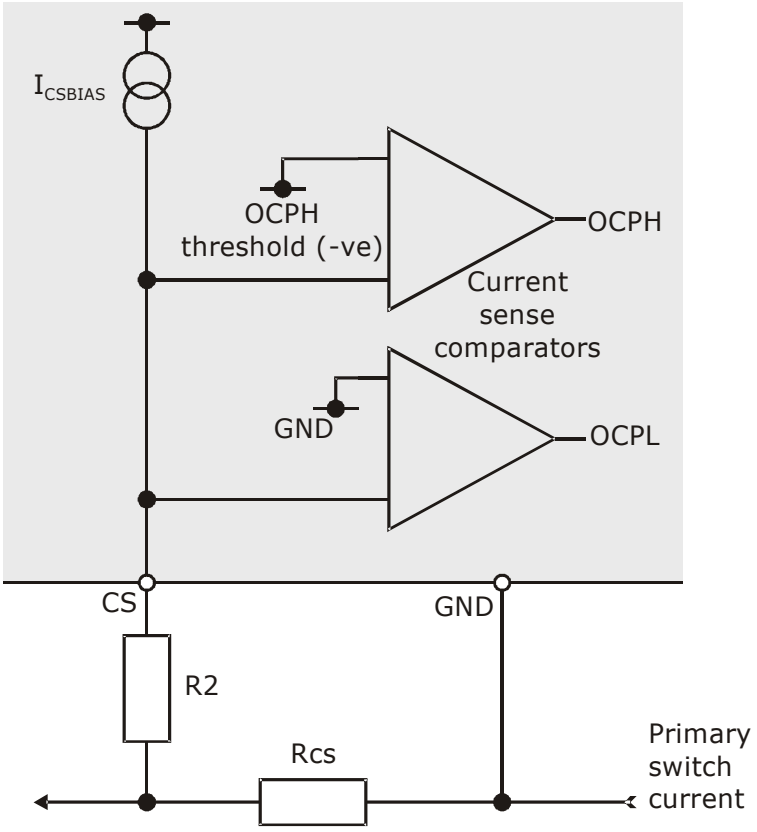


Figure 10: Current Sense Diagram

The internal current source (I_{CSBIAS}) develops an offset voltage across the series resistor (R2 in Figure 10) so setting OCPL current threshold. Switch current in excess of overload (OCPH) is detected using a fixed threshold voltage but the contribution from the offset voltage across R2 has to be taken into account.

I_{OCPL} threshold current = (V_{OCPL} + I_{CSBIAS}.R2)/Rcs

I_{OCPH} threshold current = (V_{OCPH} + I_{CSBIAS}.R2)/Rcs

$$R2 = \frac{V_{OCPH} \cdot I_{OCPL} - V_{OCPL} \cdot I_{OCPH}}{I_{OCPH} \cdot I_{CSBIAS} - I_{OCPL} \cdot I_{CSBIAS}}$$

$$Rcs = \frac{V_{OCPH} - V_{OCPL}}{I_{OCPH} - I_{OCPL}}$$

Note: I_{OCPL}, I_{OCPH}, V_{OCPH} IC_{SBIAS} are all positive magnitude in these formulae

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Protection Features

Collector De-saturation (Over Voltage) Protection (COVP)

To protect the primary switch from excessive power dissipation, the on-state voltage of the primary switching transistor is limited by the controller. The controller will go to Foldback mode if the COL pin voltage is greater than V_{COVP} at the end of the on-time for four consecutive cycles.

Over-temperature Protection (OTP)

Temperature sensing is integrated with the controller. If the temperature of the die rises above the shutdown temperature, T_{SH}, the BAS output is inhibited. It restarts once the temperature has fallen more than $T_{SH\ (HYST)}$ below T_{SH}. In typical applications “hiccup” operation will occur. While BAS is inhibited, the device is active and draws I_{DDWAKE}. This causes V_{DD} to fall since auxiliary power is not provided by the transformer. Once V_{DD} reaches $V_{UVDTHR,}$ the controller enters the Sleep state and I_{DD} falls to $I_{DDSLEEP}$ allowing V_{DD} to rise again (via the resistors Vht1 and Vht2). When V_{DD} reaches V_{OVDTHR} reset occurs and the controller re-starts. If the die temperature is below $T_{SH,}$ BAS operation continues but if it is still above T_{SH}, BAS operation ceases after a short period and the hiccup cycle repeats.

Primary Switch Over-current Protection (OCP)

To protect the primary switch, the base drive is turned off if the primary switch current rises too high, sensed via the CS input voltage falling below a preset negative threshold V_{OCPH}. See also Power Control on page 10.

Output Overload/Short-circuit Protection

If the application circuit is overloaded beyond a certain limit the controller goes into Foldback mode with reduced duty cycle, protecting the primary switch by reducing its power dissipation. Transition to Foldback mode is triggered by the CS pin voltage crossing the V_{OCPH} threshold within a time T_{FBTHR} of the start of the FON pulse. This typically happens when the load holds the output voltage low. See also Power Control on page 10.

Under Voltage Protection

The controller is prevented from operating if the V_{DD} supply is inadequate ($V_{DD} < V_{UVDTHR}$). Once the controller has stopped operation it will not restart until the V_{DD} supply voltage rises above V_{OVDTHR}.

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ABSOLUTE MAXIMUM RATINGS

CAUTION: Permanent damage may result if a device is subjected to operating conditions at or in excess of absolute maximum ratings.

Parameter	Symbol	Condition		Min	Max	Units
Supply voltage	V_{DD}				4.6	V
Input voltage AUX	V_{AUX}			-0.5	V_{DD} + 0.5	V
Input voltage BAS	V_{BAS}			-0.5	V_{DD} + 0.5	V
Input voltage CS	V_{CS}			-0.5	V_{DD} + 0.5	V
Input voltage COL	V_{COL}			-0.5	V_{DD} + 0.5	V
Pin current VDD	I_{DD}			-100	30	mA
Pin current AUX	I_{AUX}			-100	100	mA
Pin current BAS	I_{BAS}	All other conditions		-100	100[1]	mA
		While Qoff is on (Figure 7), base duty < 30%	T_j < 125 °C	-100	220	mA
			T_j < 100 °C	-100	400	mA
Pin current CS	I_{CS}			-100	100	mA
Pin current COL	I_{COL}	During PBD: ESD diode limit, input is high impedance		-100	100	mA
		During turn-on transient (ACTICLAMP active)		-250	250	mA
		During resonance off period		-125	250	mA
Junction temperature	T_J			-25	125	°C
Storage temperature	T_{STOR}			-40	150	°C
Lead temperature (soldering, 10 s)	T_L				260	°C
ESD withstand		Human body model, JESD22-A114			2	kV
		Charged device model, ANSI-ESD-STM5.3.1			500	V

[1] I_{BAS} can be higher if controller is active and not in PBD or FON, up to $V_{BAS} = V_{DD}$

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NORMAL OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply voltage	V_{DD}	VDD pin, limited by internal regulator	3.1	3.3	3.5	V
Junction temperature	T_J	Over temperature protection operates at higher temperatures	-25	25	100	ºC
Internal digital clock frequency	F_{CLK}	T_j = 25 °C, V_{DD}=$V_{DDREG(R)}$	9.7	12.1	14.5	MHz
	F_{CLKTC}	Temperature coefficient	-35		5	kHz°C^{-1}
Switching frequency, Normal mode	F_{MAX}	Determined by T_{RES} (F_{CLK} in MHz)		F_{CLK} / 61		MHz
	F_{MIN}			F_{CLK} / 490		MHz
Transformer resonance time	T_{RESMIN}	Natural resonance of transformer and associated capacitances. F_{CLK} in MHz.		35 / F_{CLK}		µs
	T_{RESMAX}			280 / F_{CLK}		µs
Supply current	I_{DD}	Limit externally			30	mA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated:

1. Min and Max electrical characteristics apply over normal operating conditions.
2. Typical electrical characteristics apply at T_J = T_{JTYP} and V_{DD} = V_{DDTYP}
3. Functionality and performance is not defined when a device is subjected to conditions outside the range of normal operating conditions and device reliability may be compromised.
4. For parameters dependent on $F_{CLK,}$ the value of $F_{CLK,}$in MHz should be used in calculations.

VDD Pin

Parameter	Symbol	Condition	Min	Typ	Max	Units
Regulation voltage	$V_{DDREG(R)}$	Active state, 2.5 mA < I_{DD} < 30 mA	3.1	3.3	3.5	V
	$V_{DDREG(S)}$	Start-up state, 2.5 mA < I_{DD} < 30 mA		4		V
Quiescent current	$I_{DDSLEEP}$	Sleep state, V_{DD} < V_{UVDTHR}			8	µA
Residual supply current	I_{DDWAKE}	Start-up & Active states, Normal mode ($V_{DDREG(R)}$ – 300 mV) < V_{DD} and V_{DD} < ($V_{DDREG(R)}$ - 100 mV)	0.5		2.5	mA
OVD threshold, Sleep	V_{OVDTHR}	Sleep state	3.5		4.6	V
UVD threshold	V_{UVDTHR}	Start-up and Active states	2.7		3.2	V
$V_{DDREG(R)}$ - V_{UVDTHR}		I_{DD} < 30 mA	150			mV

AUX Pin

Parameter	Symbol	Condition		Min	Typ	Max	Units
Input current	I_{AUXMAX}					100	mA
AUX pin voltage	V_{AUXFON}	BAS = 800 mV 0 °C < T_J < 100 °C	I_{AUX} = 10 mA	0.84		1.22	V
			I_{AUX} = 80mA	1.2		1.64	V

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CS Pin

Parameter	Symbol	Condition	Min	Typ	Max	Units
OCPH comparator threshold	V_{OCPH}	0 °C < T_J < 100 °C	-260		-235	mV
OCPL comparator threshold	V_{OCPL}		-5		5	mV
OCPH comparator response time	T_{OCP}	Step CS input from V_{CS} > -200 mV to V_{CS} < -300 mV			0.1	µs
Bias current	I_{CSBIAS}	0 °C < T_J < 100 °C	40		67.5	µA
		T_j = 25°C	41.5		59.5	µA
OCPL sampling time	T_{OCPL}	F_{CLK} in MHz		19 / F_{CLK} - 0.06		µs
Blanking period	$T_{CSBLANK}$	F_{CLK} in MHz		4 / F_{CLK} - 0.06		µs
Foldback threshold time	T_{FBTHR}	F_{CLK} in MHz		26 / F_{CLK} - 0.06		µs

BAS Pin

Parameter	Symbol	Condition	Min	Typ	Max	Units
Base drive current	I_{BASMAX}	Limit by external resistor			100	mA
Base clamp turn-off resistance	$R_{BASCLAMP}$	V_{BAS} = 400 mV			8.5	Ω
Duty cycle	D_{NORMAL}	Normal mode		43		%
Force-on period (depends on F_{CLK})	T_{FON}	Standby mode 0 °C < T_J < 100 °C	100		230	ns
		Normal, Foldback & Power Burst modes. 0 °C < T_J < 100 °C	400		705	ns
Minimum on-period	T_{ONMIN}	Standby (F_{CLK} in MHz)		20 / F_{CLK}		µs
Maximum off-period	T_{OFFMAX}	Standby (F_{CLK} in MHz)		1920 / F_{CLK} + T_{RES}		µs
Power Burst mode	N_{BURST}	Burst length, number of converter cycles		22144		cycles
	$T_{BURSTCYCMIN}$	Minimum converter cycle period in Power Burst mode[2] (F_{CLK} in MHz)		39 / F_{CLK}		µs
Foldback mode	N_{FOLD}	Foldback duration between bursts, number of converter cycles		18326		cycles
	$T_{FOLDCYCMIN}$	Converter period in Foldback mode[3] (F_{CLK} in MHz)		900 / F_{CLK} + T_{RES}		µs
	$T_{OFFEXTMIN}$	Extended off time (F_{CLK} in MHz)		896 / F_{CLK}		µs

[2] Minimum converter period = T_{RES} + T_{ONMIN}
[3] Minimum converter period = T_{RES} + T_{OFFEXT} + T_{ONMIN}

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COL Pin

Parameter	Symbol	Condition	Min	Typ	Max	Units
Rising edge comparator threshold	I_{CRISE}			0.4		mA
Falling edge comparator threshold	I_{CFALL}			-0.4		mA
Collector over-voltage comparator threshold	V_{COVP}		$0.7V_{DD}$		$0.9V_{DD}$	V
PBD threshold voltage	V_{CREF}	Intercept of characteristic 10 mA < I_{BAS} < 80mA (see Figure 11)	0.76		1.1	V
PBD transconductance				200		mAV^{-1}
Input leakage current		T_J < 100 ° C	-650		650	nA
Input capacitance	C_{INCOL}	V_{COL} = 1 V	25	28	31	pF
ACTICLAMP duration after FON	T_{ACT}	Standby mode (F_{CLK} in MHz)		3 / F_{CLK} – 0.06		µs
		Normal, Foldback and Power Burst modes (F_{CLK} in MHz)		4 / F_{CLK} – 0.06		µs

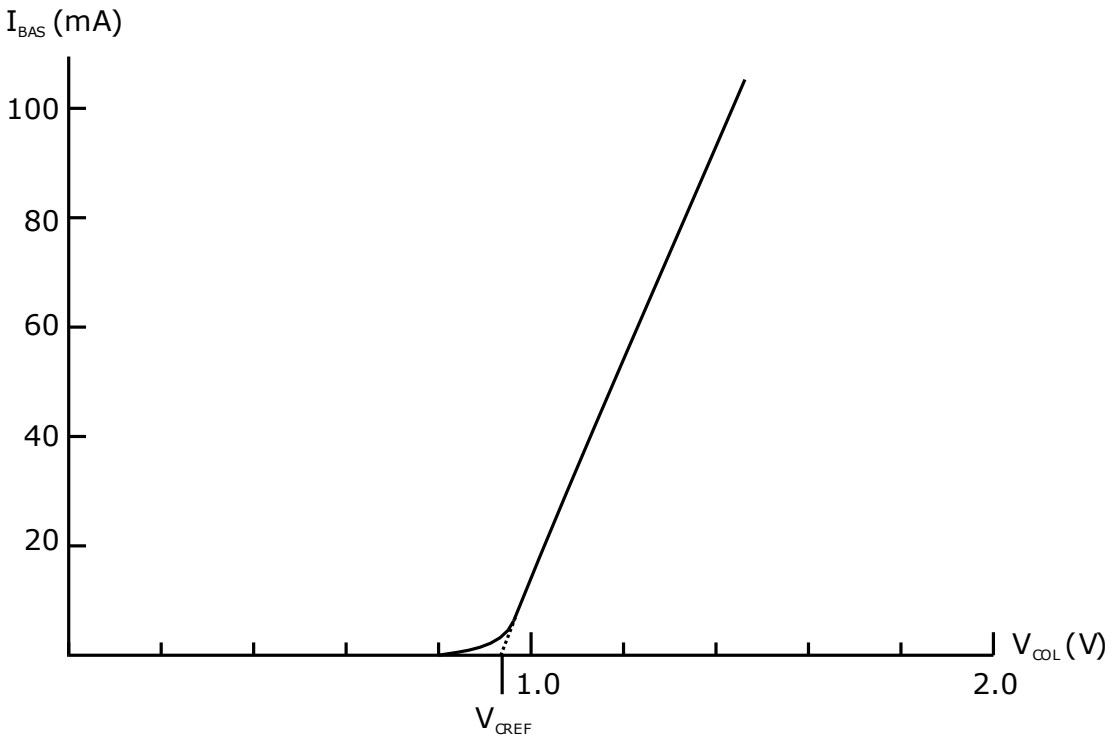


Figure 11: COL/BAS Transconductance (typical, at 25 °C)

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THERMAL CIRCUIT PROTECTION

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown temperature	T_{SH}	At junction	105	115	125	°C
Thermal shutdown hysteresis	$T_{SH\ (HYST)}$	At junction		35		°C

PACKAGE THERMAL RESISTANCE CHARACTERISTICS

Conditions:

1. Controller IC mounted on typical PCB (1.6 mm thick, 35 µm copper, CEM1);
2. θ_{JP} measured to pin terminal of device at the surface of the PCB.

Package	Junction-to-pin θ_{JP} (Typical)	Junction-to-ambient θ_{JA} (Typical)	Units
SOT23-6	60	170	°C / W
SOP-8	70	140	°C / W
PDIP-8	35	105	°C / W

PACKAGE AND ORDERING INFORMATION

Package Marking

The PDIP-8 (C2474PW1) and SOP-8 (C2473PX1) packages are marked with the full product type number. The SOT23-6 package (C2472PX2) is marked with a short code **FA** as illustrated in Figure 12.

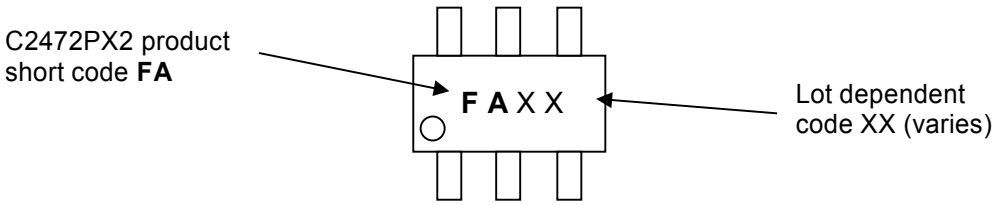


Figure 12: C2472PX2 SOT23-6 Package Marking

Ordering

Type	Package	Packing Form	Order
C2472PX2	SOT23-6	7” Tape & Reel	C2472PX2-TR7
		13” Tape & Reel	C2472PX2-TR13
C2473PX1	SOP-8	7” Tape & Reel	C2473PX1-TR7
		13” Tape & Reel	C2473PX1-TR13
C2474PW1	PDIP-8	Tube	C2474PW1-T1

For further package and ordering information please contact CamSemi.

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Datasheet Status	Product Status	Definition
Product preview	In development	The Datasheet contains target specifications relating to design and development of the described IC product. Application circuits are illustrative only. Specifications are subject to change without notice.
Preliminary	In qualification	The Datasheet contains preliminary specifications relating to functionality and performance of the described IC product. Application circuits are illustrative only. Specifications are subject to change without notice.
Product data	In production	The Datasheet contains specifications relating to functionality and performance of the described IC product. Application circuits are illustrative only. Specifications are subject to change without notice.

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