C185EKV01 User's Guide

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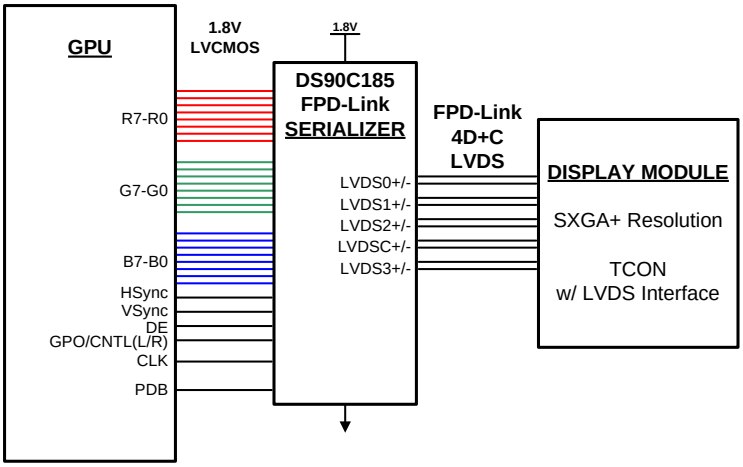
1. Introduction

The Texas Instruments C185EVK01 evaluation module (EVK) helps designers evaluate the operation and performance of the DS90C185 Low Power 1.8V FPD-Link (LVDS) Serializer. The device operates off of a single 1.8V supply and supports input pixel clocks from 25 MHz to 105 MHz.



The EVM contains one Low Power 1.8V FPD-Link (LVDS) Serializer (See Table 1).

Table 1: Device and Package Configurations

SERIALIZER	IC	PACKAGE
U1	DS90C185SQ	SQF48A

2. Setup

This section describes the jumpers and connectors on the EVK as well and how to properly connect, set up and use the C185EVK01.

2.1. Input/Output Connector Description

JP1 – PDB is the jumper used to enable the Serializer. Power Down Bar (PDB) set to logic HIGH enables the device, while connecting this jumper to logic LOW will disable the device.

JP2 – VODSEL is the jumper that controls the differential output voltage. When VODSEL is set to logic HIGH, the output launch amplitude of the LVDS drivers will be set to have a larger output swing. If this jumper is set to logic LOW, then the LVDS drivers will be configured to have a power saving smaller output swing.

JP3 – RFB is the jumper that selects the clock edge that the input LVCMOS data will be sampled on. If RFB is logic HIGH, the input data is latched on the RISING EDGE of the pixel clock. If RFB is set to logic LOW, the input data is latched on the FALLING EDGE of the pixel clock.

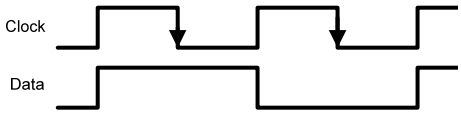


Figure 1: Falling Edge Data Strobe

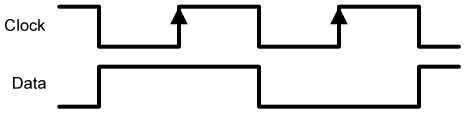


Figure 2: Rising Edge Data Strobe

JP4 – 18B_MODE is the jumper used to enable a power saving mode for 18-bit color applications. When this jumper is set to logic LOW, all data inputs will be sampled, serialized and driven out through the LVDS drivers to support 24-bit color applications or 28-bit generic data buses. If this jumper is set to logic HIGH, the device will enter a power saving mode that will power down the circuitry that feeds the 4th LVDS driver. In this mode the 4th LVDS driver, TxOUT3+/- will be TRI-STATE®.

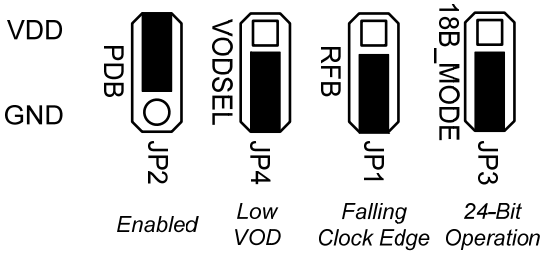


Figure 3: Default Jumper Settings

J1 – LVDS OUTPUTS are brought out to a 2 x10 bank of header pins. Note that each LVDS output is separated from adjacent LVDS signals by one ground pin. By default, 100 ohm termination resistors are soldered onto the EVM to allow for easy measuring and probing of the LVDS signals. **If a cable is connected to J1, these termination resistors (R57, R58, R62, R63, R64) must be removed or the differential voltage swing will be reduced.**

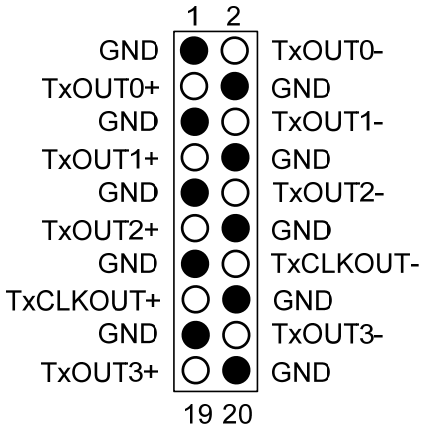


Figure 4: LVDS Output Connections (J1)

J2 – LVCMOS INPUTS are connected to the 2 x 30 bank of header pins. Note that each LVCMOS signal is paired with a ground signal. When attaching external test equipment or other hardware to this board it is important that there be sufficient ground connections to ensure good signal integrity for the input clock and data waveforms. There is a provision to populate 50 ohm terminations if needed.

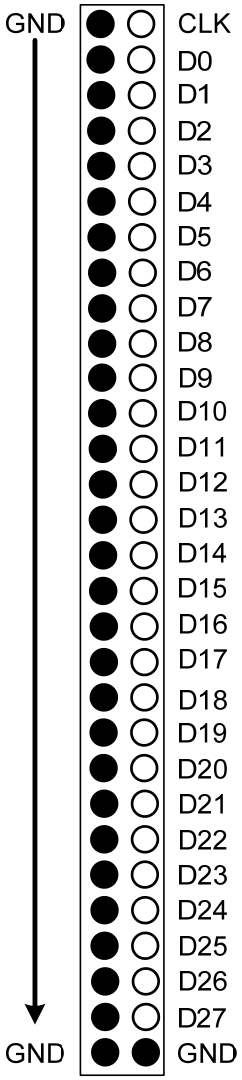


Figure 5: LVCMOS Input Connections (J2)

J3 – VDD is the terminal where 1.8V power should be applied.

J4 – GND is the terminal where ground should be applied.

2.2. System Setup

The input power jack (J3) should receive a voltage within the range of 1.71 V to 1.89 V. Once, power has been applied to the board, the PDB pin can be set to logic HIGH. After setting the PDB pin to HIGH, 1.8V clock and data can be transmitted to the EVM. **If a cable is connected to J1, the termination resistors (R57, R58, R62, R63, R64) should be removed.**

2.3. Operation

For proper operation of the DS90C185, JP1, JP2, JP3 and JP4 should be properly configured by using shorting blocks (jumpers); see Figure 3.

JP1 to HIGH, after power on
JP2 to LOW for reduced VOD swing or HIGH for large VOD swing
JP3 to LOW for falling clock edge strobe or HIGH for rising clock edge strobe
JP4 to LOW for 24-bit color (28-bit data bus) or to HIGH for 18-bit color (21-bit data bus)

After applying power and setting JP1 to HIGH, a clock signal can be sent to the DS90C185. When the clock signal is detected, the DS90C185 will power on and begin to transmit serialized LVDS data.
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3. Board Layout

Figure 4, Figure 5 and Figure 6 show the board layout for the C185EV01 printed circuit board. The EVM offers jumpers to configure and power on/off the DS90C185. Resistor pads are provided so that 50 ohm shunt terminations can be implemented when interfacing with external video (data) generators with 50 ohm signal sources. 100 ohm differential termination resistors are populated by default to allow for probing of the LVDS outputs at J1.

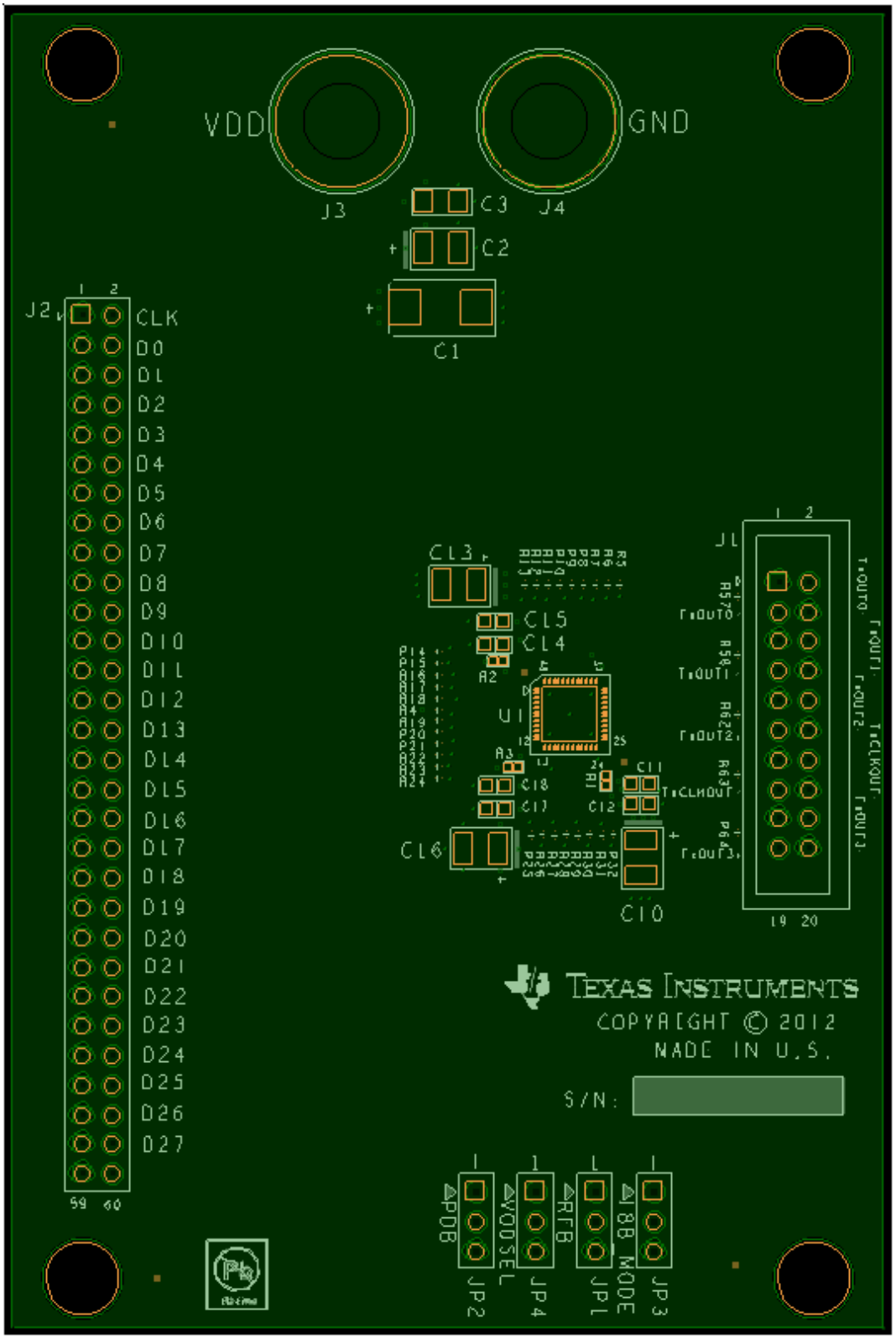

Figure 6: Top Assembly Layer

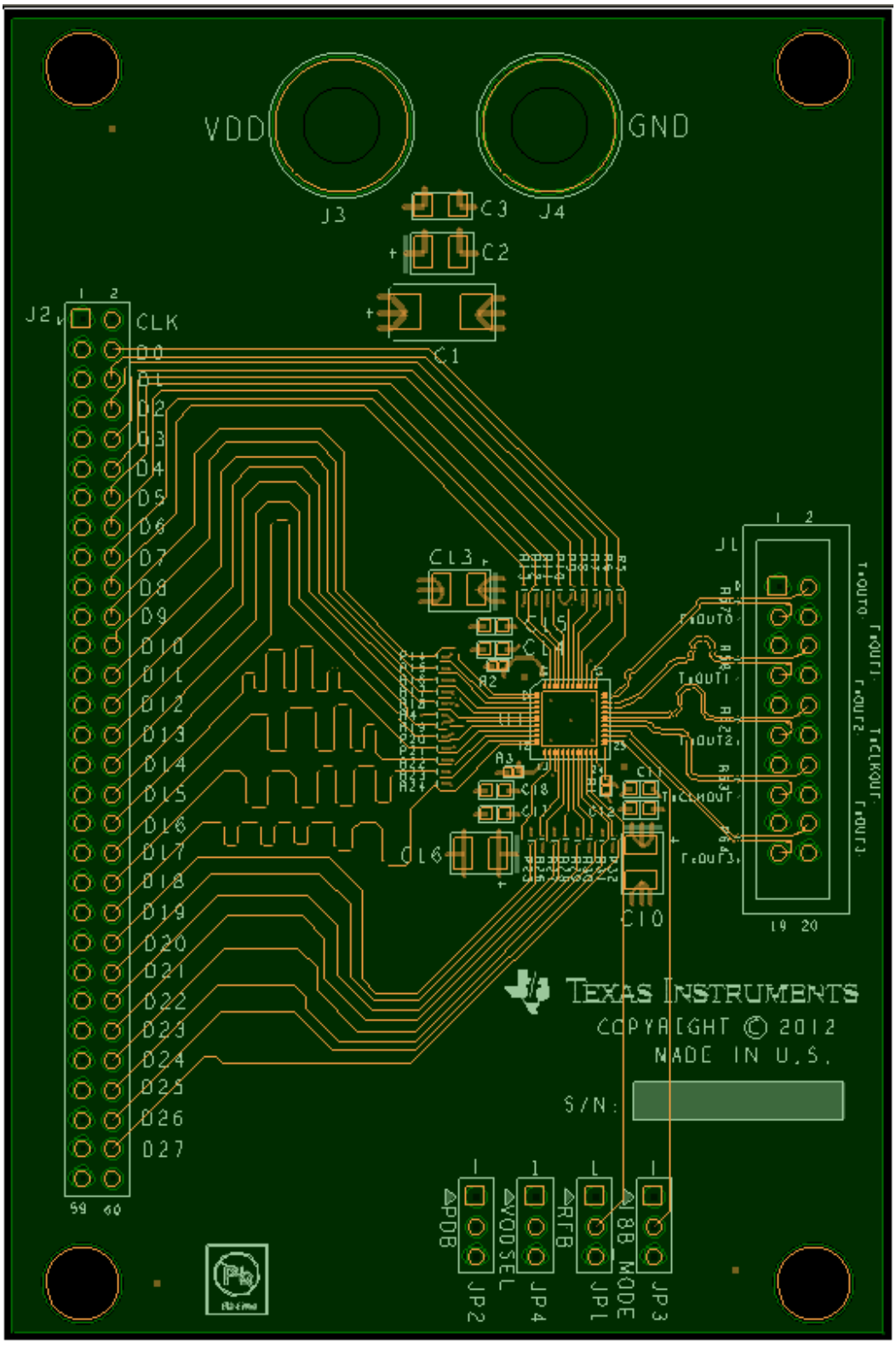

Figure 7: Top Layer Routing

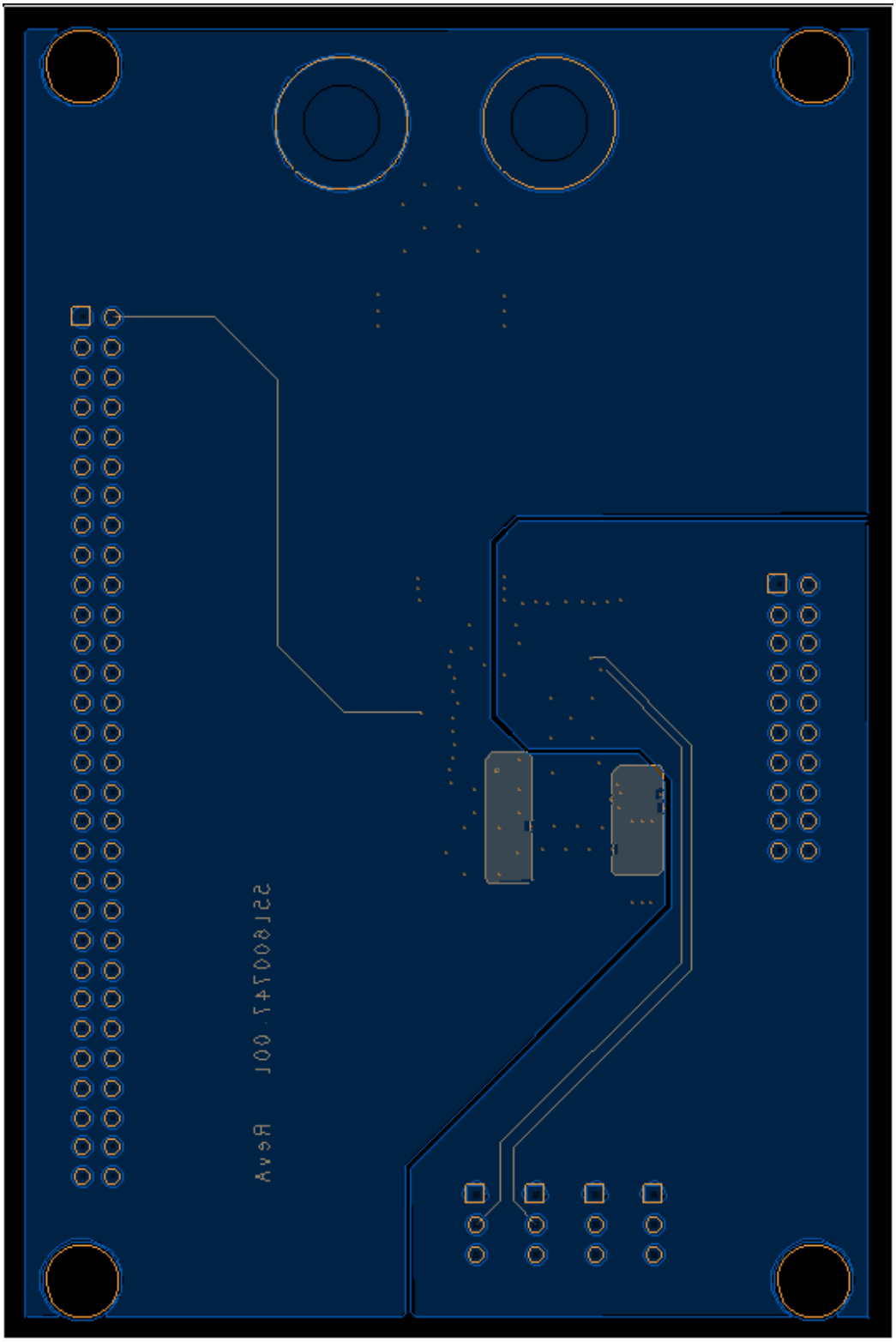

Figure 8: Bottom Layer Routing

4. Schematic

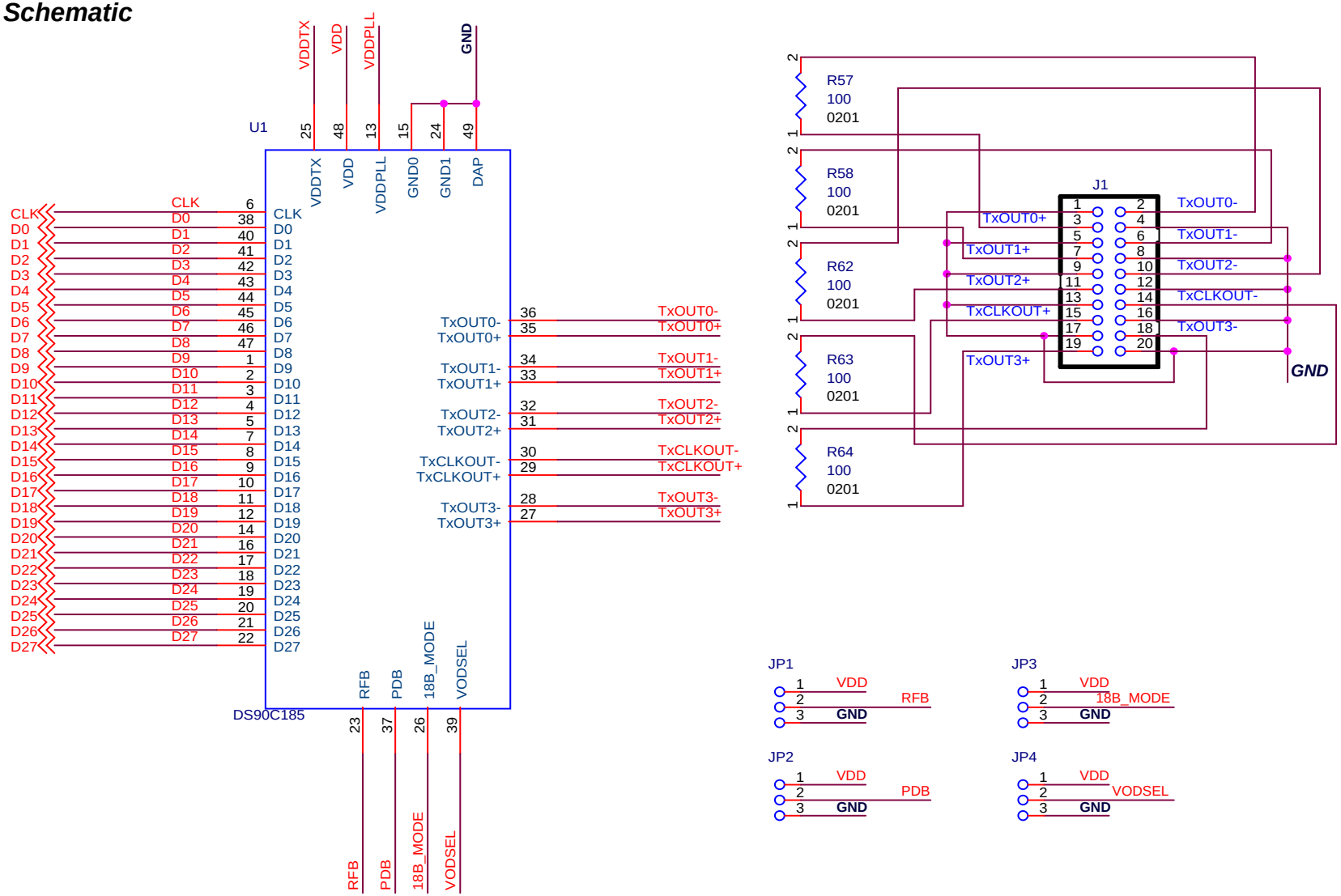

Figure 9: C185EVK01 Schematic Page 1

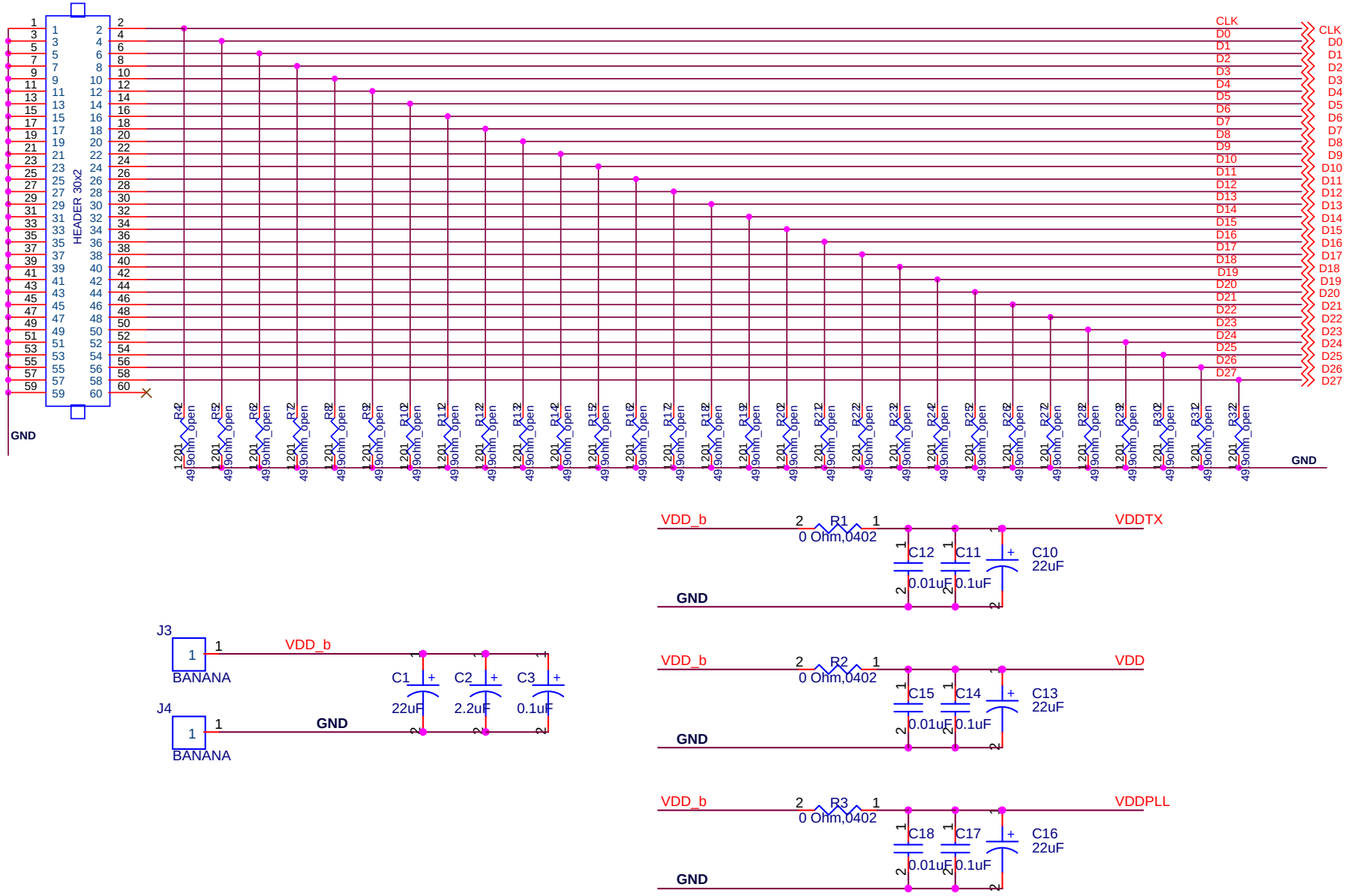

Figure 10: C185EVK01 Schematic Page 1

Table 2: C185EVK01 Bill of Materials

Quantity	Reference Designator	Part	Vendor	Part number
1	C1	22uF	Nichicon	F931E226MNC
1	C2	2.2uF	KEMET	T491B225K020AT
1	C3	0.1uF	KEMET	C1206C104K5RACTU
3	C10,C13,C16	22uF	Kemet	T494B226M016AT
3	C11,C14,C17	0.1uF	Panasonic	ECJ-1VB1E104K
3	C12,C15,C18	0.01uF	KEMET	C0603C103K1RACTU
4	JP1,JP2,JP3,JP4	3-Pin Header	AMP/Tyco	87224-3
1	J1	2X10 Pin Header	3M	N2520-6002RB
1	J2	30x2 Pin Header	AMP/Tyco	3-87215-0
2	J3,J4	BANANA	Johnson	108-0740-001
3	R1,R2,R3	0 Ohm, 0402	Panasonic	ERJ-2GEJ0R00X
29	R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,R15,R16,R17,R18,R19,R20,R21,R22,R23,R24,R25,R26,R27,R28,R29,R30,R31,R32	49.9ohm_open	Panasonic	ERJ-1GEF49R9C_open
5	R57,R58,R62,R63,R64	100 ohm	Susumu	RR0306P-101-D
1	U1	DS90C185	TI	DS90C185SQ

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It is important to operate this EVM within the input voltage range of -0.3 V to 48 V and the output voltage range of 0.9 V to 18 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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