Data Sheet | October 1998 | File Number 2263.1

5.8A, 200V, 0.600 Ohm, N-Channel Power MOSFET

This is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Formerly developmental type TA4600.

Ordering Information

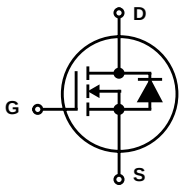
PART NUMBER	PACKAGE	BRAND
BUZ73A	TO-220AB	BUZ73A

NOTE: When ordering, use the entire part number.

Features

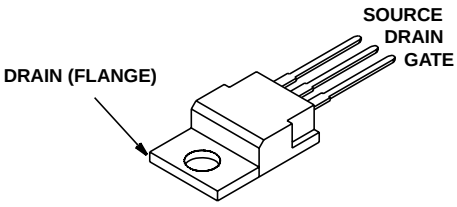
- 5.8A, 200V
- $r_{DS(ON)} = 0.600\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		BUZ76A	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	200	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	200	V
Continuous Drain Current ($T_C = 30^oC$)	I_D	5.8	A
Pulsed Drain Current (Note 3)	I_{DM}	23	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	40	W
Linear Derating Factor		0.32	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	200	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA (Figure 9)	2.1	3	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$T_J = 25^oC$, V_{DS} = 200V, V_{GS} = 0V	-	20	250	μA
		$T_J = 125^oC$, V_{DS} = 200V, V_{GS} = 0V	-	100	1000	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 20V, V_{DS} = 0V	-	10	100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 3.5A, V_{GS} = 10V (Figure 8)	-	0.5	0.600	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 25V, I_D = 3.5A (Figure 11)	2.2	3.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{CC} = 30V, $I_D \approx$ 2.8A, V_{GS} = 10V, R_{GS} = 50Ω, R_L = 10Ω. (Figures 14, 15)	-	15	20	ns
Rise Time	t_r		-	40	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	90	ns
Fall Time	t_f		-	40	55	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 10)	-	450	600	pF
Output Capacitance	C_{OSS}		-	100	160	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	80	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		≤ 3.1			$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		≤ 75			$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	$T_C = 25^oC$	-	-	5.8	A
Pulsed Source to Drain Current	I_{SDM}		-	-	23	A
Drain to Source Diode Voltage	V_{SD}	$T_J = 25^oC$, I_{SD} = 11.6A, V_{GS} = 0V	-	1.4	1.7	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 5.8A, dI_{SD}/dt = 100A/μs, V_R = 100V	-	200	-	ns
Reverse Recovery Charge	Q_{RR}		-	0.6	-	μC

NOTES:

2. Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

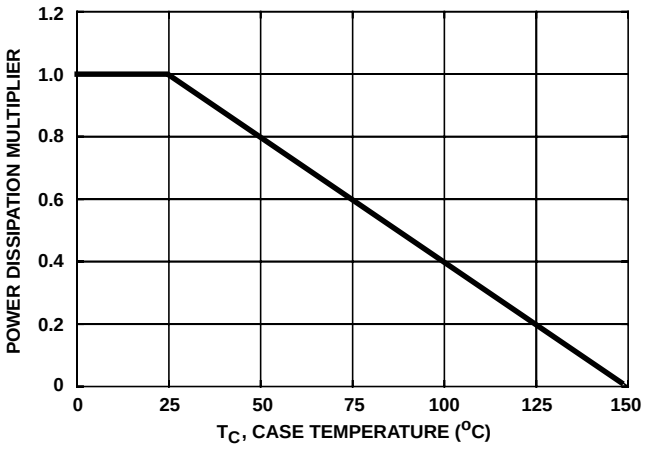


FIGURE 18. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

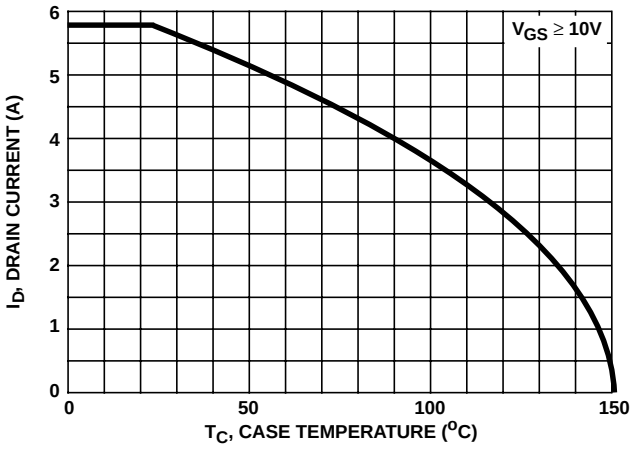


FIGURE 19. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

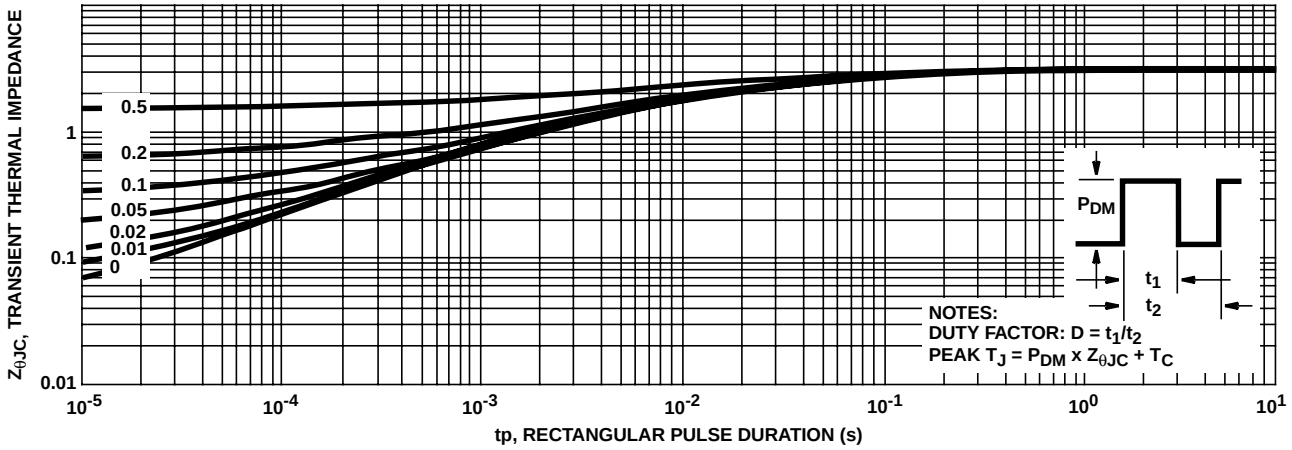


FIGURE 20. MAXIMUM TRANSIENT THERMAL IMPEDANCE

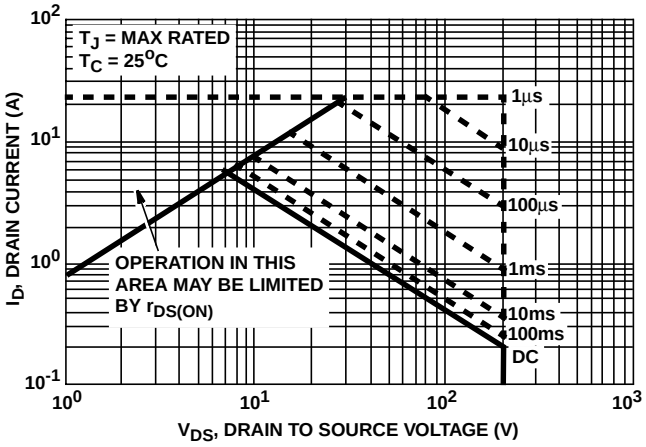


FIGURE 21. FORWARD BIAS SAFE OPERATING AREA

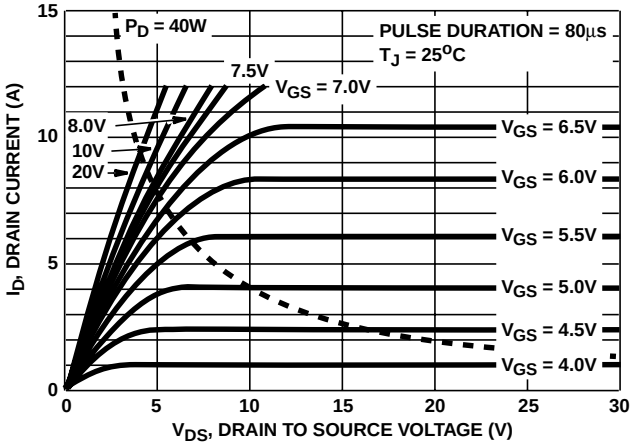


FIGURE 22. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

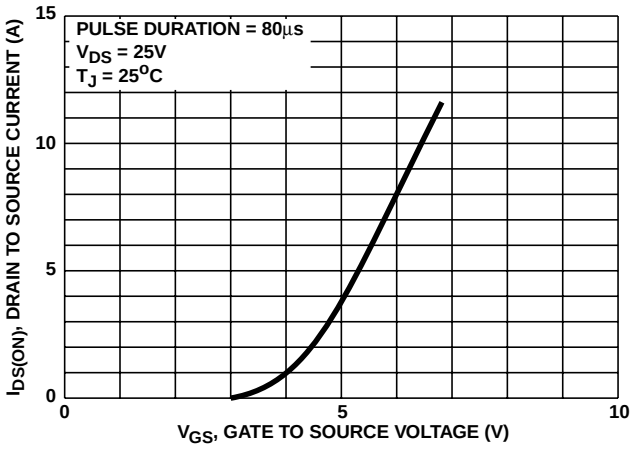


FIGURE 23. TRANSFER CHARACTERISTICS

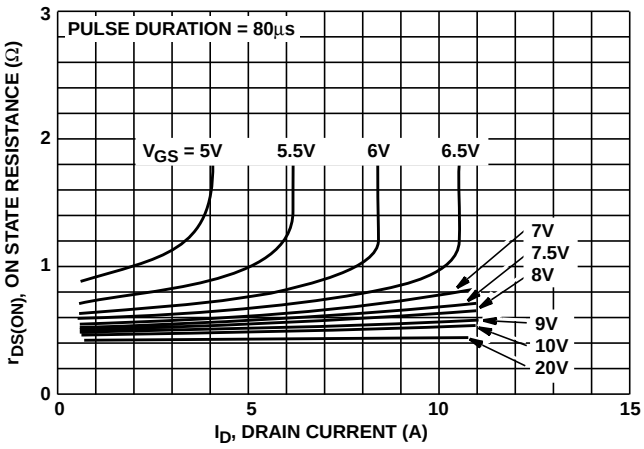


FIGURE 24. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

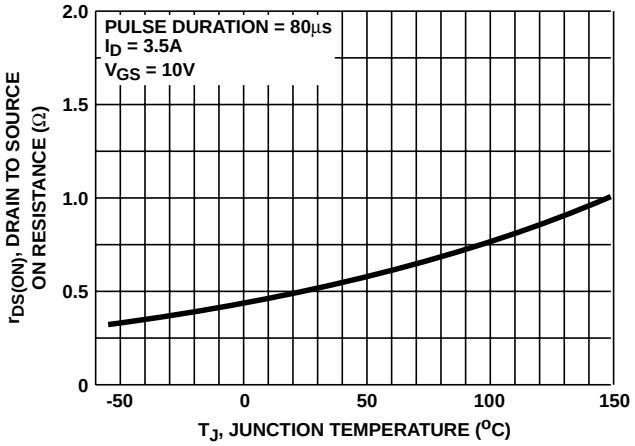


FIGURE 25. DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

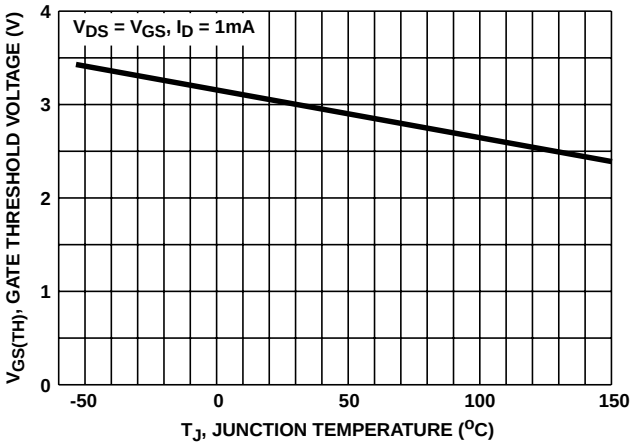


FIGURE 26. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

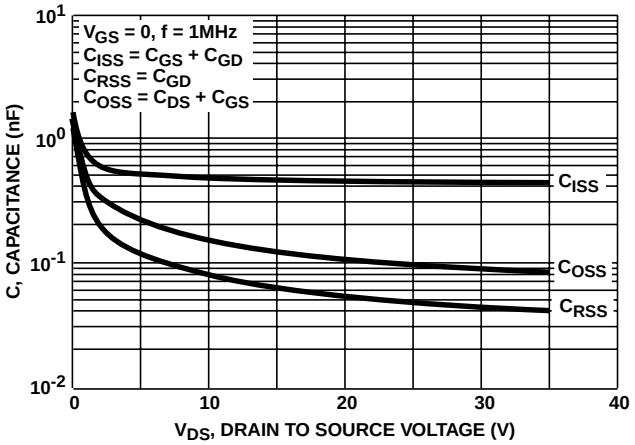


FIGURE 27. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

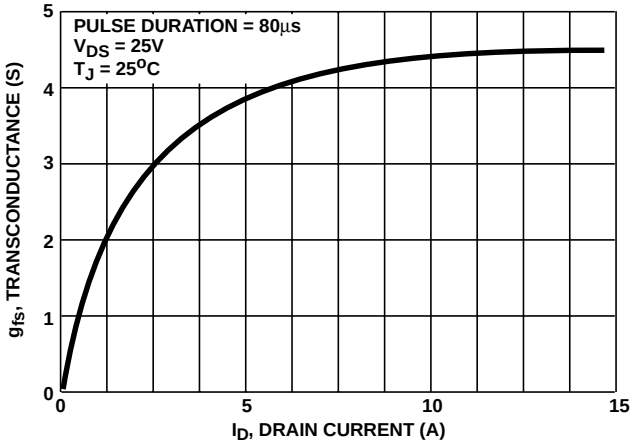


FIGURE 28. TRANSCONDUCTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

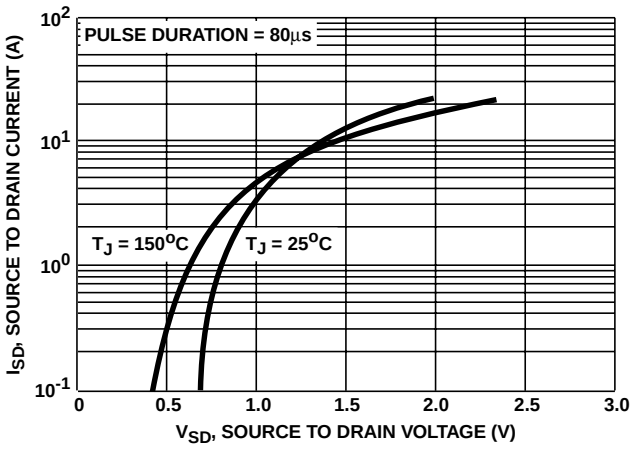


FIGURE 29. SOURCE TO DRAIN DIODE VOLTAGE

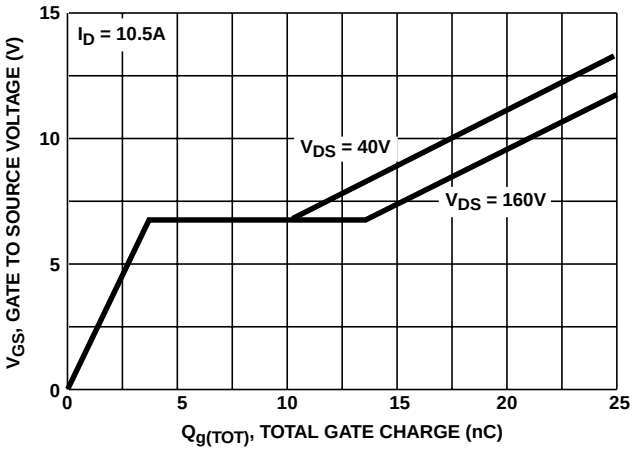


FIGURE 30. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

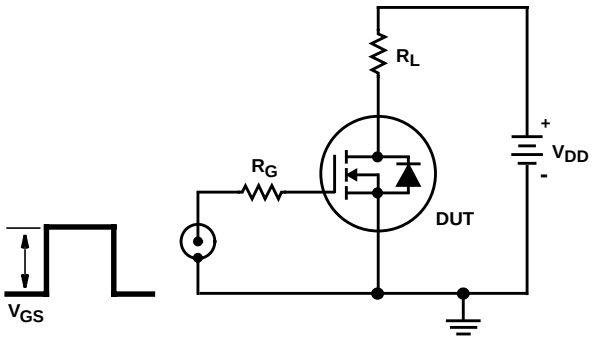


FIGURE 31. SWITCHING TIME TEST CIRCUIT

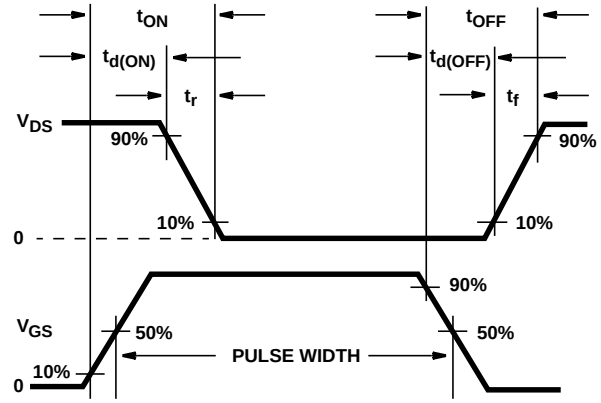


FIGURE 32. RESISTIVE SWITCHING WAVEFORMS

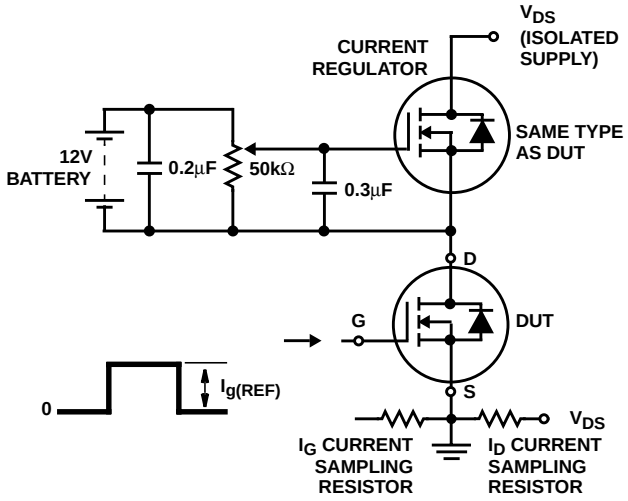


FIGURE 33. GATE CHARGE TEST CIRCUIT

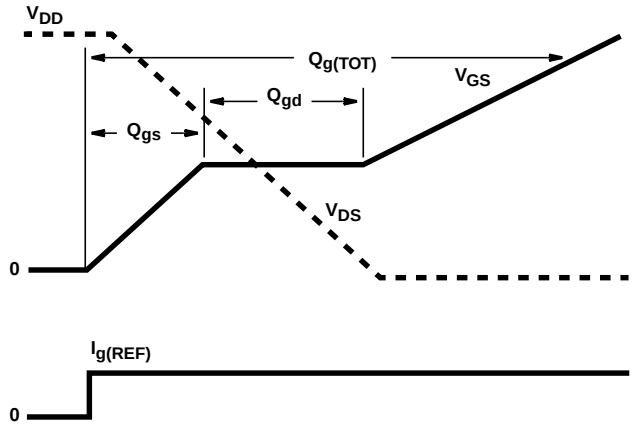


FIGURE 34. GATE CHARGE WAVEFORMS