BUT34

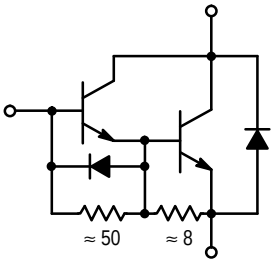
Designer's™ Data Sheet

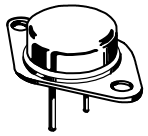
SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

50 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTOR
850 VOLTS
250 WATTS

The BUT34 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated SWITCHMODE applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  - 0.7 μs Inductive Fall Time at 25°C (Typ)
  - 1.8 μs Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range –65 to 200°C





CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	BUT34	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter–Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	50 75	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Free Wheel Diode Forward Current — Continuous — Peak	I_F I_{FM}	50 75	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 140	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.2 4.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	—	—	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 16 A, V_{CE} = 5 V) (I_C = 32 A, V_{CE} = 5 V)	h_{FE}	 30 15	 — —	 — —	
Collector–Emitter Saturation Voltage (I_C = 16 A, I_B = 0.8 A) (I_C = 32 A, I_B = 3.2 A) (I_C = 40 A, I_B = 4 A) (I_C = 50 A, I_B = 10 A)	$V_{CE(sat)}$	 — — — —	 — — — —	 2.0 3.0 3.5 5.0	Vdc
Base–Emitter Saturation Voltage (I_C = 16 A, I_B = 0.8 A) (I_C = 32 A, I_B = 3.2 A) (I_C = 40 A, I_B = 4 A)	$V_{BE(sat)}$	 — — —	 — — —	 2.5 2.9 3.3	Vdc
Diode Forward Voltage (I_F = 40 A)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	T_C = 25°C	See Table 1	t_s	—	1.8	3.0	μs
Fall Time		I_C = 32 A	t_f	—	0.7	1.5	μs
Storage Time	T_C = 100°C	I_{B1} = 3.2 A	t_s	—	2.2	—	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	—	0.8	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

TYPICAL CHARACTERISTICS

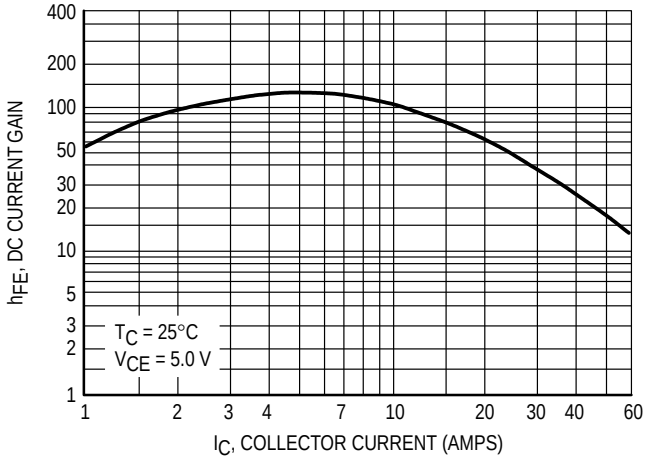


Figure 1. DC Current Gain

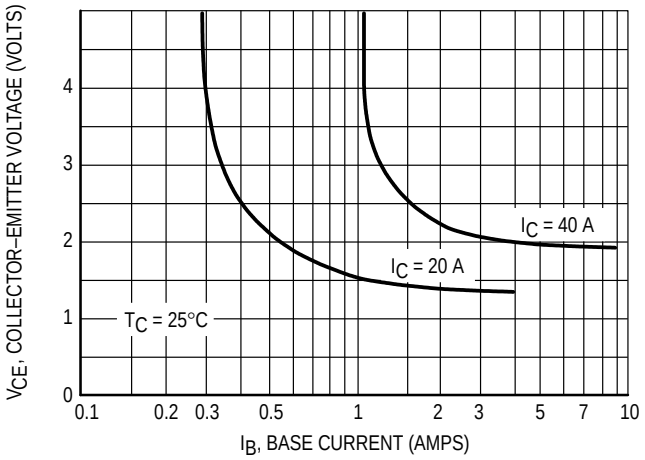


Figure 2. Collector Saturation Region

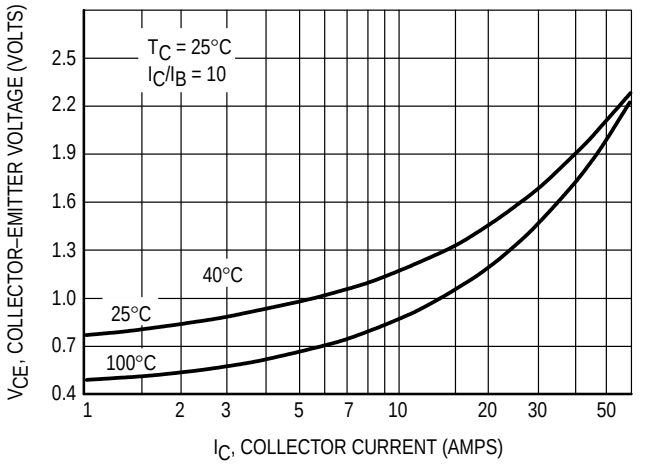


Figure 3. Collector–Emitter Saturation Voltage

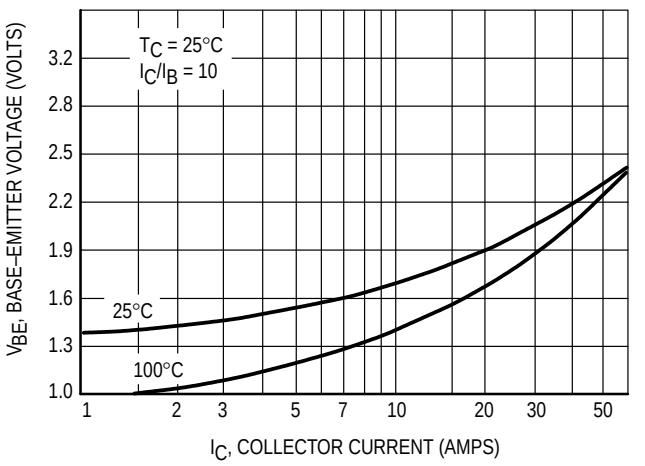


Figure 4. Base–Emitter Voltage

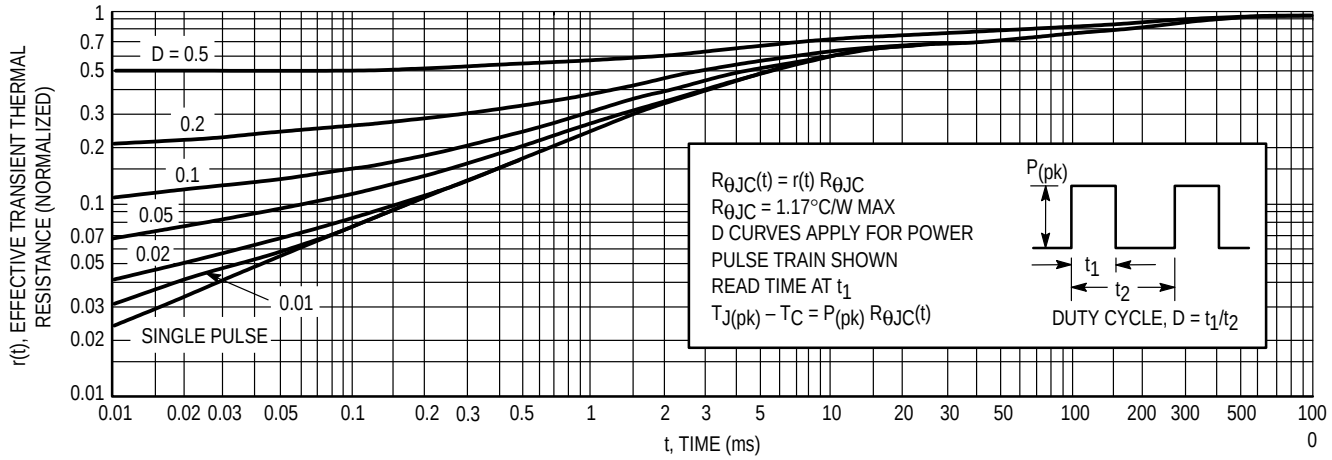


Figure 5. Thermal Response

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE–WHEEL DIODE
INPUT CONDITIONS	20 Ω, 5 V, 0, 1, 2 PW Varied to Attain I_C = 100 mA	+10 V, 33 2 W, D1, 22 µF, 2N6438, MR854, 160, 680 pF, 220, 100, MM3735, D1 D2 D3 D4 1N4934, 1 µF, I_{b1} ADJUST, I_{b2} ADJUST, dT_b ADJUST, dT, 2N3763, 2N6339, D3, D4, 22, PULSES δ = 3%, V_{CC}	DRIVER, V_D, I_D
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 10 V	
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1, INPUT, SEE ABOVE FOR DETAILED CONDITIONS, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, RS = 0.1 Ω, 2 OUTPUT WAVEFORMS: I_C, I_{CM}, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CEM}, V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	AV up to 50 V, CRONETICS PG130 up to 50 V, 5 µs 1%, 510, V_D, I_D

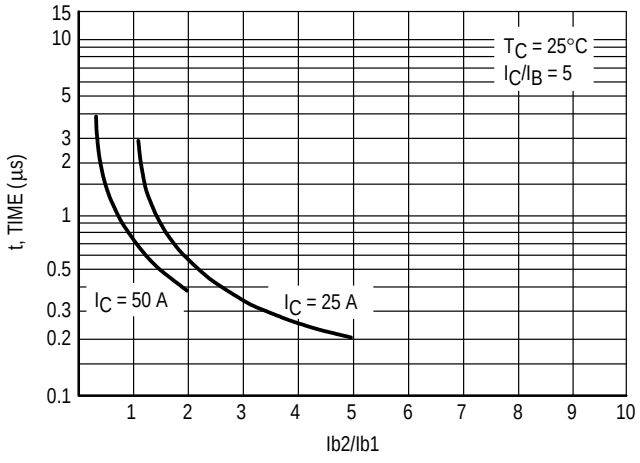


Figure 6. Fall Time versus IB2/IB1

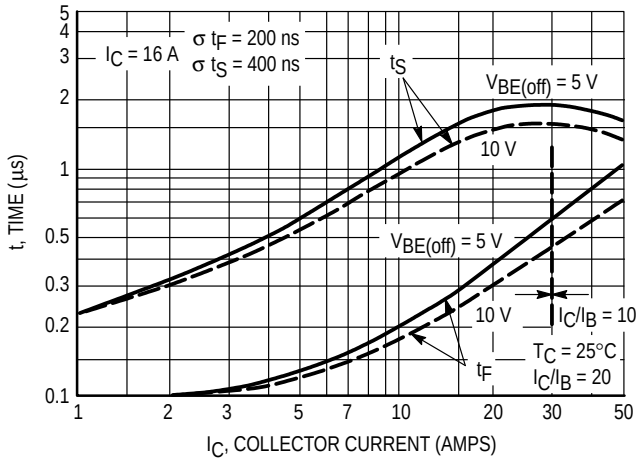


Figure 7. Turn–Off Time versus I_C

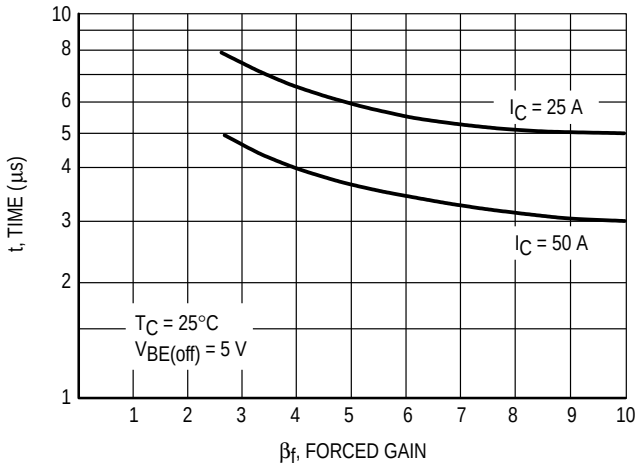


Figure 8. Storage Time versus Forced Gain

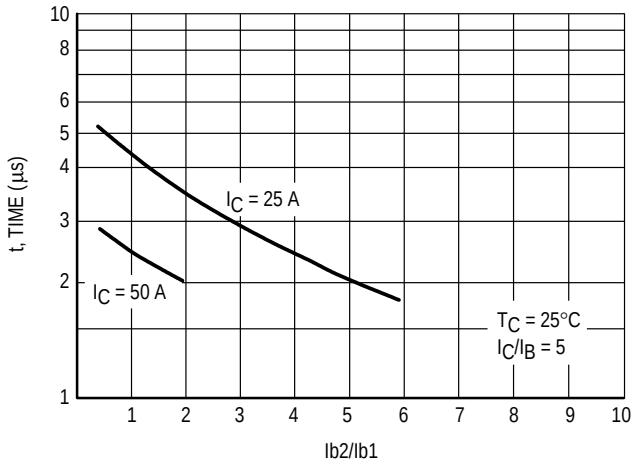


Figure 9. Storage Time versus Ib2/Ib1

FREE–WHEEL DIODE CHARACTERISTICS

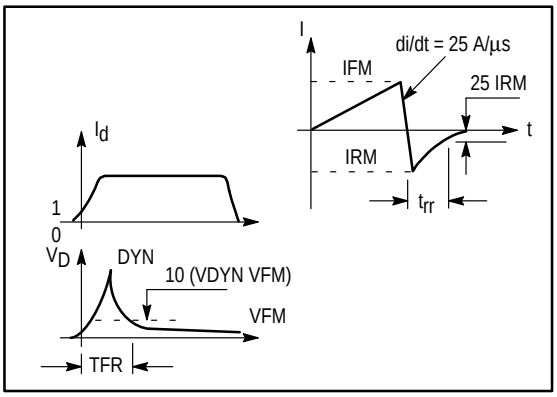


Figure 10. Free Wheel Diode Measurements

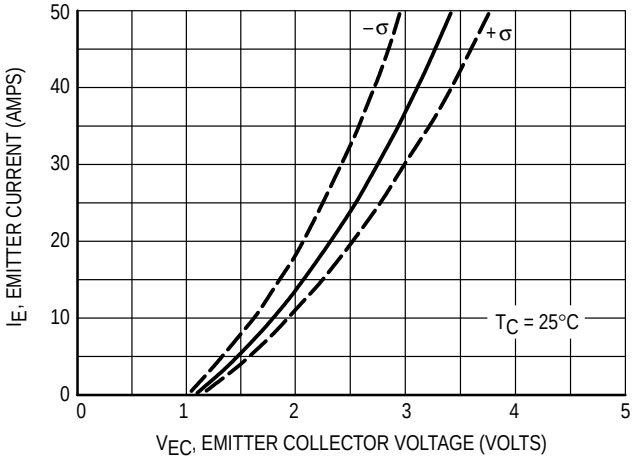


Figure 11. Forward Voltage

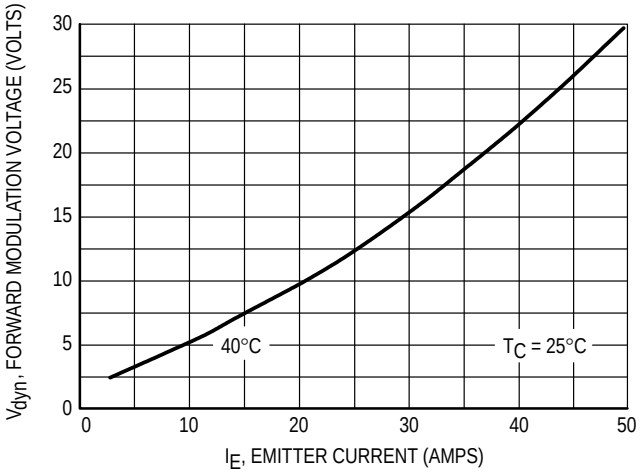


Figure 12. Forward Modulation Voltage

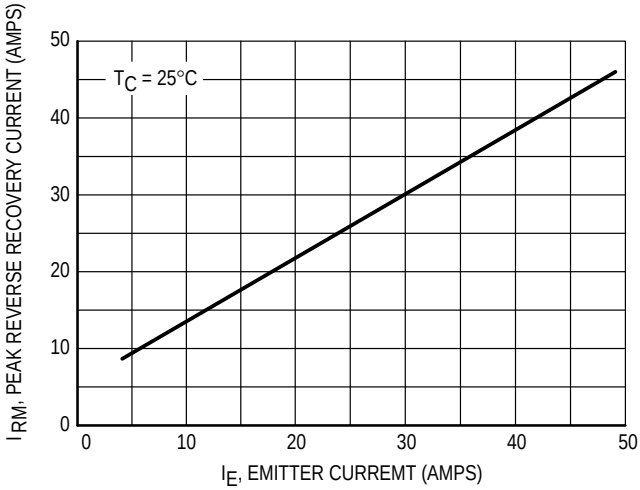


Figure 13. Peak Reverse Recovery Current

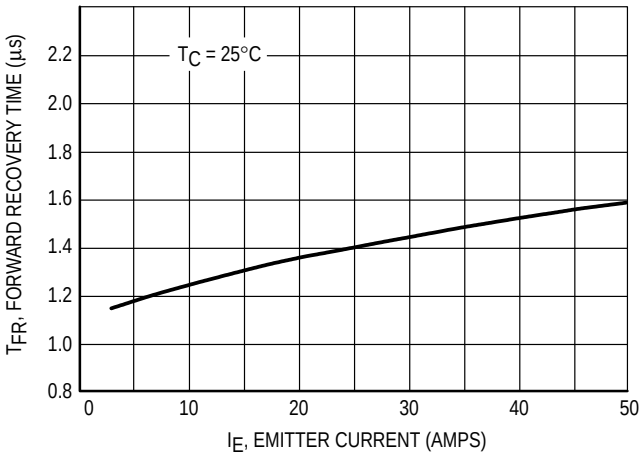


Figure 14. Forward Recovery Time

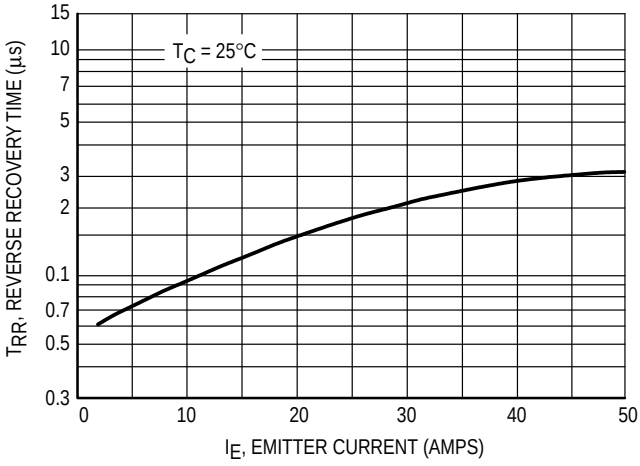


Figure 15. Reverse Recovery Time

The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

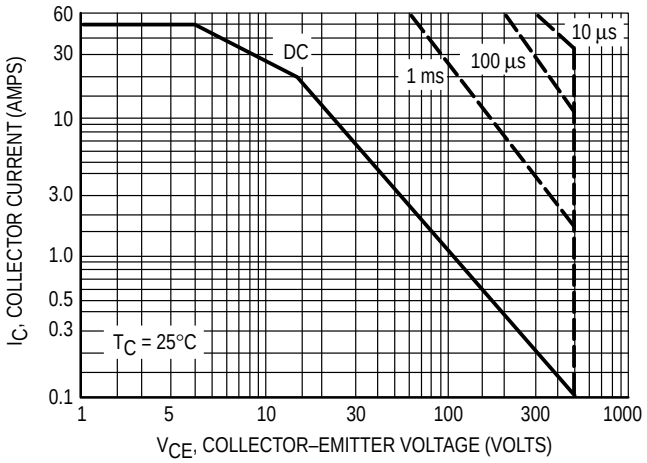


Figure 16. Safe Operating Area

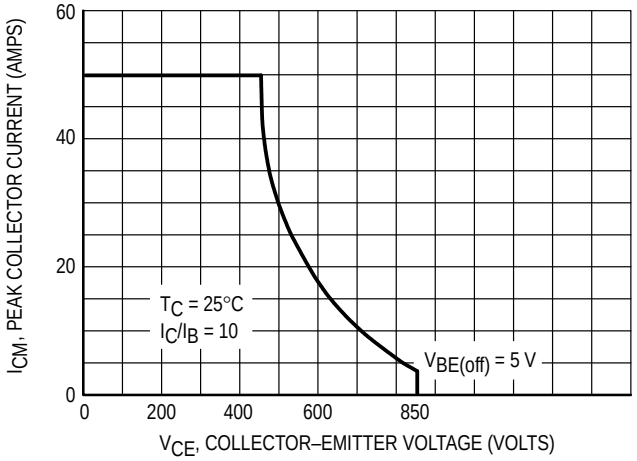


Figure 17. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

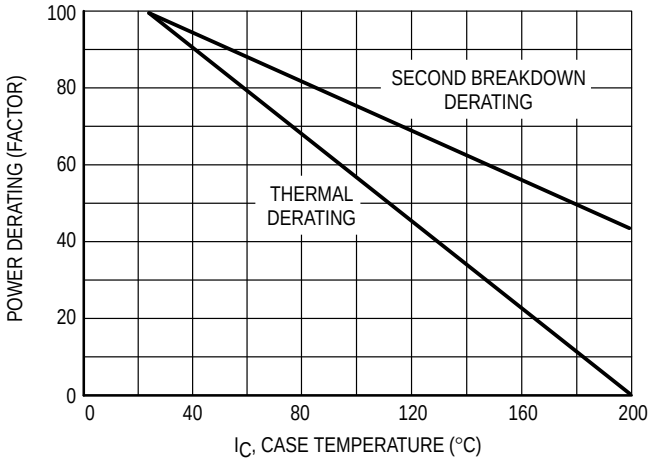
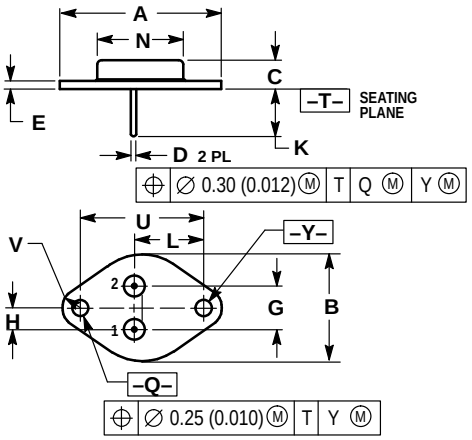


Figure 18. Power Derating

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 197A–05
TO–204AE (TO–3)
ISSUE J

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