



BUJ302AD

NPN power transistor

Rev. 01 — 28 March 2011

Product data sheet

1. Product profile

1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT428 (DPAK) surface mounted package.

1.2 Features and benefits

- Fast switching
- High voltage capability
- Low thermal resistance
- Surface-mountable package

1.3 Applications

- DC-to-DC converters
- High-frequency electronic lighting ballast applications
- Inverters
- Motor control systems

1.4 Quick reference data

Table 1. Quick reference data

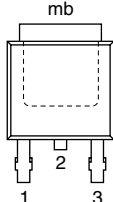
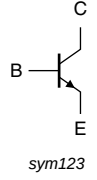
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_C	collector current	see Figure 1 ; see Figure 2 ; see Figure 4	-	-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; see Figure 3	-	-	80	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	-	1050	V
Static characteristics						
h_{FE}	DC current gain	$I_C = 0.1\text{ A}$; $V_{CE} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 11	[1]	48	66	100
		$I_C = 0.8\text{ A}$; $V_{CE} = 3\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 12	[1]	25	42	50

[1] Pulse test: pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ %}$



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base		
2	C	collector ^[1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

SOT428 (DPAK)

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUJ302AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	1050	V
V_{CEO}	collector-emitter voltage	$I_B = 0\text{ A}$	-	400	V
I_C	collector current	see Figure 1 ; see Figure 2 ; see Figure 4	-	4	A
I_{CM}	peak collector current		-	8	A
I_B	base current		-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; see Figure 3	-	80	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C
V_{EBO}	emitter-base voltage	$I_C = 0\text{ A}$; $I_E = 2\text{ A}$; $t_p < 10\text{ ms}$	-	24	V

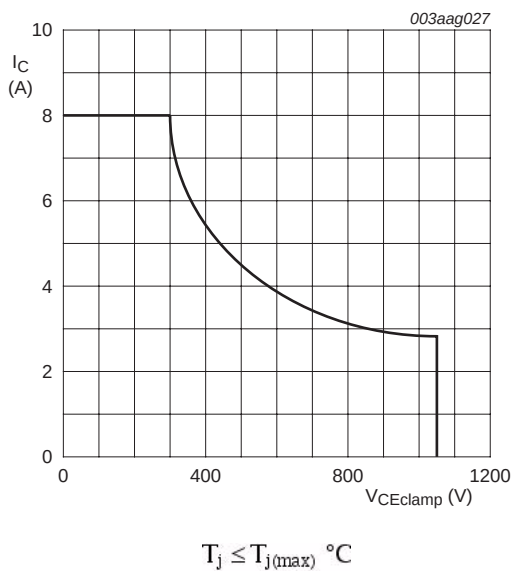
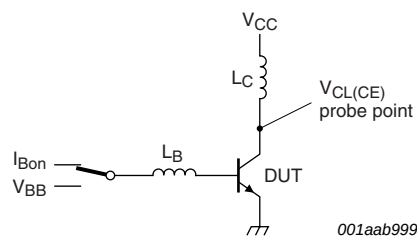
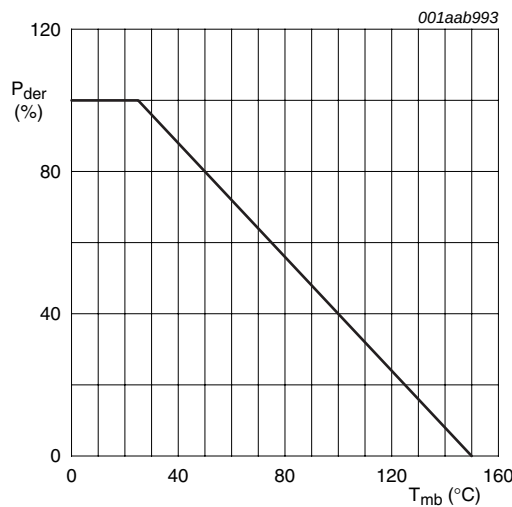


Fig 1. Reverse bias safe operating area



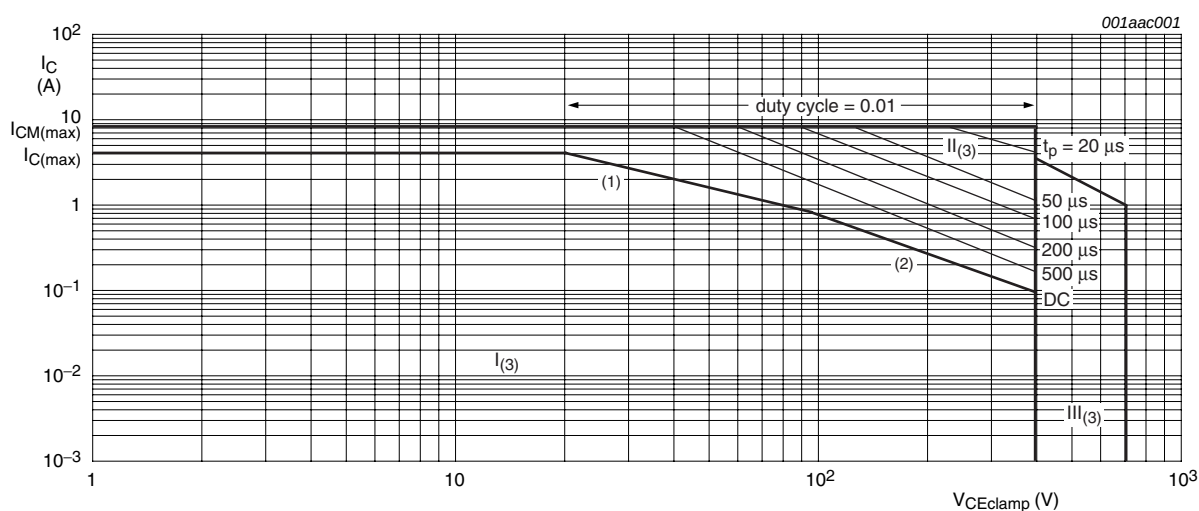
$V_{CL(CE)} \leq 1000 \text{ V}; V_{CC} = 150 \text{ V}; V_{BB} = -5 \text{ V};$
 $L_B = 1 \text{ } \mu\text{H}; L_C = 200 \text{ } \mu\text{H}$

Fig 2. Test circuit for reverse bias safe operating area



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig 3. Normalized total power dissipation as a function of mounting base temperature



- 1) P_{tot} maximum and P_{tot} peak maximum lines
- 2) Second breakdown limits
- 3) I = Region of permissible DC operation
 - II = Extension for repetitive pulse operation
 - III = Extension during turn-on in single transistor converters
provided that $R_{BE} \leq 100 \Omega$ and $t_p \leq 0.6 \mu s$

Fig 4. Forward bias safe operating area for $T_{mb} \leq 25^\circ C$

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air		-	60	-	K/W

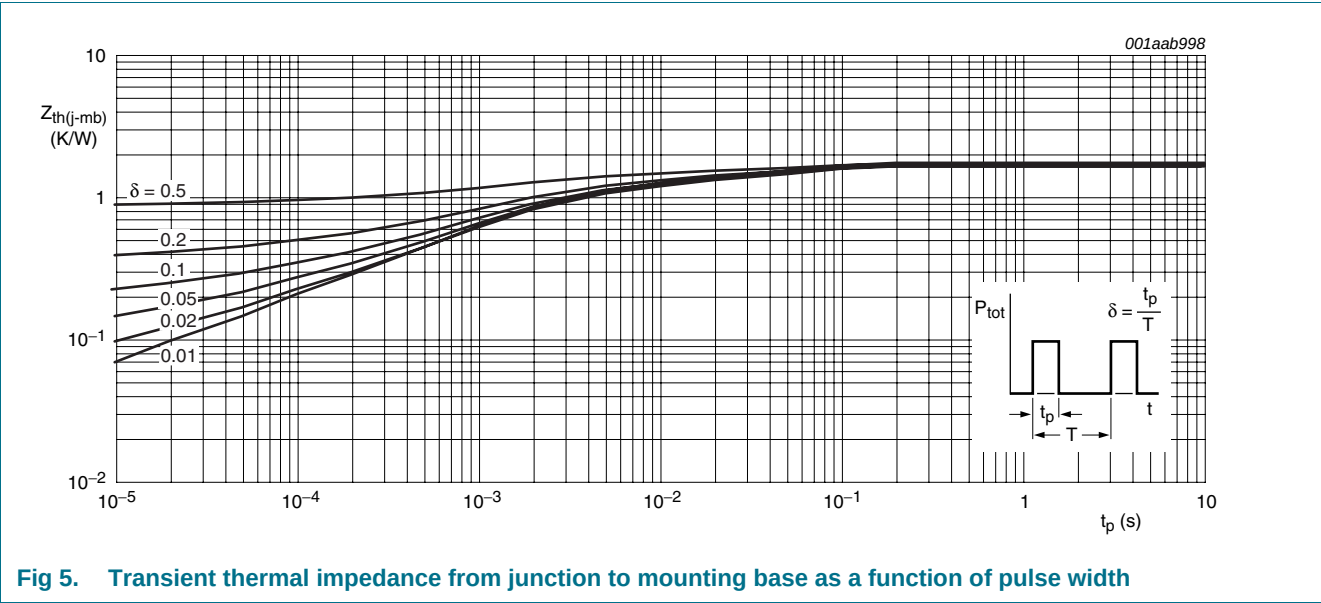


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{CES}	collector-emitter cut-off current	V _{BE} = 0 V; V _{CE} = 1050 V; T _{mb} = 25 °C	-	0.2	10	μA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 400 V; I _B = 0 A; T _{mb} = 25 °C	-	10	250	mA
V _{(BR)EBO}	open-collector emitter-base breakdown voltage	I _B = 1 mA; I _C = 0 A; T _{mb} = 25 °C	15	19	-	V
V _{CEOsus}	collector-emitter sustaining voltage	I _B = 0 A; I _C = 10 mA; L _C = 25 mH; T _{mb} = 25 °C; see Figure 6 ; see Figure 7	[1] 400	470	-	V
V _{CEsat}	collector-emitter saturation voltage	I _C = 1 A; I _B = 0.2 A; T _{mb} = 25 °C; see Figure 8 ; see Figure 9	[1] -	0.15	0.5	V
		I _C = 3.5 A; I _B = 1 A; T _{mb} = 25 °C; see Figure 8 ; see Figure 9	[1] -	0.6	1.5	V
V _{BEsat}	base-emitter saturation voltage	I _C = 3.5 A; I _B = 1 A; T _{mb} = 25 °C; see Figure 10	[1] -	1.1	1.5	V
h _{FE}	DC current gain	I _C = 0.1 A; V _{CE} = 5 V; T _{mb} = 25 °C; see Figure 11	[1] 48	66	100	
		I _C = 0.8 A; V _{CE} = 3 V; T _{mb} = 25 °C; see Figure 12	[1] 25	42	50	
Dynamic characteristics						
t _s	storage time	I _C = 2.5 A; I _{Bon} = 0.5 A; I _{Boff} = -0.5 A;	-	-	3.5	μs
t _f	fall time	R _L = 60 Ω; V _{BB} = -5 V; T _{mb} = 25 °C; resistive load; t _p = 300 μs; see Figure 13 ; see Figure 14	-	-	500	ns

[1] Pulse test: pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

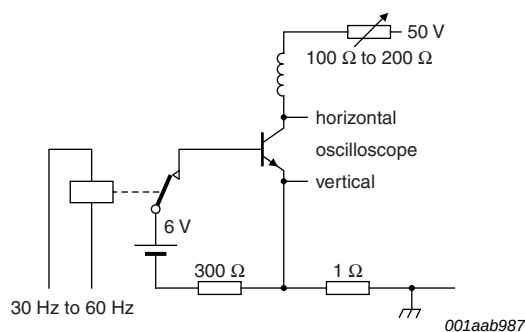


Fig 6. Test circuit for collector-emitter sustaining voltage

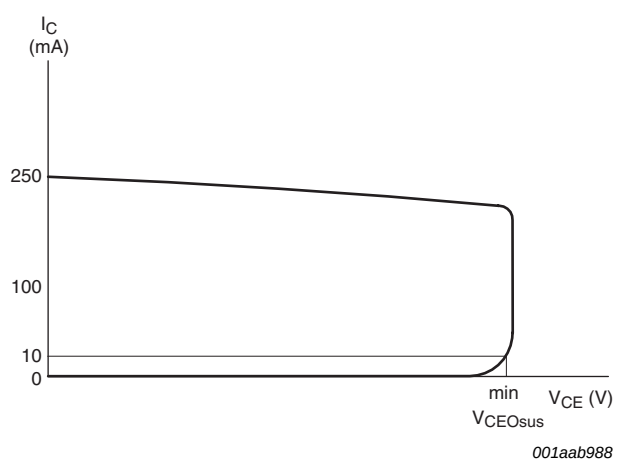


Fig 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

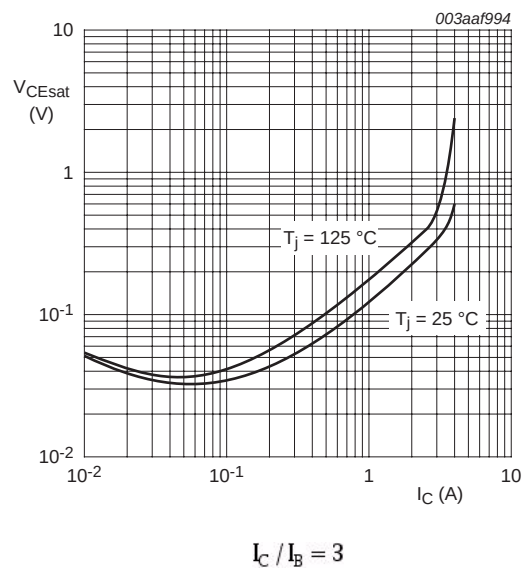


Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values

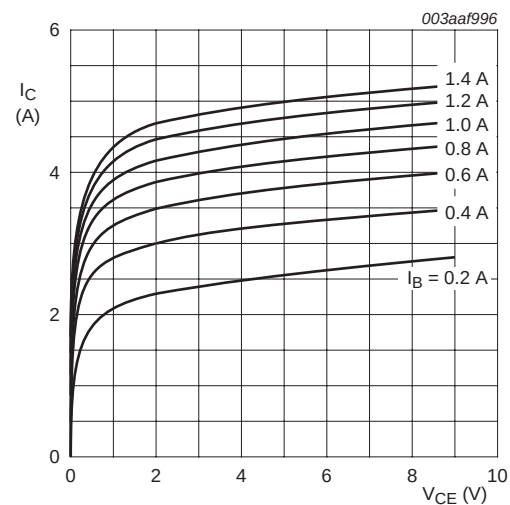


Fig 9. Collector current as a function of collector-emitter voltage; typical values

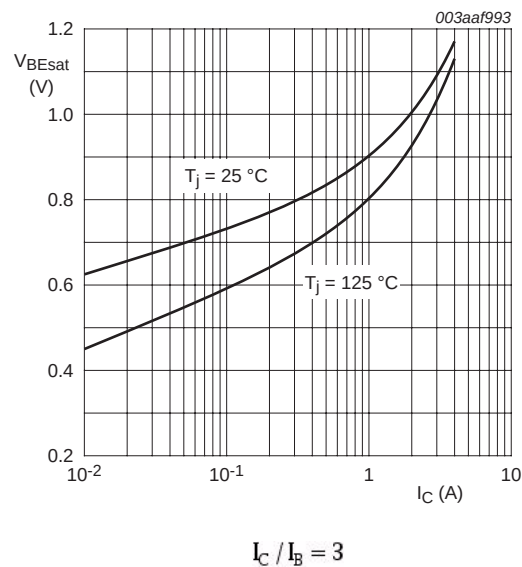


Fig 10. Base-emitter saturation voltage as a function of collector current; typical values

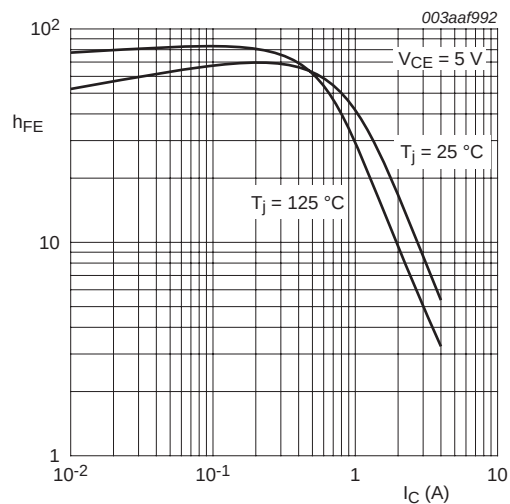


Fig 11. DC current gain as a function of collector current; typical values

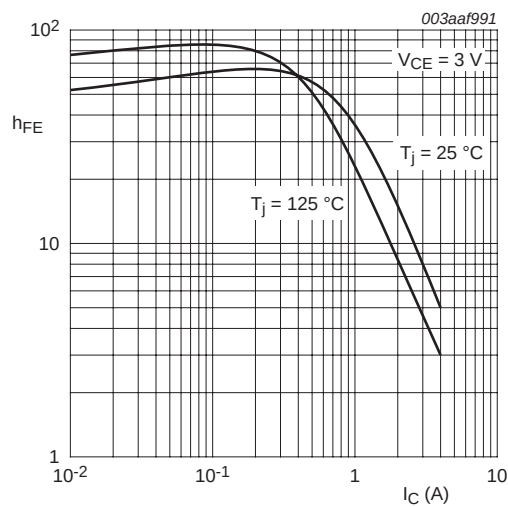
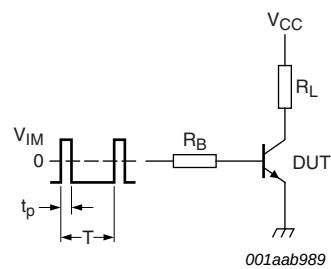


Fig 12. DC current gain as a function of collector current; typical values



$V_{IM} = -6\text{ to }+8\text{ V}$; $V_{CC} = 250\text{ V}$; $t_p = 20\text{ }\mu\text{s}$; $\delta = \frac{t_p}{T} = 0.01$
 R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 13. Test circuit for resistive load switching

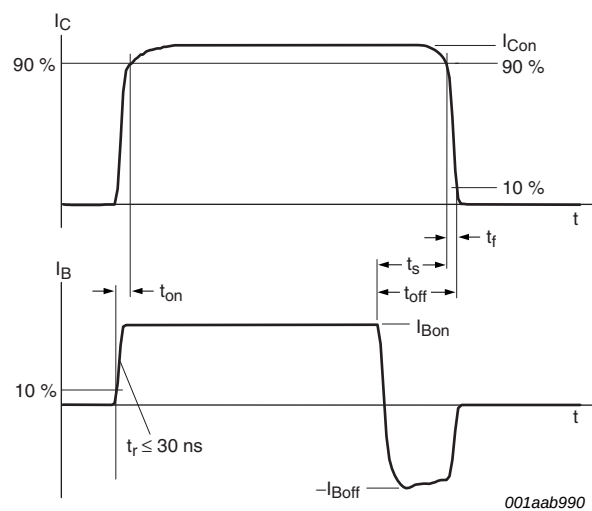


Fig 14. Switching times waveforms for resistive load

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428

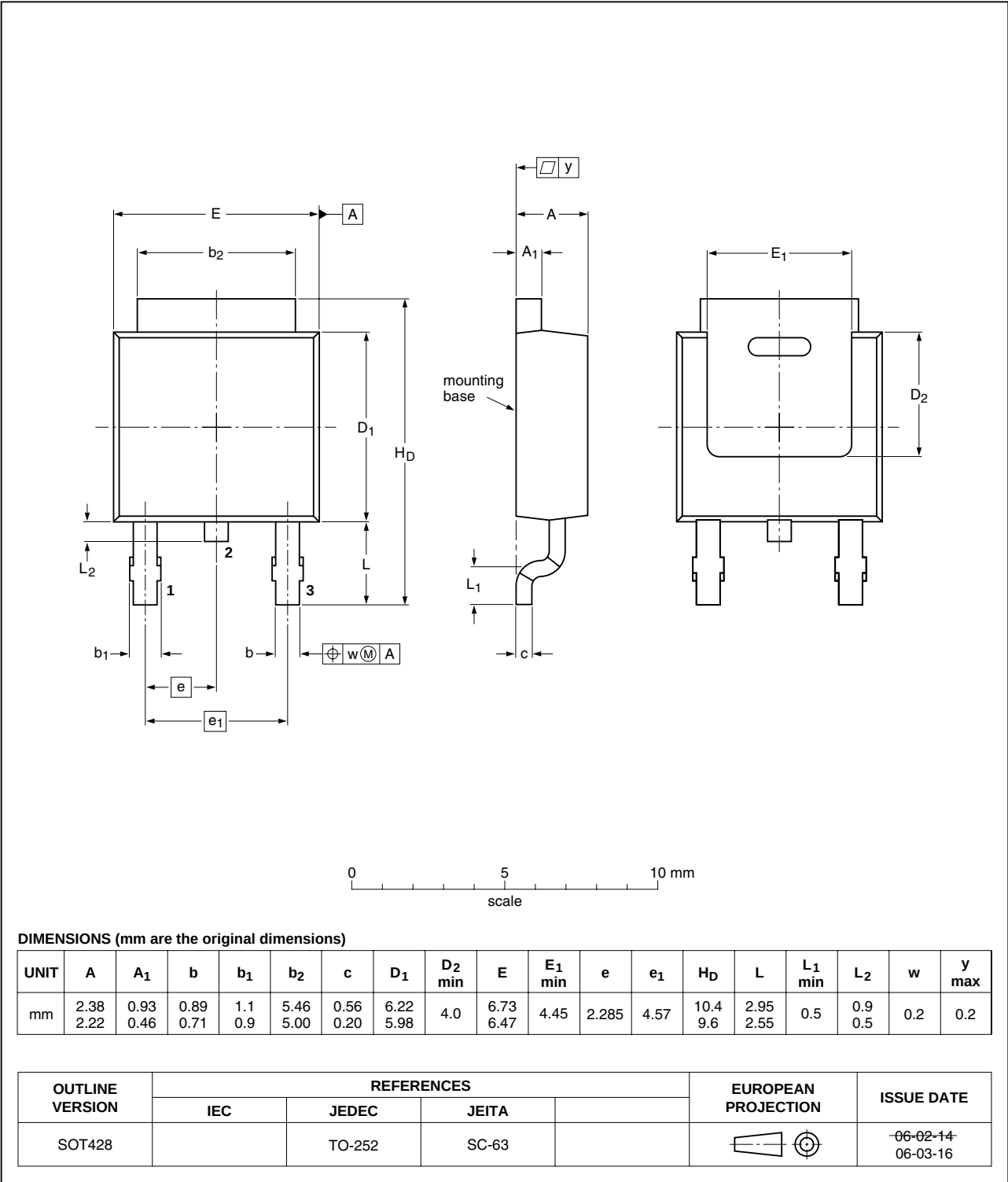


Fig 15. Package outline SOT428 (DPAK)

8. Soldering

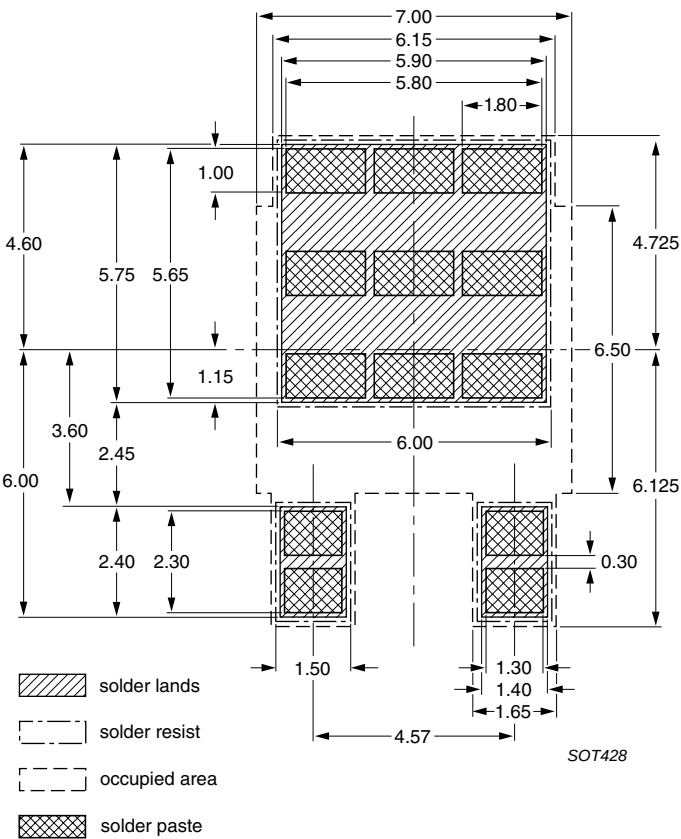


Fig 16. Reflow soldering footprint for SOT428 (DPAK)

9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUJ302AD v.1	20110328	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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