PLL frequency synthesizer for tuners
BU2618FV

The BU2618FV is a low current dissipation PLL frequency synthesizer designed for use in FM multiplex radio receiver and FM pager receiver. Featuring very small package and built-in prescaler that can operate at up to 130MHz.

●Applications

FM multiplex radio receivers, pagers, radios, and other signal generators

●Features

1) Built-in high-speed prescaler can divide 130 MHzVCO.
2) Low current dissipation (during operation: 1.5mA, PLL OFF: 200μA Typ.)
3) Seven standard frequencies: 25kHz, 12.5kHz, 6.25kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
4) Counter for intermediate frequency detection.
5) Unlock detection circuit.
6) Four output ports.
7) Serial data input (CE, CK, DA)

●Absolute maximum ratings (Ta = 25°C)

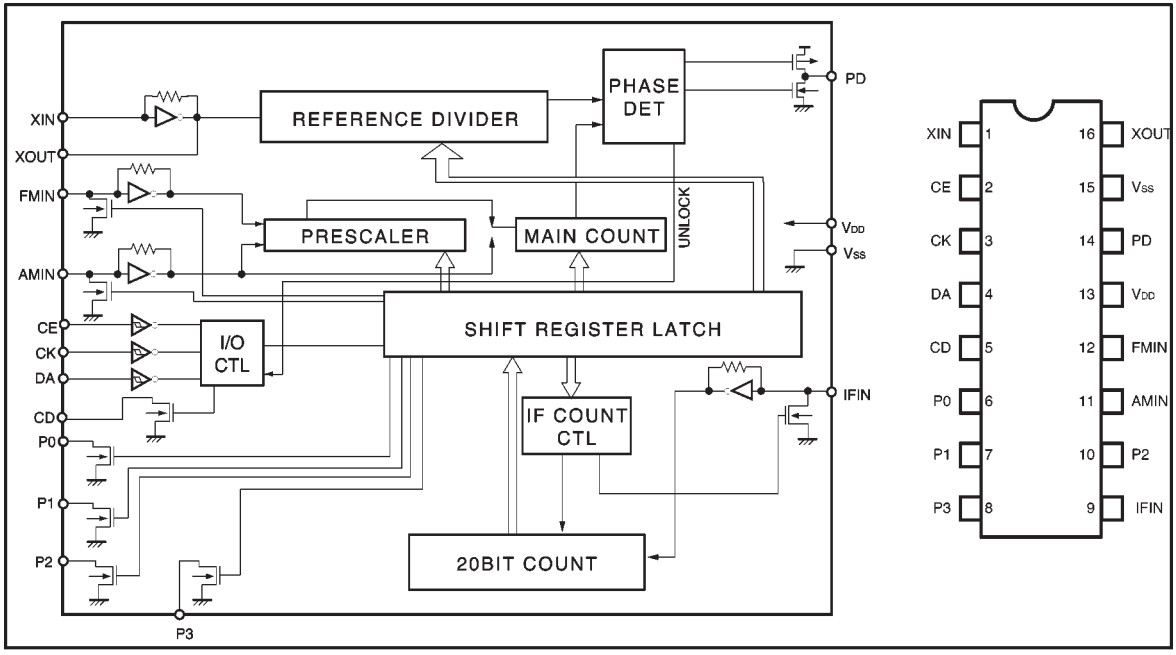
Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V_{DD}	−0.3～+7.0	V	V_{DD}
Maximum input voltage 1	V_{IN1}	−0.3～+7.0	V	CE, CK, DA
Maximum input voltage 2	V_{IN2}	−0.3～V_{DD}+0.3	V	XIN, FMIN, AMIN, IFIN
Maximum output voltage 1	V_{OUT1}	−0.3～+10.0	V	P_0, P_1, P_2, P_3, CD
Maximum output voltage 2	V_{OUT2}	−0.3～V_{DD}+0.3	V	PD, XOUT
Maximum output current	I_{OUT}	0～4.0	mA	P_0, P_1, P_2, P_3, CD
Power dissipation	Pd	350*	mW	—
Operating temperature	Topr	−25～+75	℃	—
Storage temperature	Tstg	−55～+125	℃	—

* Reduced by 3.5mW for each increase in Ta of 1 ℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	2.7	—	6.0	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	Pin description	Function	I / O
16	XOUT	Crystal oscillation terminal	For generation of standard frequency and internal clock.	OUT
1	XIN		Connected to 7.2 MHz crystal resonator.	IN
2	CE	Chip enable	When CE is H, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the timing of the fall of CE. Also, output data is output from the CD terminal synchronous to the rise of CK.	IN
3	CK	Clock signal		
4	DA	Serial data		
5	CD	Count data	Frequency data and unlock data are output.	Nch open drain
6	PO	Output port	Controlled on the basis of input data.	
7	P1			
8	P3			
9	IFIN	IF input	Input for frequency measurement	IN
10	P2	Output port	Controlled on the basis of input data.	Nch open drain
11	AMIN	AM input	Local input for AM	IN
12	FMIN	FM input	Local input for FM	IN
13	V_{DD}	Power supply	Power supply, with 2.7V to 6.0V applied voltage.	—
14	PD	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
15	V_{SS}	GROUND		—

∗ : When power is ON, pins 5 through 12 and pin 14 are not set until data is input.

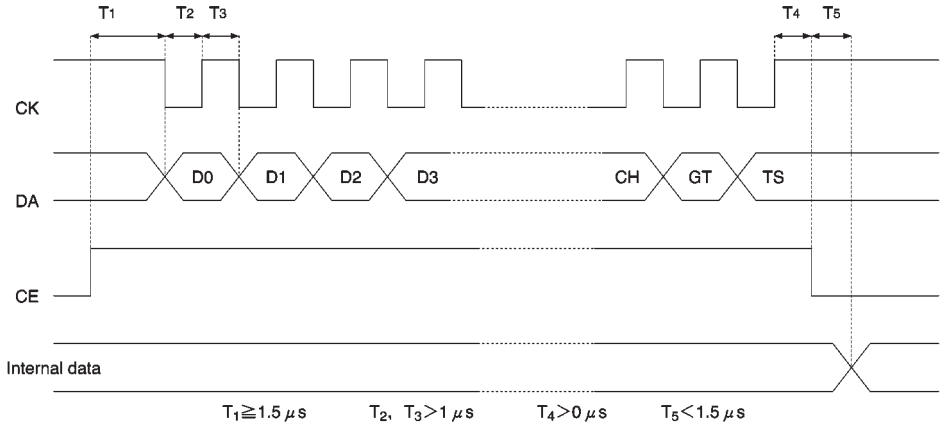
●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 3.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	I_{DD1}	—	1.5	2.5	mA	FM_{IN}=130MHz, 100mV_{rms}
Quiescent current	I_{DD2}	—	0.2	0.3	mA	No input, PLL=OFF
Input high level voltage	V_{IH}	0.8V_{DD}	—	—	V	CE, CK, DA terminals
Input low level voltage	V_{IL}	—	—	0.2V_{DD}	V	CE, CK, DA terminals
Input high level current 1	I_{IH1}	—	—	1.0	μA	CE, CK, DA terminals V_{IN}=V_{DD}
Input high level current 2	I_{IH2}	—	0.3	0.7	μA	XIN terminals V_{IN}=V_{DD}
Input high level current 3	I_{IH3}	5	10	15	μA	FMIN, AMIN, IFIN terminals V_{IN}=V_{DD}
Input low level current 1	I_{IL1}	−1.0	—	—	μA	CE, CK, DA terminals V_{IN}=V_{SS}
Input low level current 2	I_{IL2}	−0.7	−0.3	—	μA	XIN terminals V_{IN}=V_{SS}
Input low level current 3	I_{IL3}	5	10	−15	μA	FMIN, AMIN, IFIN terminals V_{IN}=V_{SS}
Output low level voltage 1	V_{OL1}	—	0.2	0.5	V	P_0 P_1 P_2 P_3 CD I_O=1.0mA
Off level leakage current 1	I_{OFF1}	—	—	1.0	μA	P_0 P_1 P_2 P_3 CD V_O=10V
Output low level voltage 2	V_{OL2}	—	—	0.5	V	FMIN AMIN IFIN I_{OUT}=0.1mA
Output high level voltage	V_{OH}	V_{DD}− 1.0	V_{DD}− 0.25	—	V	PD I_{OUT}=−1.0mA
Output low level voltage	V_{OL4}	—	0.15	1.0	V	PD I_{OUT}=1.0mA
Off level leakage current 2	I_{OFF2}	—	—	100	nA	PD V_{OUT}=V_{DD}
Off level leakage current 3	I_{OFF3}	−100	—	—	nA	PD V_{OUT}=V_{SS}
Internal feedback resistor 1	R_{F1}	3.8	10	16	MΩ	XIN
Internal feedback resistor 2	R_{F2}	300	500	1000	kΩ	FMIN, AMIN, IFIN
Input frequency 1	F_{IN1}	1	7.2	10	MHz	XIN ,sine wave, C coupling
Input frequency 2	F_{IN2}	10	—	130	MHz	FMIN ,sine wave, C coupling V_{IN}=100mV_{rms}
Input frequency 3	F_{IN3}	0.5	—	30	MHz	AMIN ,sine wave, C coupling V_{IN} =100mV_{rms}
Input frequency 4	F_{IN4}	0.4	—	12	MHz	IFIN ,sine wave, C coupling V_{IN} =100mV_{rms}
Maximum input amplitude	F_{INMAX}	—	—	1.0	Vrms	XIN ,FMIN ,AMIN ,IFIN, sine wave, C coupling
Minimum pulse width	TW	—	1.0	—	μs	CK, DA
Input rise time	TR	—	—	500	ns	CE, CK, DA
Input fall time	TF	—	—	500	ns	CE, CK, DA

◎ Not designed for radiation resistance.

●Circuit operation

・Input data format



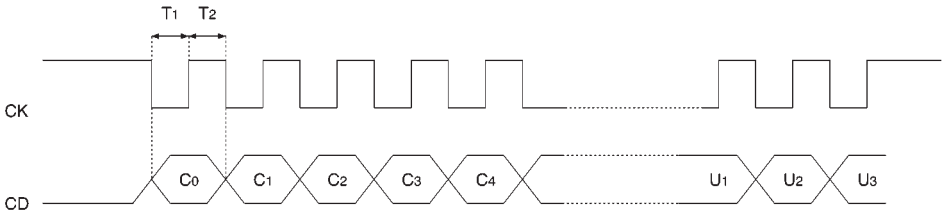
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

← Input from D0.

P0	P1	P2	P3	*	*	*	CT	R0	R1	R2	S	PS	*	GT	TS

*：Irrelevant

・Output data format CE output is set to LO.



Figures for output assume the presence of pullup resistance. T_1, $T_2 > 1\ \mu s$

Output data format

C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15

C16	C17	C18	C19	U0	U1	U2	U3

← Input done from C0.

* Data is output only when CT = 1 or GT = 1.

• Explanation of the data

(1) Division data: For D_0 through D_{15} (When S = 0, use D_4 through D_{15}.)

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Examples:

Divide ratio=1106(D) 1106(D)÷2=553(D)=229(H) S=0, PS=0

0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0

Divide ratio=1107(D)=453(H) S=1, PS=1

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0

Divide ratio=926(D)=39E(H) S=1, PS=0

×	×	×	×	0	1	1	1	1	0	0	1	1	1	0	0

(2) CT: Frequency measurement beginning data
1: Begins measurement.
0: Resets internal counter, IFIN goes to pulldown.

(3) Output port control data:
1: Open drain output ON
2: Open drain output OFF

(4) R_0, R_1, R_2, standard frequency data

Data			
R_0	R_1	R_2	Standard frequency
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	6.25kHz
0	1	1	10kHz
1	0	0	5kHz
1	0	1	9kHz
1	1	0	1kHz
1	1	1	∗ PLL OFF

∗ FMIN = pulldown, AMIN = pulldown, PD = high impedance

(5) S: switch between FMIN and AMIN
0: FMIN 1: AMIN

(6) PS: If this bit is set to ON while AMIN is selected, swallow counter division is possible.

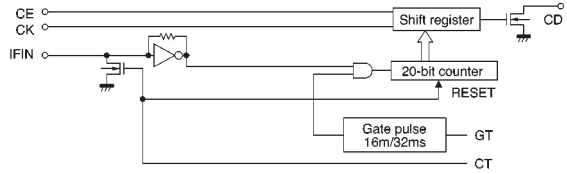
(7) GT: Frequency measurement time and unlock detection ON/OFF

CT	GT	Frequency measurement	Unlock detection	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time = 16 ms	ON	
1	1	ON Gate time = 32 ms	ON	

(8) TS: Test data (0) is input

• Frequency counter

(1) Structure



(2) How the frequency counter operates

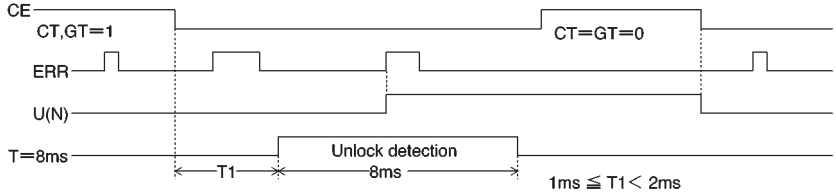
When control data CT equals 1, the 20-bit counter and the amp go into operation. When CT equals 0, amp input goes to pulldown and the counter is reset. Measuring time (gate pulse) is selected (16ms / 32ms) on the basis of control data GT. When control data CT equals 0, the counter is reset.

(3) Explanation of output data

D_0: LSB D_{19}: MSB

Unlock detection

When control data GT equals 1, or CT equals 1, the unlock detection circuit goes into operation for 8 ms. When CT equals 1, the unlock detection circuits stops operating before the frequency counter gate pulse is emitted. When CT equals 0, or GT equals 0, the unlock detection circuit is reset.

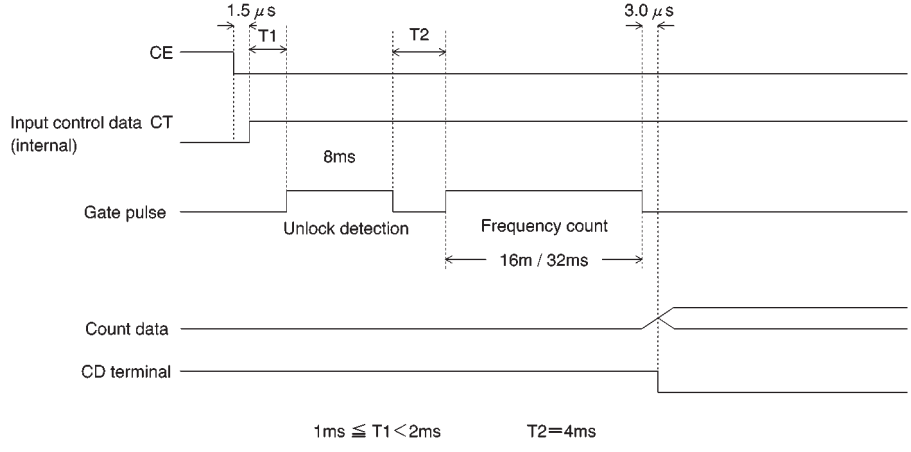


Explanation of the output data

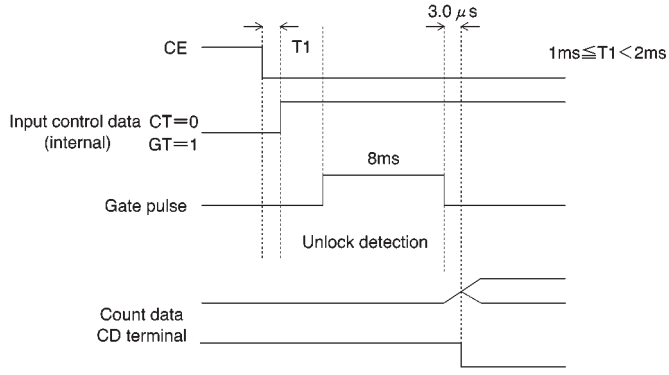
U0	U1	U2	U3					
0	0	0	0			ERR	<	1.1 μs
1	0	0	0	1.1 μs	<	ERR	<	2.2 μs
1	1	0	0	2.2 μs	<	ERR	<	3.3 μs
1	1	1	0	3.3 μs	<	ERR	<	4.4 μs
1	1	1	1	4.4 μs	<	ERR		

• Frequency counter and unlock detection

(1) When CT = 1: Frequency count and unlock detection are carried out.

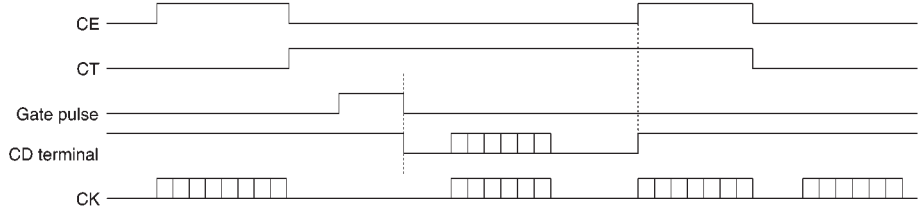


(2) When CT = 0 and GT = 1: Only unlock detection is carried out.



• Explanation of CD

When frequency measurement or unlock detection is finished, the CD terminal goes to LO to indicate that the count and unlock detection have finished. It also synchronizes with CK to output counter data. When the next data is input, it goes to HI.



●Electrical characteristics curves

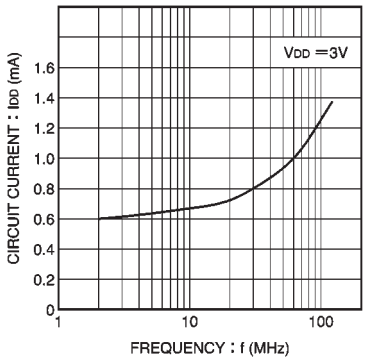


Fig. 1 Operating frequency vs.supply current characteristics

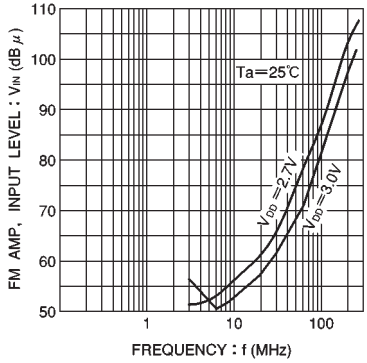


Fig. 2 FM amp input leve vs. frequency characteristics

●External dimensions (Units: mm)

