STRUCTURE Silicon Monolithic Integrated Circuit

TYPE **BU2098F**

FUNCTION 8bit Serial IN / Parallel Out Driver

FEATURES 1) Compatible with I^2C BUS

2) Nch open drain, capable of driving a maximum of 25mA

3) 18V high voltage output can be used.

● ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{DD}	7.0*	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	T_{opr}	-40～+85	℃
Storage Temperature Range	T_{stg}	-55～+125	℃
Input Voltage	V_{IN}	-0.5～V_{DD}+0.5	V

* Output (Q0～Q7) are 18V (Max.)

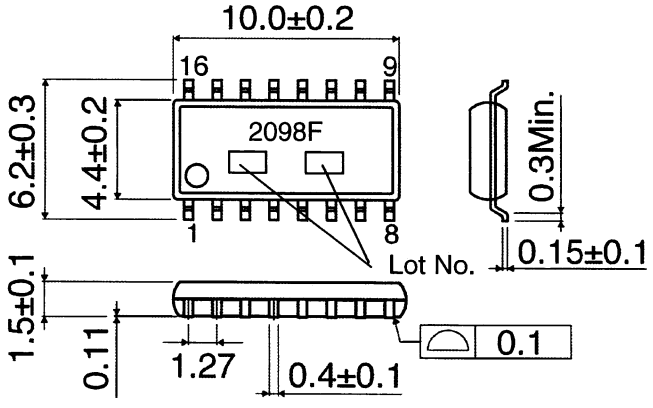
・Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any difference in translation version of this document, formal version takes priority.

● ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25℃, V_{DD}=5.0V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Power Supply Voltage range	V_{DD}	2.7	-	5.5	V	VDD pin
Output Voltage range	V_o	0	-	15.0	V	
Supply current	I_{cc1}	-	-	2.0	μA	Static supply current
Input "H" voltage	V_{IH}	0.7	-	-	V/V	Ratio against VDD
Input "L" voltage	V_{IL}	-	-	0.3	V/V	Ratio against VDD
Output "L" voltage	V_{OL}	-	-	0.4	V	
Input "L" current	I_{IL}	-	-	2.0	μA	Vin=0
Input "L" current	I_{IH}	-	-	-2.0	μA	Vin=VDD
Output Leakage current	I_L	-	-	±5.0	μA	Output=OPEN,Vout=VDD
Data Minimum set up time	t_1	100	-	-	n S	High speed mode
Data hold time	t_2	-	-	900	nS	High speed mode
Minimum shift pulse width (High speed mode)	t_{31}	0	-	400	KHz	
Minimum shift pulse width (normal mode)	t_{32}	0	-	100	KHz	

This product is not assessed whether to be strategic materials in foreign exchange and trade law or not, so please confirm at trading. This product is not deigned against radioactive ray.

● PHYSICAL DIMENSIONS

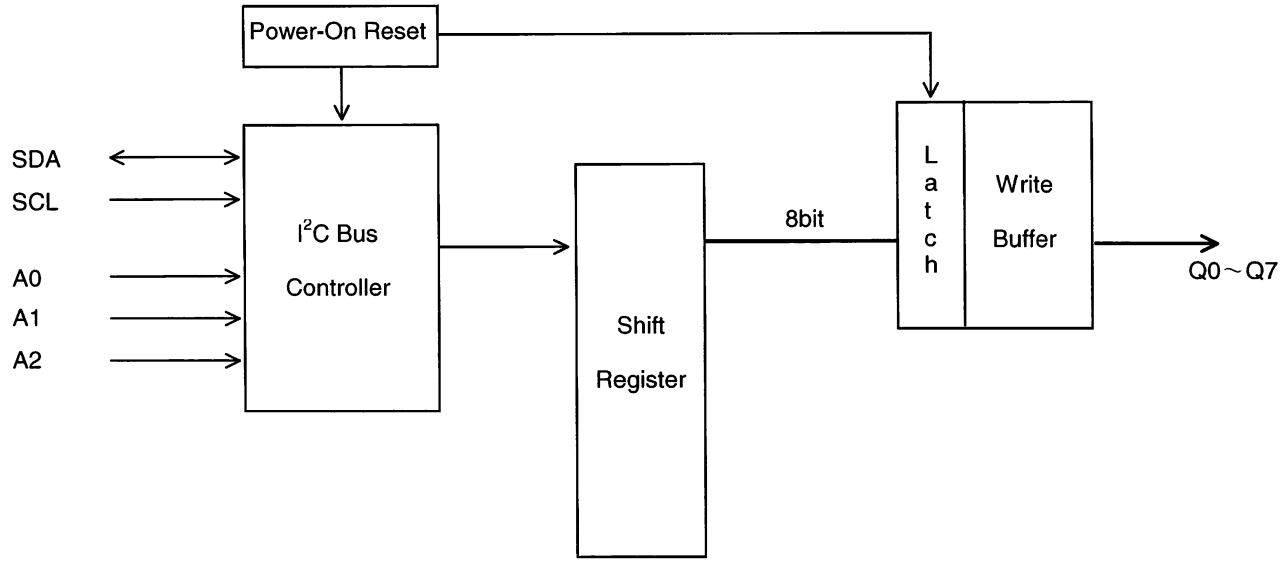


SOP16 (UNIT : mm)

● Pin Description

Pin. No	Terminal	Symbol	Function
14	SCL	C	Shift pulse for shift register
15	SDA	S_I	Data input for shift register, data is set at rising edge of shift pulse
1	A0	A_o	Address input 0
2	A1	A_1	Address input 1
3	A2	A_2	Address input 2
4	Q0	O_0	1st bit output, it becomes "1" when data in register is "1"
5	Q1	O_1	2nd bit output, it becomes "1" when data in register is "1"
6	Q2	O_2	3rd bit output, it becomes "1" when data in register is "1"
7	Q3	O_3	4th bit output, it becomes "1" when data in register is "1"
9	Q4	O_4	5th bit output, it becomes "1" when data in register is "1"
10	Q5	O_5	6th bit output, it becomes "1" when data in register is "1"
11	Q6	O_6	7th bit output, it becomes "1" when data in register is "1"
12	Q7	O_7	8th bit output, it becomes "1" when data in register is "1"
13	NC	NC	NC pin
8	VSS	GND	GND
16	VDD	VDD	Power supply

● BLOCK DIAGRAM



● NOTES FOR USE

(1) Absolute maximum ratings
Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.

(2) Ground Potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

(3) Thermal design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Electromagnetic fields
Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.

(5) Ground wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

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