

BT151-500L

SCR, 12 A, 5mA, 500 V, SOT78

Rev. 05 — 2 March 2009

Product data sheet

1. Product profile

1.1 General description

Planar passivated SCR (Silicon Controlled Rectifier) in a SOT78 plastic package.

1.2 Features and benefits

- High reliability
- High surge current capability
- High thermal cycling performance

1.3 Applications

- Ignition circuits
- Motor control
- Protection Circuits
- Static switching

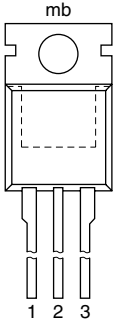
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	500	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{mb}} \leq 109\text{ }^{\circ}\text{C}$; see Figure 3	-	-	7.5	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{mb}} \leq 109\text{ }^{\circ}\text{C}$; see Figure 1 ; see Figure 2	-	-	12	A
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; $I_{\text{T}} = 100\text{ mA}$; see Figure 8	-	2	5	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	mb	anode		
			SOT78 (TO-220AB;SC-46)	

3. Ordering information

Table 3. Ordering information

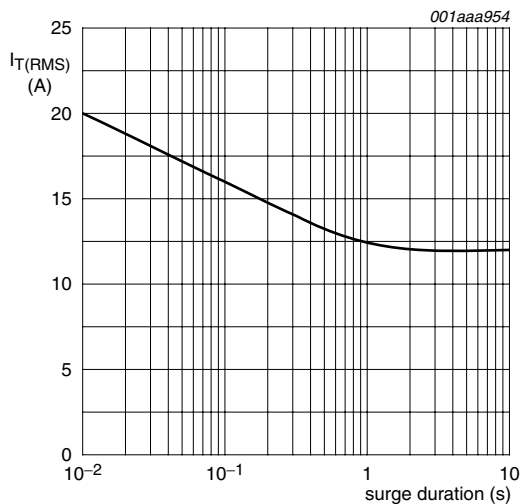
Type number	Package		Version
	Name	Description	
BT151-500L	TO-220AB; SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	500	V
V_{RRM}	repetitive peak reverse voltage		-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 109\text{ }^{\circ}\text{C}$; see Figure 3	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 109\text{ }^{\circ}\text{C}$; see Figure 1 ; see Figure 2	-	12	A
di_T/dt	rate of rise of on-state current	$I_T = 20\text{ A}$; $I_G = 50\text{ mA}$; $di_G/dt = 50\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$
I_{TSM}	non-repetitive peak on-state current	half sine wave; $t_p = 8.3\text{ ms}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$	-	132	A
		half sine wave; $t_p = 10\text{ ms}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; see Figure 4 ; see Figure 5	-	120	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	72	A^2s
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
V_{RGM}	peak reverse gate voltage		-	5	V



$$f = 50\text{ Hz}; T_{mb} = 109\text{ }^{\circ}\text{C}$$

Fig 1. RMS on-state current as a function of surge duration; maximum values

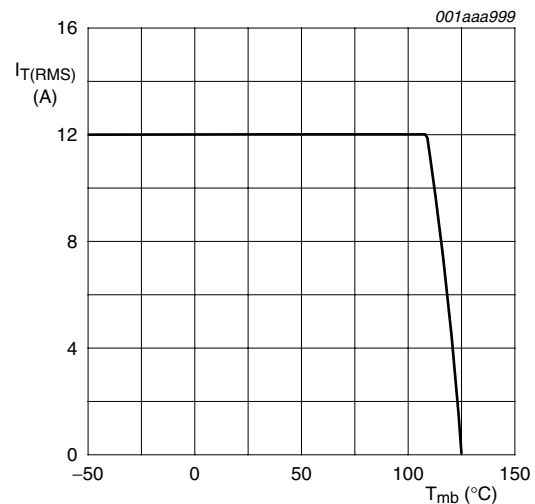
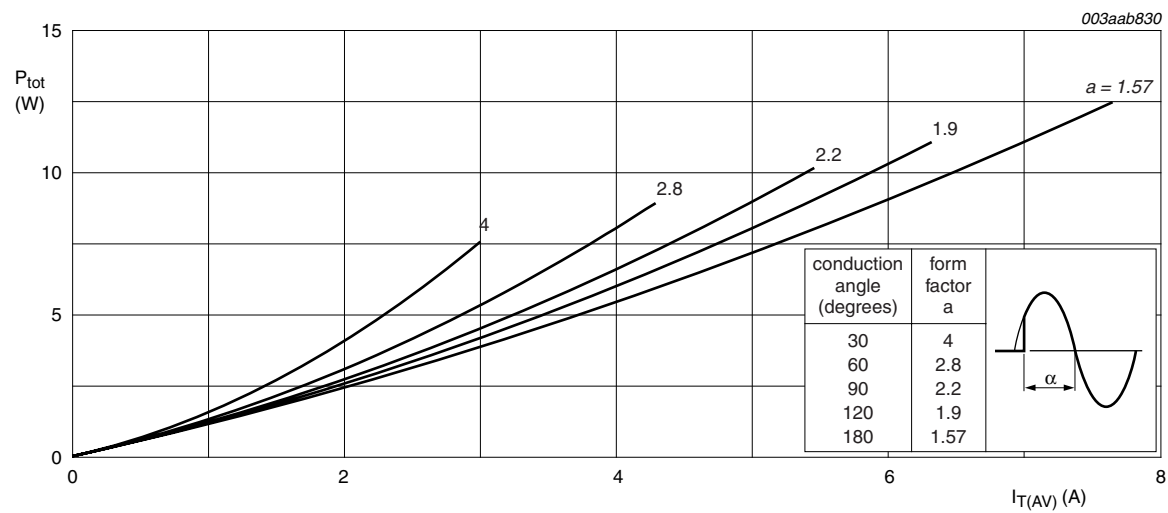
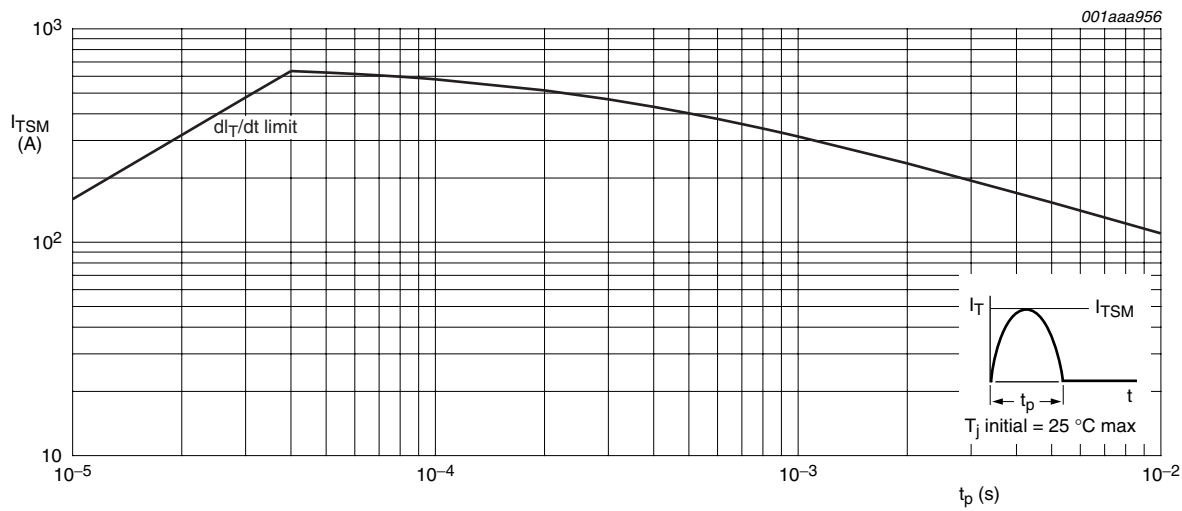


Fig 2. RMS on-state current as a function of mounting base temperature; maximum values



$a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

Fig 3. Total power dissipation as a function of average on-state current; maximum values



$t_p = 10\text{ ms}$

Fig 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

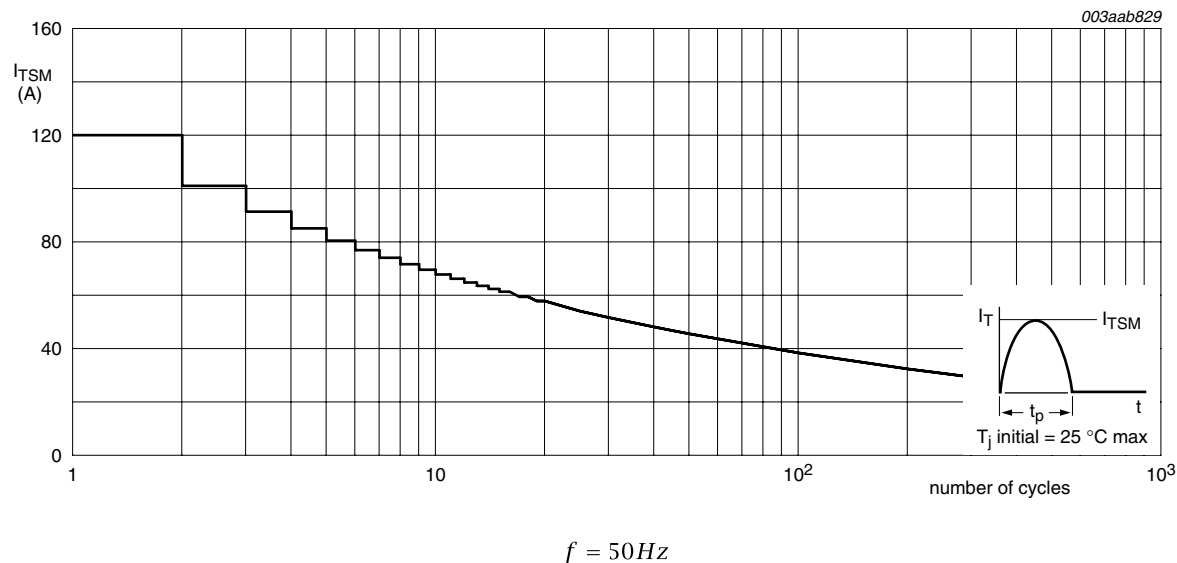


Fig 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 6	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air		-	60	-	K/W

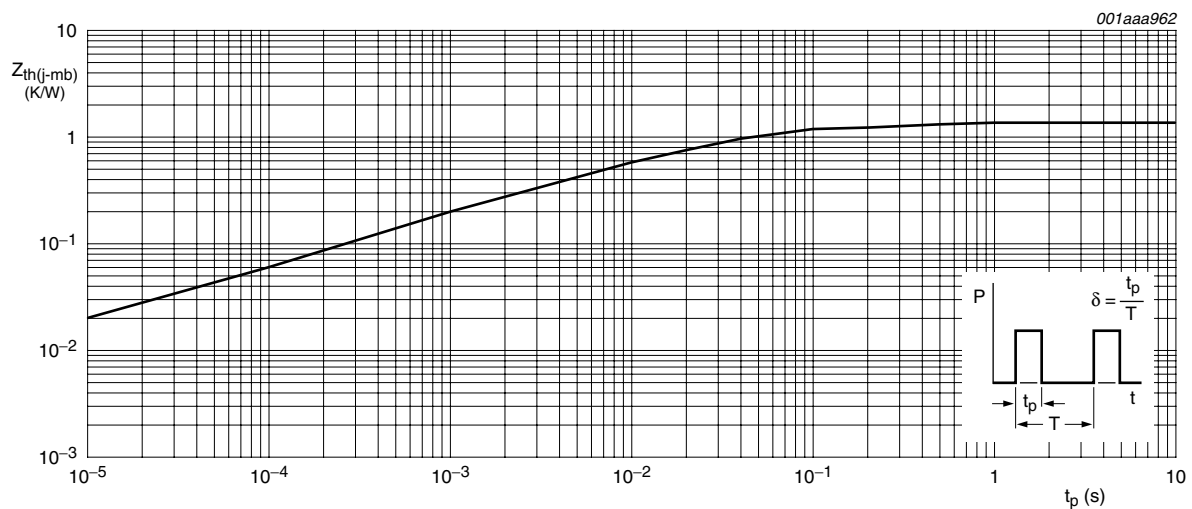
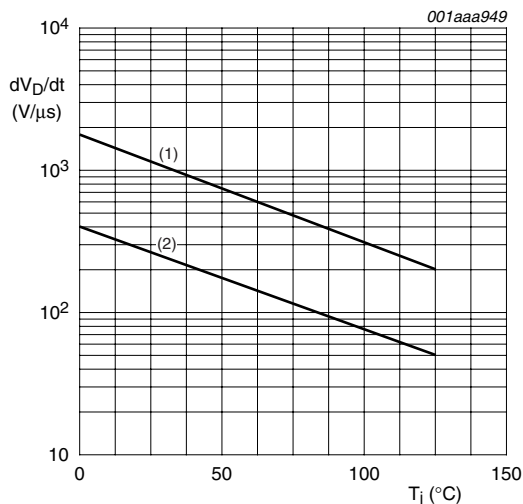


Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; $I_T = 100\text{ mA}$; see Figure 8	-	2	5	mA
I_L	latching current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; see Figure 9	-	10	40	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; see Figure 10	-	7	20	mA
V_T	on-state voltage	$I_T = 23\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11	-	1.4	1.75	V
V_{GT}	gate trigger voltage	$I_T = 100\text{ mA}$; $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; see Figure 12	-	0.6	1.5	V
		$I_T = 100\text{ mA}$; $V_D = 500\text{ V}$; $T_j = 125\text{ °C}$	0.25	0.4	-	V
I_D	off-state current	$V_D = 500\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
I_R	reverse current	$V_R = 500\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 335\text{ V}$; $T_j = 125\text{ °C}$; exponential waveform; gate open circuit	50	130	-	V/ μ s
		$V_{DM} = 335\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 100\text{ }\Omega$; exponential waveform; see Figure 7	200	1000	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$; $V_D = 500\text{ V}$; $I_G = 100\text{ mA}$; $di_G/dt = 5\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$	-	2	-	μ s
t_q	commutated turn-off time	$V_{DM} = 335\text{ V}$; $T_j = 125\text{ °C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $(di_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK} = 100\text{ }\Omega$	-	70	-	μ s



- (1) $R_{GK} = 100\text{ }\Omega$
 (2) Gate open circuit

Fig 7. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

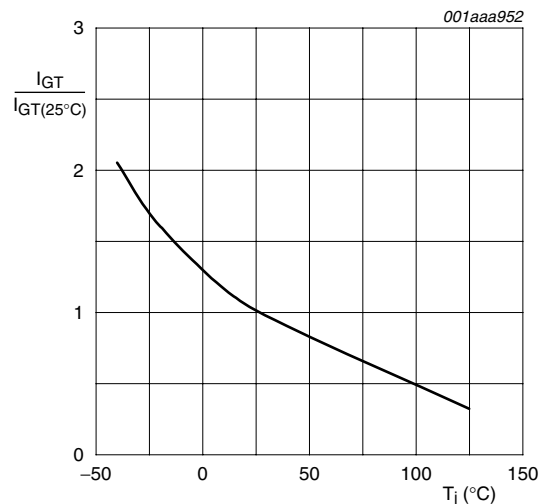


Fig 8. Normalized gate trigger current as a function of junction temperature

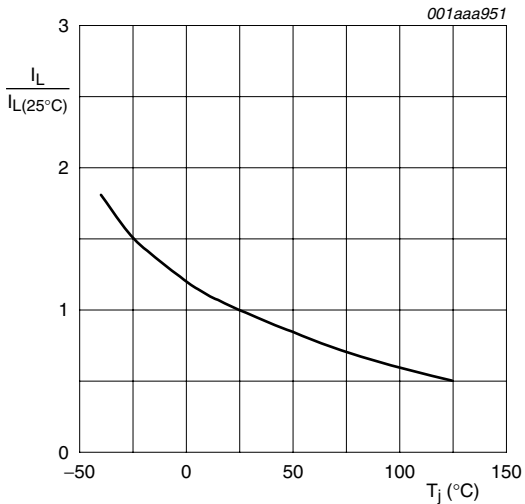


Fig 9. Normalized latching current as a function of junction temperature

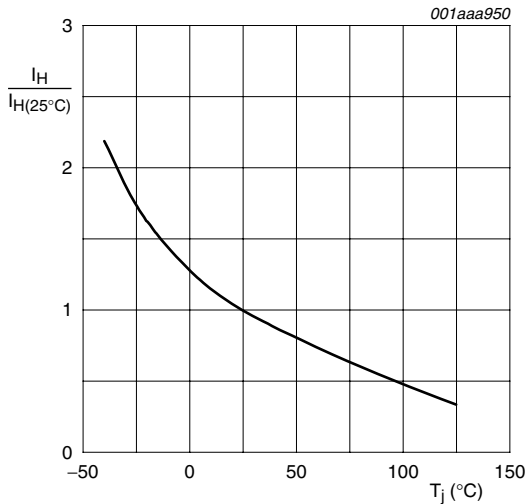
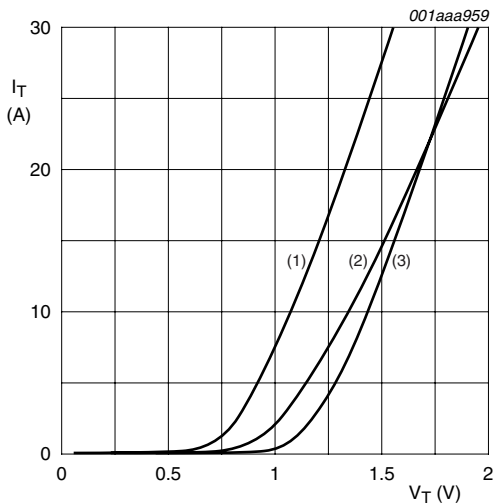


Fig 10. Normalized holding current as a function of junction temperature



$V_0 = 1.06 \text{ V}; R_s = 0.0304 \Omega$
(1) $T_j = 150 \text{ }^\circ\text{C}$; typical values
(2) $T_j = 150 \text{ }^\circ\text{C}$; maximum values
(3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig 11. On-state current as a function of on-state voltage

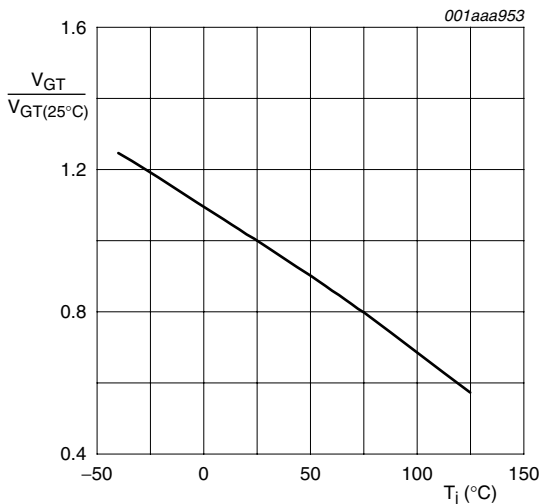


Fig 12. Normalized gate trigger voltage as a function of junction temperature

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB SOT78

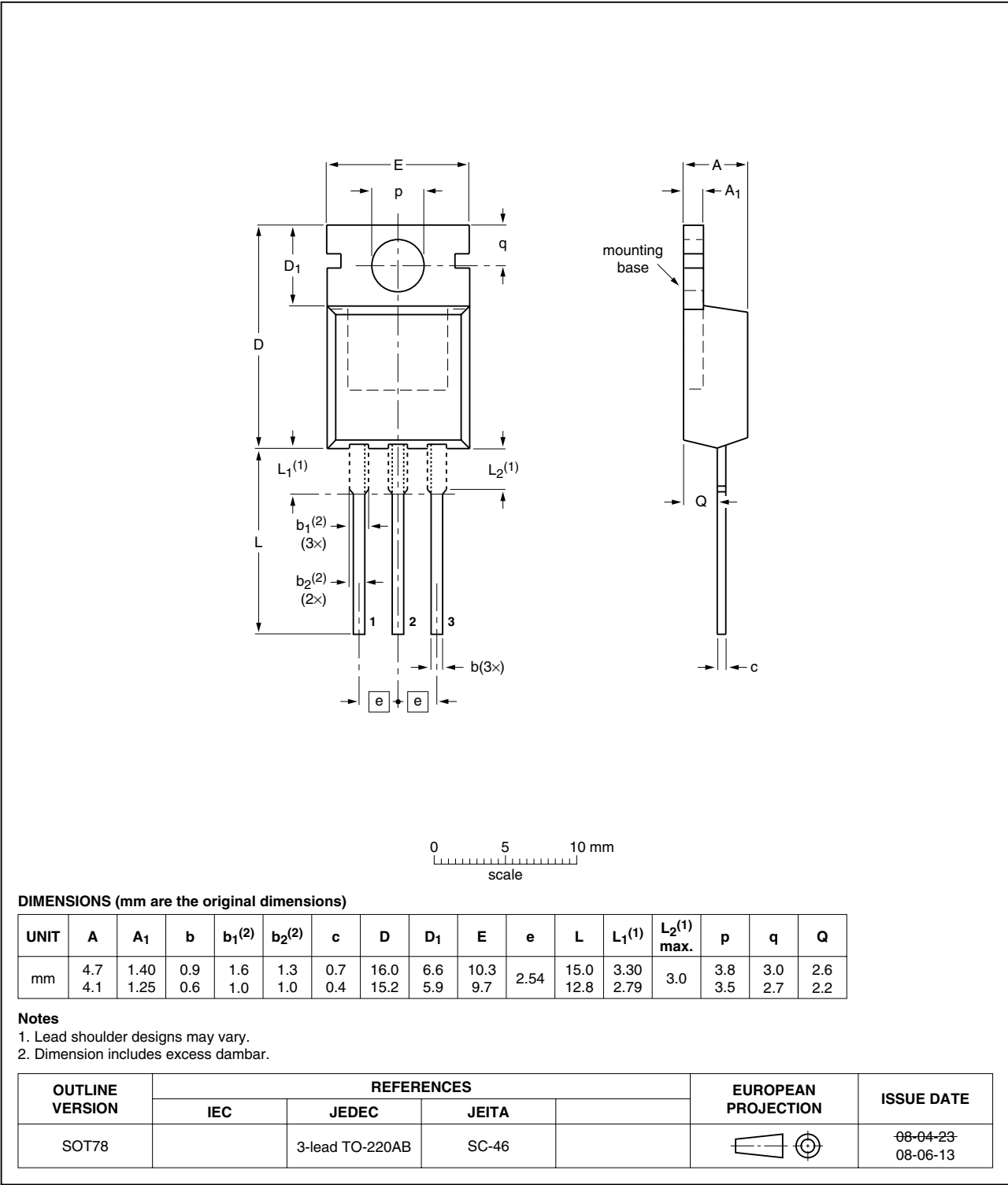


Fig 13. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT151-500L_5	20090302	Product data sheet	-	BT151_SER_L_R_4
Modifications:	• Package outline updated. • Type number BT151-500L separated from data sheet BT151_SER_L_R_4.			
BT151_SER_L_R_4	20061023	Product data sheet	-	BT151_SERIES_3
BT151_SERIES_3 (9397 750 13159)	20040607	Product specification	-	BT151_SERIES_2
BT151_SERIES_2	19990601	Product specification	-	BT151_SERIES_1
BT151_SERIES_1	19970901	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

9.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

10. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

11. Contents

1 Product profile1

1.1 General description1

1.2 Features and benefits1

1.3 Applications1

1.4 Quick reference data1

2 Pinning information2

3 Ordering information2

4 Limiting values3

5 Thermal characteristics5

6 Characteristics6

7 Package outline8

8 Revision history9

9 Legal information10

9.1 Data sheet status10

9.2 Definitions10

9.3 Disclaimers10

9.4 Trademarks10

10 Contact information10



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.