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December 2015

BSS123W

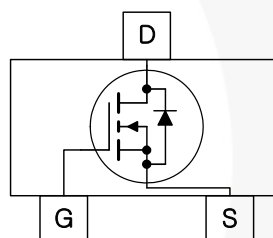
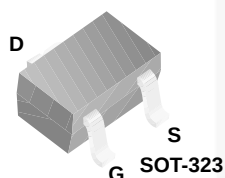
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Features

- 0.17 A, 100 V, $R_{DS(ON)} = 6 \Omega$ at $V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 10 \Omega$ at $V_{GS} = 4.5 \text{ V}$
- High Density Cell Design for Low $R_{DS(ON)}$
- Rugged and Reliable
- Ultra Small Surface Mount Package
- Very Low Capacitance
- Fast Switching Speed
- Lead Free / RoHS Compliant

Description

This N-channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on-state resistance while providing rugged, reliable and fast switching performance. This product is particularly suited for low-voltage, low-current applications such as small servo motor control, power MOSFET gate drivers, logic level transistor, high speed line drivers, power management/power supply and switching applications.



Ordering Information

Part Number	Marking	Package	Packing Method
BSS123W	SA	SOT-323 3L	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-Source Voltage		100	V
V_{DGR}	Drain-Gate Voltage $R_{GS} \leq 20 \text{ k}\Omega$		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	Continuous	0.17	A
		Pulsed	0.68	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	200	mW
	Derate Above 25°C	1.6	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⁽¹⁾	625	$^\circ\text{C/W}$

Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V			10	nA
I _{GSSF}	Gate-Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			50	nA
I _{GSSR}	Gate-Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-50	nA
On Characteristics ⁽²⁾						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 1 mA	0.8	1.7	2.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.17 A		1.39	6	Ω
		V _{GS} = 4.5 V, I _D = 0.17 A		1.48	10	
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 0.17 A	80			mS
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.34 A		0.81	1.30	V
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		71		pF
C _{oss}	Output Capacitance			6.6		pF
C _{rss}	Reverse Transfer Capacitance			2.74		pF
Switching Characteristics ⁽²⁾						
t _r	Turn-On Rise Time	V _{DD} = 30 V, I _D = 0.28 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		1.24	8	ns
t _f	Turn-Off Fall Time			5.73	16	ns
t _{d(on)}	Turn-On Delay			2.94	8	ns
t _{d(off)}	Turn-Off Delay			8.4	13	ns

Note:

2. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2.0\%$.

Typical Performance Characteristics

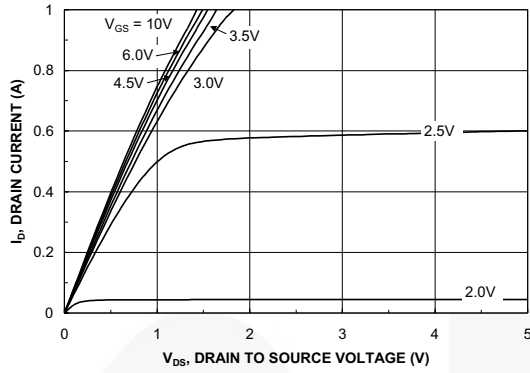


Figure 1. On-Region Characteristics

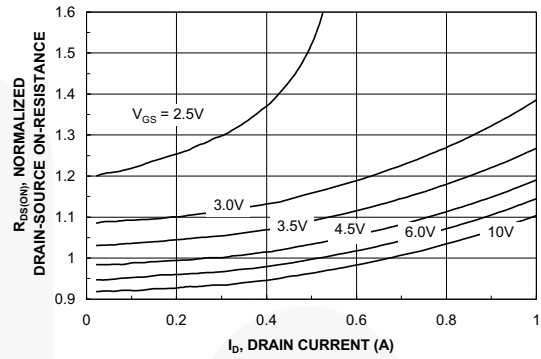


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

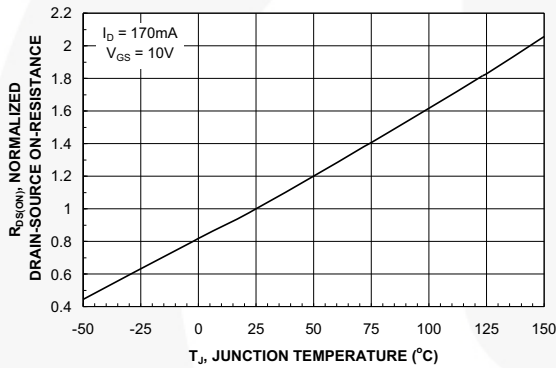


Figure 3. On-Resistance Variation with Temperature

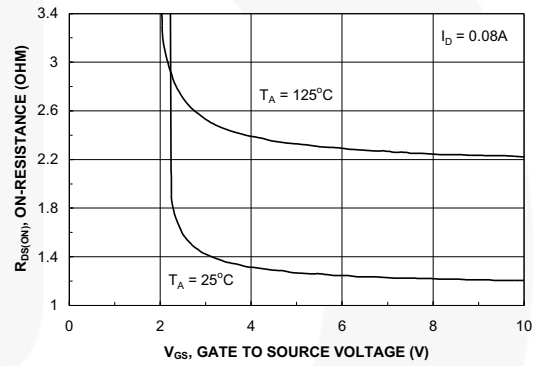


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

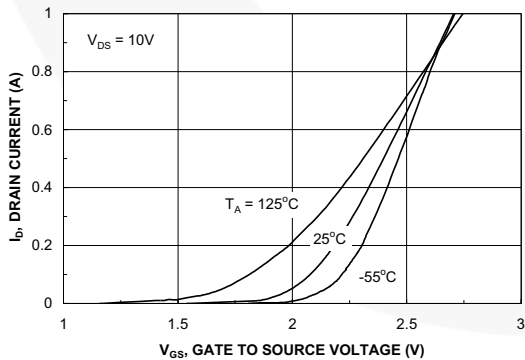


Figure 5. Transfer Characteristics

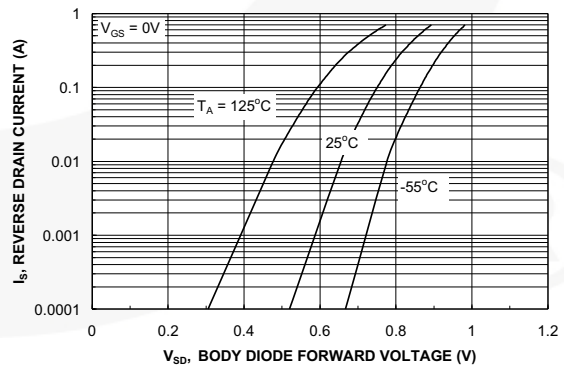


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Performance Characteristics (Continued)

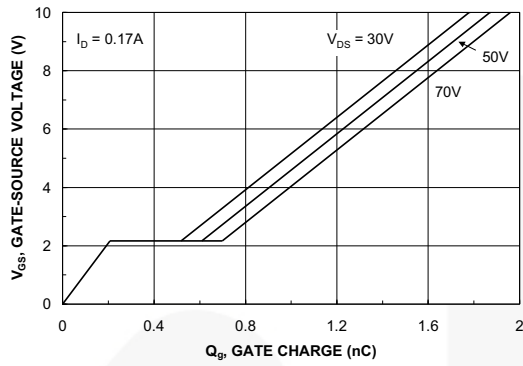


Figure 7. Gate Charge Characteristics

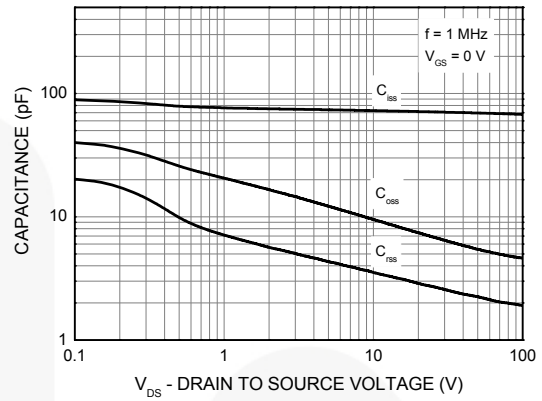


Figure 8. Capacitance



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