bq3050 CEDV Gas Gauge and Battery Pack Manager for 2-Series, 3-Series, and 4-Series Li-Ion Batteries

1 Features

- Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- Advanced Compensated End-of-Discharge Voltage (CEDV) Gauging
- High Side N-CH Protection FET Drive
- Integrated Pre-Charge FET
- Integrated Cell Balancing
- Low Power Modes
  - Low Power: < 180 µA
  - Sleep < 76 µA
- Full Array of Programmable Protection Features
  - Voltage
  - Current
  - Temperature
- Sophisticated Charge Algorithms
  - JEITA
  - Enhanced Charging
  - Adaptive Charging
- Supports Two-Wire SMBus v1.1 Interface
- SHA-1 Authentication
- Compact Package: 38-Lead TSSOP

2 Applications

- Notebook/Netbook PCs
- Medical and Test Equipment
- Portable Instrumentation

3 Description

The Texas Instruments bq3050 Compensated End-of-Discharge Voltage (CEDV) Gas Gauge and Battery Pack Manager is a single-chip solution that provides a rich array of features for protection, authentication, and data gathering for 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq3050 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

The bq3050 provides software-based 1st-level and 2nd-level safety protection for overvoltage, undervoltage, overtemperature, and overcharge conditions, as well as hardware-based protection for overcurrent in discharge and short circuit in charge and discharge conditions.

SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs beyond any doubt.

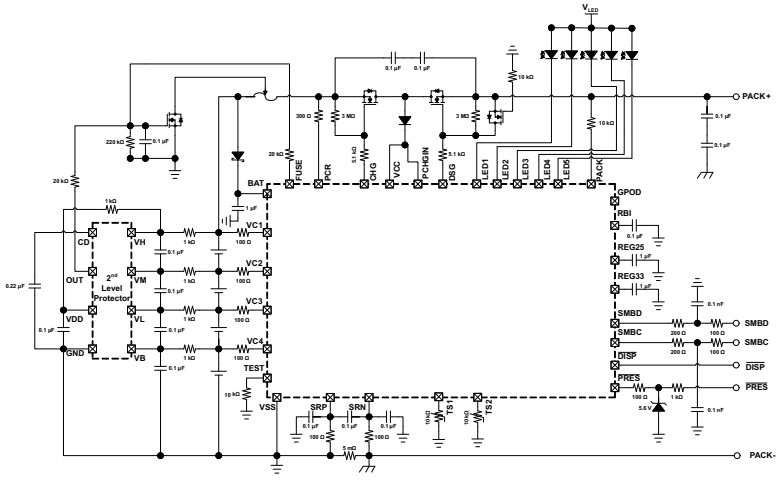
The compact 38-lead TSSOP package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq3050	TSSOP (38)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2014) to Revision D — **Page**

- Added *Community Resources* section ... 1
- Changed SRP, SRN absolute maximum values ... 6
- Changed all occurrences of "bq29412" to "bq294705" ... 25

Changes from Revision B (October 2013) to Revision C — **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted range from Storage temperature description ... 6

Changes from Revision A (June 2011) to Revision B — **Page**

- Changed TEST pin resistor value ... 5

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Changes from Original (January 2011) to Revision A **Page**

- Changed TS2 pin number 4
- Changed Block Diagram 22
- Changed schematic 23

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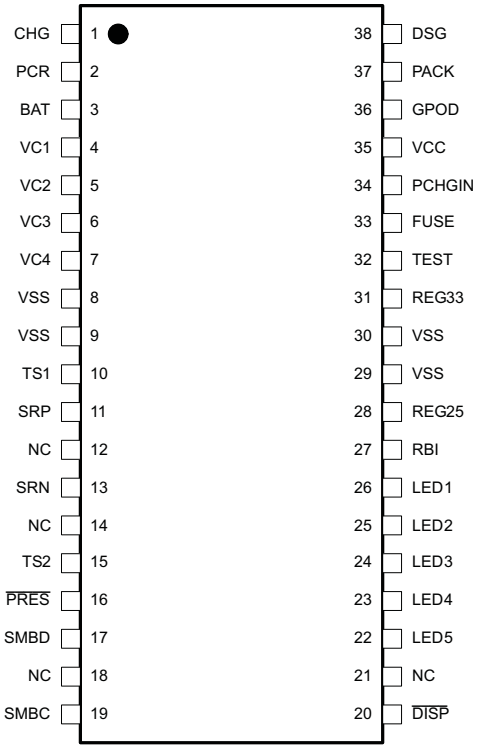
6 Pin Configuration and Functions



Pin Functions

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
CHG	1	O	Charge N-FET gate drive
PCR	2	O	Internal Precharge FET output
BAT	3	P	Alternate power source
VC1	4	I	Sense input for positive voltage of top most cell in stack and cell balancing input for top most cell in stack
VC2	5	I	Sense input for positive voltage of third lowest cell in stack and cell balancing input for third lowest cell in stack
VC3	6	I	Sense input for positive voltage of second lowest cell in stack and cell balancing input for second lowest cell in stack
VC4	7	I	Sense input for positive voltage of lowest cell in stack and cell balancing input for lowest cell in stack
VSS	8	P	Device ground
VSS	9	P	Device ground
TS1	10	AI	Temperature sensor 1 thermistor input
SRP	11	AI	Differential Coulomb Counter input
NC	12	—	Not internally connected. Connect to VSS.
SRN	13	AI	Differential Coulomb Counter input
NC	14	—	Not internally connected. Connect to VSS.
TS2	15	AI	Temperature sensor 2 thermistor input
$\overline{\text{PRES}}$	16	I	Host system present input
SMBD	17	I/OD	SMBus v1.1 data line
NC	18	—	Not internally connected. Connect to VSS.
SMBC	19	I/OD	SMBus v1.1 clock line
$\overline{\text{DISP}}$	20	I	Display active input

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

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Pin Functions (continued)

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
NC	21	—	Not internally connected. Connect to VSS.
LED5	22	O	LED display constant current sink
LED4	23	O	LED display constant current sink
LED3	24	O	LED display constant current sink
LED2	25	O	LED display constant current sink
LED1	26	O	LED display constant current sink
RBI	27	P	RAM backup
REG25	28	P	2.5-V regulator output
VSS	29	P	Device ground
VSS	30	P	Device ground
REG33	31	P	3.3-V regulator output
TEST	32	—	Test pin, connect to VSS through 10-kΩ resistor
FUSE	33	O	Fuse drive
PCHGIN	34	I	Internal Precharge FET input
VCC	35	P	Power supply voltage
GPOD	36	I/OD	High voltage general purpose I/O
PACK	37	P	Alternate power source
DSG	38	O	Discharge N-FET gate drive

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{MAX}	VCC, PCHGIN, PCR, TEST, PACK w.r.t. V_{SS}	–0.3	34	V
Input voltage range, V_{IN}	VC1, BAT	V_{VC2} – 0.3	V_{VC2} + 8.5 V or 34 V, whichever is lower	V
	VC2	V_{VC3} – 0.3	V_{VC3} + 8.5 V	
	VC3	V_{VC4} – 0.3	V_{VC4} + 8.5 V	
	VC4	V_{SRP} – 0.3	V_{SRP} + 8.5 V	
	SRP, SRN	–0.5	0.5	
	LED1, LED2, LED3, LED4, LED5, SMBC, SMBD	V_{SS} – 0.3	6.0	
	$\overline{DISP}$,TS1, TS2, $\overline{PRES}$	–0.3 V	V_{REG25} + 0.3 V	
Output voltage range, V_O	DSG	–0.3	V_{PACK} + 20 V or V_{SS} + 34 V, whichever is lower	V
	CHG	–0.3	V_{BAT} + 20 V or V_{SS} + 34 V, whichever is lower	
	GPOD, FUSE	–0.3	34	
	RBI, REG25	–0.3	2.75	
	REG33	–0.3	5.0	
Maximum VSS current, I_{SS}		50		mA
Current for cell balancing, I_{CB}			10	
ESD Rating	HBM, VCx Only		1	kV
Functional Temperature, T_{FUNC}		–40	110	°C
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage		VCC, PACK, PCHGIN, PCR			25	V
		BAT	3.8		V_{VC2} + 5.0	
$V_{STARTUP}$		Start up voltage at PACK	3.0		5.5	V
V_{IN}	Input voltage range	VC1, BAT	V_{VC2}		V_{VC2} + 5.0	V
		VC2	V_{VC3}		V_{VC3} + 5.0	
		VC3	V_{VC4}		V_{VC4} + 5.0	
		VC4	V_{SRP}		V_{SRP} + 5.0	
		VCn – VC(n+1), (n=1, 2, 3, 4)	0		5.0	
		PACK			25	
		SRP to SRN	–0.2		0.2	
C_{REG33}	External 3.3V REG capacitor		1			µF
C_{REG25}	External 2.5V REG capacitor		1			µF
T_{OPR}	Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC		bq3050 TSSOP (DBT) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	16.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	26.9	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	n/a	

7.5 Supply Current

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal	CHG on, DSG on, no Flash write		410		µA
	Sleep	CHG on, DSG on, no SBS communication		160		
		CHG off, DSG off, no SBS communication		80		
	Shutdown				3.7	

7.6 Power-On Reset (POR)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-}	Negative-going voltage input	At REG25	1.9	2.0	2.1	V
V_{HYS}	POR Hysteresis	At REG25	65	125	165	mV

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7.7 WAKE FROM SLEEP

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE}	V_{WAKE} Threshold	V_{WAKE}	0.2	1.2	2.0	mV
		V_{WAKE}	0.4	2.4	3.6	
		V_{WAKE}	2.0	5.0	6.8	
		V_{WAKE}	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of VWAKE accuracy			0.5%		°C
t_{WAKE}	Time from application of current and wake of bq3050			0.2	1	ms

7.8 RBI RAM Backup

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	VRBI > $V_{(RBI)MIN}$, VCC < VIT		20	1100	nA
		VRBI > $V_{(RBI)MIN}$, VCC < VIT, T_A= 0°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage		1			V

7.9 3.3-V Regulator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG33}	Regulator output voltage	3.8 V < VCC or BAT ≤ 5 V, I_{CC} ≤4 mA	2.4		3.5	V
		5V < VCC or BAT ≤ 6.8 V, I_{CC} ≤13 mA	3.1	3.3	3.5	
		6.8 V < VCC or BAT ≤ 20 V, I_{CC} ≤ 30 mA	3.1	3.3	3.5	
I_{REG33}	Regulator output current		2			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		0.2%		
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		1	13	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		5	18	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, V_{REG33} = 3 V			70	mA
		VCC or BAT = 14.4 V, V_{REG33} = 0 V			33	

7.10 2.5-V Regulator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	I_{REG25} = 10 mA	2.35	2.5	2.55	V
I_{REG25}	Regulator Output Current		3			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		0.25%		
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		1	4	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		20	40	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, V_{REG25} = 2.3 V			65	mA
		VCC or BAT = 14.4 V, V_{REG25} = 0 V			23	

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7.11 $\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC	2.0			V
V_{IL}	Low-level input	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC			0.8	V
V_{OL}	Low-level output voltage	SMBD, SMBC			0.4	V
C_{IN}	Input capacitance	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC		5		pF
I_{LKG}	Input leakage current	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC			1	µA
I_{WPU}	Weak Pull Up Current	$\overline{PRES}$, $V_{OH} = V_{REG25} – 0.5$ V	60		120	µA
$I_{(\overline{DISP})}$	$\overline{DISP}$ source currents	$\overline{DISP}$ active, $\overline{DISP} = V_{REG25} – 0.6$ V	–3			mA
$I_{LKG(\overline{DISP})}$	$\overline{DISP}$ leakage current	$\overline{DISP}$ inactive	–0.22		0.22	µA
$R_{PD(SMBx)}$	SMBC, SMBD Pull-Down	T_A = –40 to 100˚C	550	775	1000	kΩ

7.12 CHG, DSG FET Drive

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{O(FETONDSG)} = V_{(DSG)} – V_{PACK}$, V_{GS} connect 10 MΩ, VCC 3.8 V to 8.4 V	8.0	9.7	12	V
		$V_{O(FETONDSG)} = V_{(DSG)} – V_{PACK}$, V_{GS} connect 10 MΩ, VCC > 8.4 V	9.0	11	12	
		$V_{O(FETONCHG)} = V_{(CHG)} – V_{BAT}$, V_{GS} connect 10 MΩ, VCC 3.8 V to 8.4 V	8.0	9.7	12	
		$V_{O(FETONCHG)} = V_{(CHG)} – V_{BAT}$, V_{GS} connect 10 MΩ, VCC > 8.4 V	9.0	11	12	
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$VO_{(FETOFFDSG)} = V_{(DSG)} – V_{PACK}$	–0.4		0.4	V
		$V_{O(FETOFFCHG)} = V_{(CHG)} – V_{BAT}$	–0.4		0.4	
t_r	Rise time	C_L= 4700 pF R_G= 5.1 kΩ VCC < 8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V V_{CHG}: V_{PACK} to V_{PACK} + 4 V		800	1400	µs
		C_L = 4700 pF R_G = 5.1 kΩ VCC > 8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V V_{CHG}: V_{PACK} to V_{PACK} + 4 V		200	500	
t_f	Fall time	C_L = 4700 pF R_G = 5.1 kΩ V_{DSG}: V_{BAT} + $V_{O(FETONDSG)}$ to V_{BAT} + 1 V V_{CHG}: V_{PACK} + $V_{O(FETONCHG)}$ to V_{PACK} + 1 V		80	200	µs

7.13 Internal Precharge Limiting

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PCHGMAX}$	Maximum Precharge current	3-cell and 4-cell configuration			100	mA
R_{PCHG_RDSON}	Internal Precharge FET RDSON	$V_{DS(PRECHG)}$ ≥ 1 V, VCC < 8.4 V	30	55	85	Ω
		$V_{DS(PRECHG)}$ ≥ 1 V, VCC ≥ 8.4 V	15	30	55	

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7.14 GPOD

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PU_GPOD}	GPOD Pull-Up Voltage				V_{CC}	V
V_{OL_GPOD}	GPOD Output Voltage Low	I_{OL} = 1 mA	0.3			V

7.15 FUSE

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(FUSE)}$	High Level FUSE Output	VCC = 3.8 V to 9 V	2.4		8.5	V
		VCC = 9 V to 25 V	7	8	9	
$V_{IH(FUSE)}$	Weak pull-up current in off state (1)		2.8			V
				100		nA
$t_{R(FUSE)}$	FUSE Output Rise Time	C_L = 1 nF, VCC = 9 V to 25 V, $V_{OH(FUSE)}$ = 0 V to 5 V		5	20	µs
$Z_{O(FUSE)}$	FUSE Output Impedance			2	5	kΩ

(1) Verified by design. Not production tested.

7.16 LED5, LED4, LED3, LED2, LED1

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
I_{OL}	Low-level output current	VOL = 0.4 V, 3 mA setting	2.5	3.5	4.5	mA
		VOL = 0.4 V, 4 mA setting	3.0	4.5	6.0	
		VOL = 0.4 V, 5 mA setting	3.5	5.5	7.5	
I_{LEDx}	Current matching between LEDx			0.1		mA

7.17 Coulomb Counter

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	SRP – SRN	–0.20		0.25	V
Conversion time	Single conversion		250		ms
Resolution (no missing codes)		16			Bits
Effective resolution	Single conversion, signed	15			Bits
Offset error	Post calibrated		10		µV
Offset error drift			0.3	0.5	µV/°C
Full-scale error		–0.8%	0.2%	0.8%	
Full-scale error drift				150	PPM/°C
Effective input resistance		2.5			mΩ

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7.18 VC1, VC2, VC3, VC4

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	–0.20		8	V
	Conversion time	Single conversion		32		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution	Single conversion, signed	15			Bits
$R_{(BAL)}$	$R_{DS(ON)}$ for internal FET at V_{DS} > 2 V	V_{DS} = VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	200	310	430	Ω
	$R_{DS(ON)}$ for internal FET at V_{DS} > 4 V	V_{DS} = VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	60	125	230	

7.19 TS1, TS2

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Internal Pull Up Resistor		16.5	17.5	19.0	KΩ
R_{DRIFT}	Internal Pull Up Resistor Drift From 25°C				200	PPM/°C
R_{PAD}	Internal Pin Pad resistance			84		Ω
V_{IN}	Input voltage range	TS1 – VSS, TS2 – VSS	–0.20		0.8 × V_{REG25}	V
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

7.20 Internal Temperature Sensor

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage		–1.9	–2.0	–2.1	mV/°C
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

7.21 Internal Thermal Shutdown

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX1}	Maximum PCHG temperature		110		150	°C
T_{MAX2}	Maximum REG33 temperature		125		175	°C
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C
$t_{PROTECT}$	Protection time			5		µs

7.22 High Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU Clock			4.194		MHz

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High Frequency Oscillator (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(EIO)}$	Frequency error(1)(2)	T_A = –20°C to 70°C	–2%	±0.25%	2%	
		T_A = –40°C to 85°C	–3%	±0.25%	3%	
$t_{(SXO)}$	Start-up time(3)	T_A = –25°C to 85°C		3	6	ms

(1) The frequency error is measured from 4.194 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5 V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% when the device is already powered.

7.23 Low Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(1)(2)	T_A = –20°C to 70°C	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time(3)	T_A = –25°C to 85°C			100	µs

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

7.24 Internal Voltage Reference

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal Reference Voltage		1.215	1.225	1.230	V
V_{REF_DRIFT}	Internal Reference Voltage Drift	T_A = –25°C to 85°C		±80		PPM/°C
		T_A = 0°C to 60°C		±50		

7.25 Flash

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Year
	Flash programming write-cycles	Data Flash	20k			Cycle
		Instruction Flash	1k			
$I_{CC(PROG_DF)}$	Data Flash-write supply current	T_A = –40°C to 85°C		3	4	mA
$I_{CC(ERASE_DF)}$	Data Flash-erase supply current	T_A = –40°C to 85°C		3	18	mA

(1) Verified by design. Not production tested.

7.26 OCD Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OCD detection threshold voltage range, typical	RSNS = 0	50		200	mV
		RSNS = 1	25		100	
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	RSNS = 0		10		mV
		RSNS = 1		5		
$V_{(OFFSET)}$	OCD offset		–10		10	mV

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OCD Current Protection (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(Scale_Err)}$	OCD scale error		–10%		10%	
$t_{(OCDD)}$	Over Current in Discharge Delay		1		31	ms
$t_{(OCDD_STEP)}$	OCDD Step options			2		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20%		20%	

7.27 SCD1 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC1)}$	SCD1 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	
$\Delta V_{(SCD1T)}$	SCD1 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		
$V_{(OFFSET)}$	SCD1 offset		–10		10	mV
$V_{(Scale_Err)}$	SCD1 scale error		–10%		10%	
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		915	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		1830	
$t_{(SCD1D_STEP)}$	SCD1D Step options	AFE.STATE_CNTL[SCDDx2] = 0		61		µs
		AFE.STATE_CNTL[SCDDx2] = 1		122		
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20%		20%	

7.28 SCD2 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC2)}$	SCD2 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	
$\Delta V_{(SCD2T)}$	SCD2 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		
$V_{(OFFSET)}$	SCD2 offset		–10		10	mV
$V_{(Scale_Err)}$	SCD2 scale error		–10%		10%	
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		458	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		915	
$t_{(SCD2D_STEP)}$	SCD2D Step options	AFE.STATE_CNTL[SCDDx2] = 0		30.5		µs
		AFE.STATE_CNTL[SCDDx2] = 1		61		
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20%		20%	

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7.29 SCC Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0	–100		–300	mV
		RSNS = 1	–50		–225	
$\Delta V_{(SCCDT)}$	SCC detection threshold voltage program step	RSNS = 0		–50		mV
		RSNS = 1		–25		
$V_{(OFFSET)}$	SCC offset		–10		10	mV
$V_{(Scale_Err)}$	SCC scale error		–10%		10%	
$t_{(SCCD)}$	Short Circuit in Charge Delay		0		915	ms
$t_{(SCCD_STEP)}$	SCCD Step options			61		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20%		20%	

7.30 SBS Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4.0			µs
$t_{HD:DAT}$	Data hold time		300			ns
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal/detect	See (1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See (2)			Disabled	
t_{HIGH}	Clock high period	See (2)	4.0		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See (4)			10	ms
t_F	Clock/data fall time	See (5)			300	ns
t_R	Clock/data rise time	See (6)			1000	ns

(1) The bq3050 times out when any clock low exceeds $t_{TIMEOUT}$.
(2) t_{HIGH}, Max, is the minimum bus idle time. SMBC = 1 for t > 50 µs causes reset of any transaction involving bq3050 that is in progress. This specification is valid when the THIGH_VAL=0. If THIGH_VAL = 1, then the value of THIGH is set by THIGH_1,2 and the timeout is not SMBus standard.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time tR = V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15)
(6) Fall time tF = 0.9 V_{DD} to (V_{ILMAX} – 0.15)

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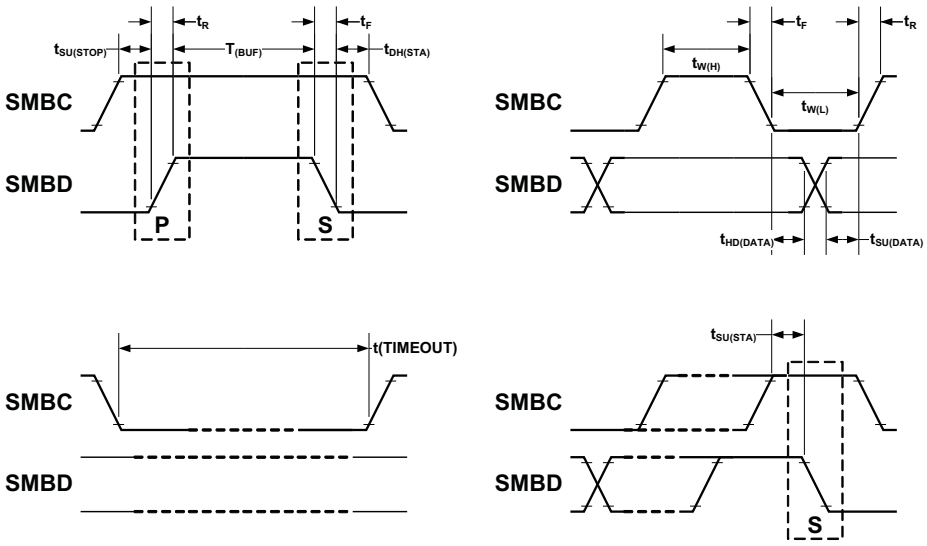

Figure 1. SMBus Timing Diagram

7.31 Typical Characteristics

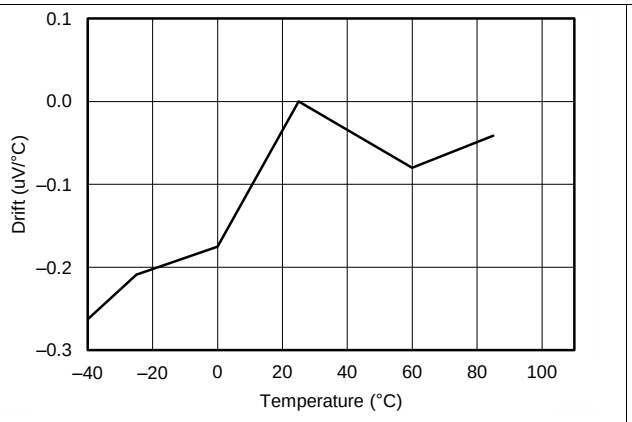

Figure 2. CC Input Offset Drift Overtemperature

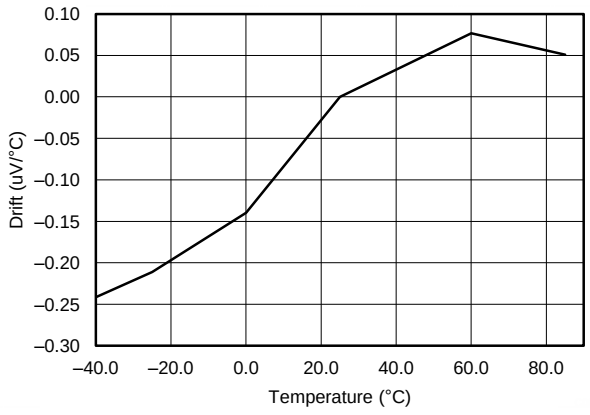

Figure 3. ADC Input Offset Drift Overtemperature

8 Detailed Description

8.1 Overview

The bq3050 measures the voltage, temperature, and current to determine battery capacity and state-of-charge (SOC). The bq3050 monitors charge and discharge activity by sensing the voltage across a small value resistor (5 mΩ to 20 mΩ, typical) between the SRP and SRN pins and in series with the battery. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge. Measurements of OCV and charge integration determine chemical SOC.

The Qmax values are taken from a cell manufacturers' data sheet multiplied by the number of parallel cells, and is also used for the value in ***Design Capacity***. It uses the OCV and Qmax value to determine *StateOfCharge()* on battery insertion, device reset, or on command. The *FullChargeCapacity()* is reported as the learned capacity available from full charge until *Voltage()* reaches the EDV0 threshold. As *Voltage()* falls below the ***Shutdown Voltage*** for ***Shutdown Time*** and has been out of SHUTDOWN mode for at least ***Shutdown Time***, the *PF Flags1 () [VSHUT]* bit is set. For additional details, see *bq3050 Technical Reference Manual* (SLUU485).

Fuel gauging is derived from the Compensated End of Discharge Voltage (CEDV) method, which uses a mathematical model to correlate remaining state of charge (RSOC) and voltage near to the end of discharge state. This requires a full-discharge cycle for a single-point FCC update. The implementation models cell voltage (OCV) as a function of battery SOC, temperature, and current. The impedance is also a function of SOC and temperature, which can be satisfied by using seven parameters: EMF, C0, R0, T0, R1, TC, and C1.

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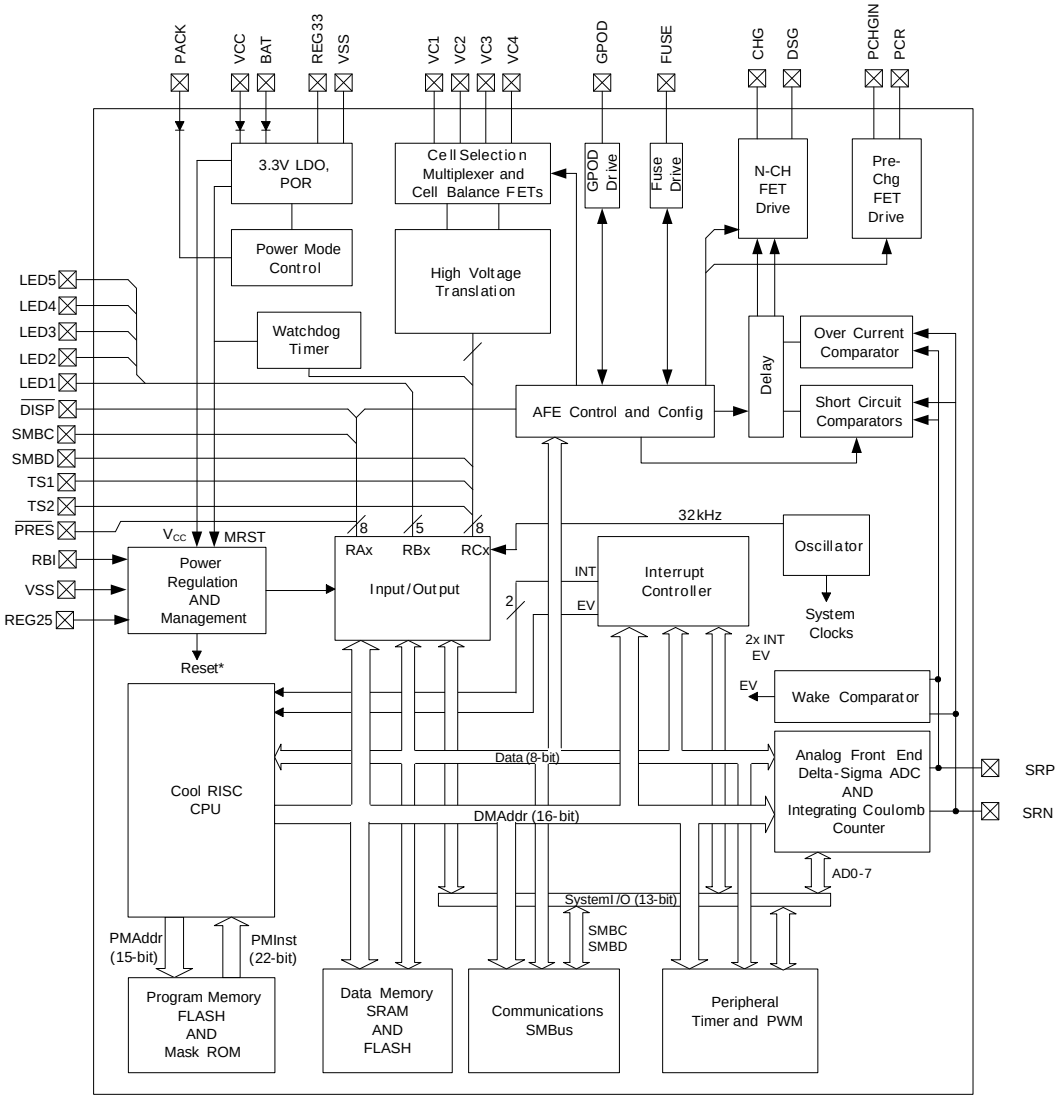
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Primary (1st Level) Safety Features

The bq3050 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell Overvoltage/Undervoltage Protection
- Charge and Discharge Overcurrent
- Short-Circuit
- Charge and Discharge Over-Temperature
- AFE Watchdog

8.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq3050 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety Overvoltage

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Feature Description (continued)

- Safety Overcurrent in Charge and Discharge
- Safety Overtemperature in Charge and Discharge
- Charge FET, Discharge FET, and Precharge FET Faults
- Cell Imbalance Detection
- Fuse Blow by Secondary Voltage Protection IC
- AFE Register Integrity Fault (AFE_P)
- AFE Communication Fault (AFE_C)

8.3.3 Charge Control Features

The bq3050 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms

8.3.4 Gas Gauging

The bq3050 uses the CEDV algorithm to measure and calculate the available capacity in battery cells. The bq3050 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq3050 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. See the *bq3050 Technical Reference Manual* (SLUU485) for further details.

8.3.5 Lifetime Data Logging Features

The bq3050 offers limited lifetime data logging for the following critical battery parameters:

- Lifetime Maximum Temperature
- Lifetime Minimum Temperature
- Lifetime Maximum Battery Cell Voltage
- Lifetime Minimum Battery Cell Voltage

8.3.6 Authentication

- The bq3050 supports authentication by the host using SHA-1.
- SHA-1 authentication by the gas gauge is required for unsealing and full access.

8.4 Device Functional Modes

The bq3050 supports three power modes to reduce power consumption:

- In NORMAL Mode, the bq3050 performs measurements, calculations, protection decisions, and data updates in 0.25-s intervals. Between these intervals, the bq3050 is in a reduced power stage.
- In SLEEP Mode, the bq3050 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq3050 is in a reduced power stage. The bq3050 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In SHUTDOWN Mode, the bq3050 is completely disabled.

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8.5 Configuration

8.5.1 Oscillator Function

The bq3050 fully integrates the system oscillators and does not require any external components to support this feature.

8.5.2 System Present Operation

The bq3050 checks the $\overline{\text{PRES}}$ pin periodically (1 s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq3050 detects this as system present.

8.5.3 2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

8.5.4 Cell Balancing

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

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Configuration (continued)

8.5.4.1 Internal Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by the external resistor R_{VC} at the VCx input. See Figure 4.

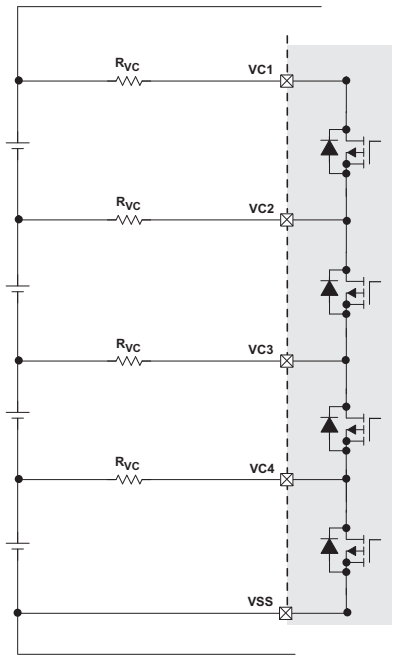

Figure 4. Internal Cell Balancing with R_{VC}

8.5.4.2 External Cell Balancing

When external cell balancing is configured, the cell balance current is defined by R_B. See Figure 5. Only one cell at a time can be balanced.

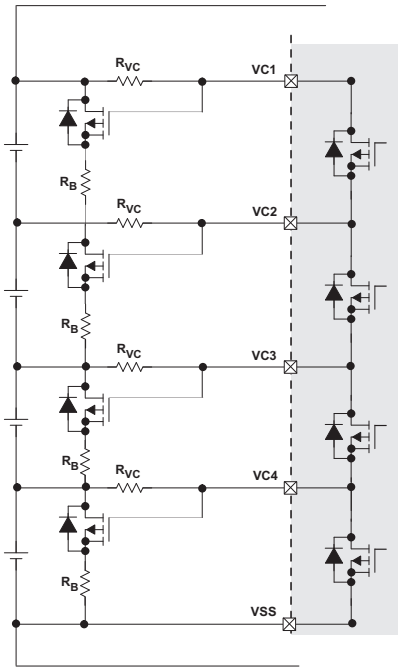

Figure 5. External Cell Balancing with R_B

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8.6 Battery Parameter Measurements

8.6.1 Charge and Discharge Counting

The bq3050 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq3050 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq3050 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

8.6.2 Voltage

The bq3050 updates the individual series cell voltages at 0.25-second intervals. The internal ADC of the bq3050 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the CEDV gas-gauging.

8.6.3 Current

The bq3050 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typ. sense resistor.

8.6.4 Auto Calibration

The bq3050 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq3050 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

8.6.5 Temperature

The bq3050 has an internal temperature sensor and inputs for two external temperature sensors. All three temperature sensor options are individually enabled and configured for cell or FET temperature. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which may be of a higher temperature type.

8.6.6 Communications

The bq3050 uses SMBus v1.1 with Master Mode and packet error checking (PEC) options per the SBS specification.

8.6.6.1 SMBus On and Off State

The bq3050 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

8.6.6.2 SBS Commands

See the *bq3050 Technical Reference Manual* (SLUU485) for further details.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq3050 gas gauge is a primary protection device that can be used with a 2-series, 3-series or 4-series Li-Ion/Li Polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, the user needs the bqEVSW tool, which is a graphical user-interface tool installed on a PC during development. The firmware installed in the product has default values, which are summarized in the *bq3050 Technical Reference Manual* (SLUU485). Using the bqEVSW tool, these default values can be changed to cater to specific application requirements during development once the system parameters are known, such as fault-trigger thresholds for protection, enable or disable certain features for operation, configuration of cells, and more.

9.2 Typical Applications

In a typical application, the bq3050 is typically paired with a 2nd-level overvoltage protection device to provide an independent level of voltage protection.

The bq3050 is often used to provide a visual display using the LED Display feature, but this is optional.

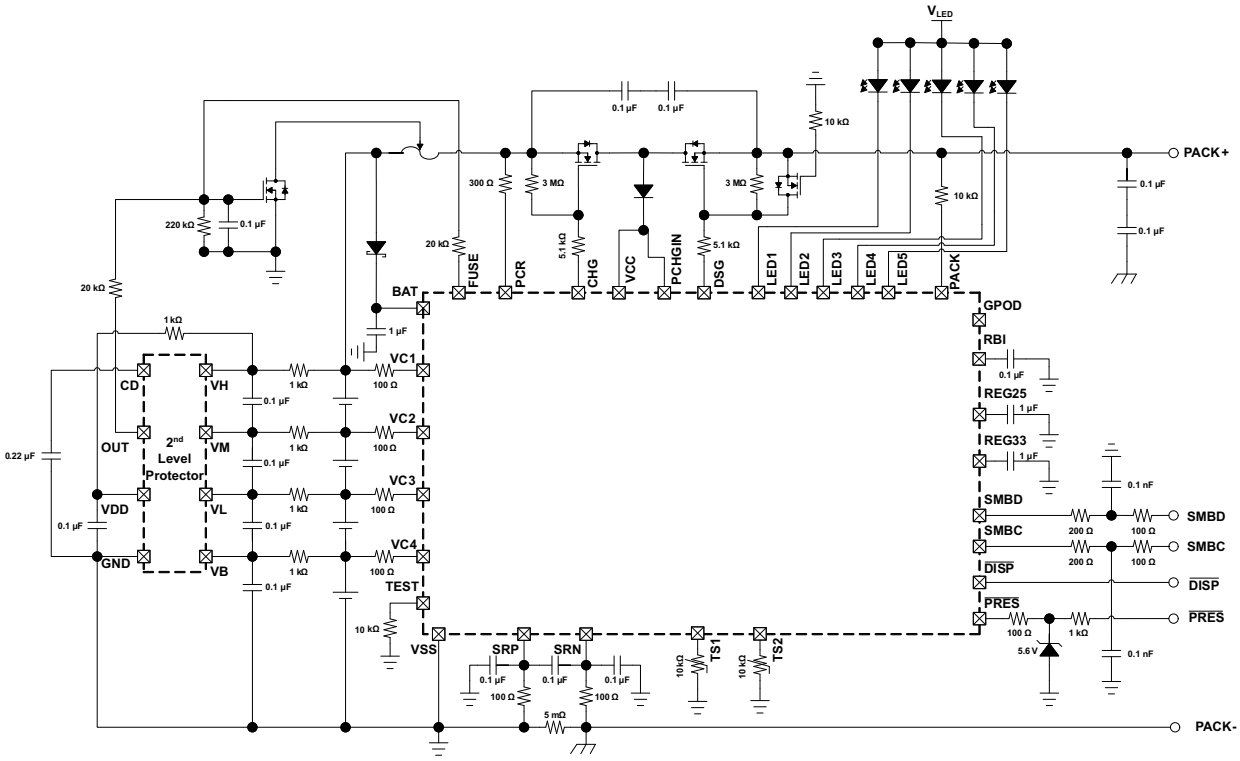

Figure 6. bq3050 Implementation

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Typical Applications (continued)

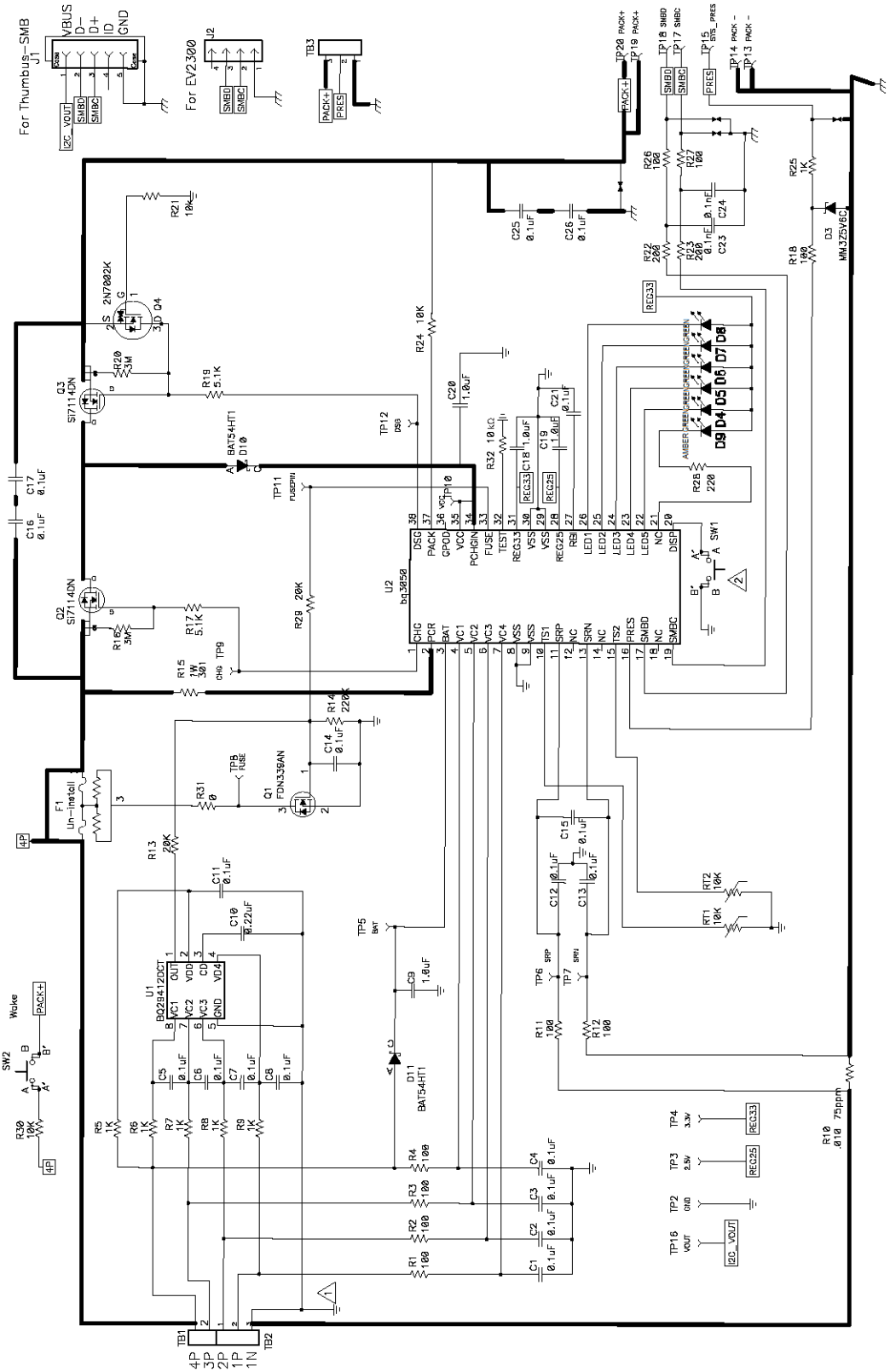

Figure 7. Application Schematic

Typical Applications (continued)

9.2.1 Design Requirements

For the bq3050 design example, use the parameters in Table 1 as input parameters.

Table 1. Requirements

DESIGN PARAMETER	VALUE OR STATE
Cell Configuration	3s2p (4-series with 1 Parallel)
Design Capacity	4400 mAh
Device Chemistry	Chem ID 100 (LiCoO2/graphitized carbon)
Cell Overvoltage (per cell)	4500 mV
Cell Undervoltage (per cell)	2200 mV
1st Tier Overcurrent in CHARGE Mode	6000 mA
1st Tier Overcurrent in DISCHARGE Mode	–6000 mA
AFE Overcurrent in CHARGE Mode	0.120 V/Rsense across SRP, SRN
AFE Short Circuit in DISCHARGE Mode	0.450 V/Rsense across SRP, SRN
AFE Short Circuit in CHARGE Mode	0.250V/Rsense across SRP, SRN
Overtemperature in CHARGE Mode	55°C
Overtemperature in DISCHARGE Mode	60°C
SAFE Pin Activation Enabled	No
Safety Overvoltage (per cell)	4600 mV
Shutdown Voltage	5250 mV
Cell Balancing Enabled	Yes
Internal or External Temperature Sensor	External Enabled
SMB BROADCAST Mode	Disabled
Display Mode (Number of LEDs)	5-bar
PRES Feature Enabled	No

9.2.2 Detailed Design Procedure

9.2.2.1 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal (see). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

9.2.2.1.1 Protection FETs

The N-channel charge and discharge FETs must be selected for a given application (Figure 8). Most portable battery applications are a good match for the CSD17308Q3. The TI CSD17308Q3 is an 47A-A, 30-V device with Rds(on) of 8.2 mΩ when the gate drive voltage is 10 V.

If a precharge FET is used, R15 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to $(V_{charger} – V_{bat})/R15$ and maximum power dissipation is $(V_{charger} – V_{bat})^2/R15$.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C16 and C17 help protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. In order to have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C16 and C17 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

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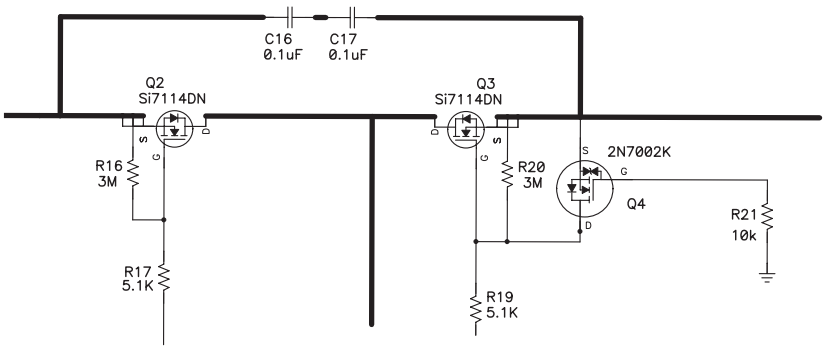

Figure 8. bq3050 Protection FETs

9.2.2.1.2 Chemical Fuse

The chemical fuse (Sony Chemical, Uchihashi, and so forth) is ignited under command from either the bq294705 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either event applies a positive voltage to the gate of Q1, shown in Figure 9, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in *FUSE Circuitry*.

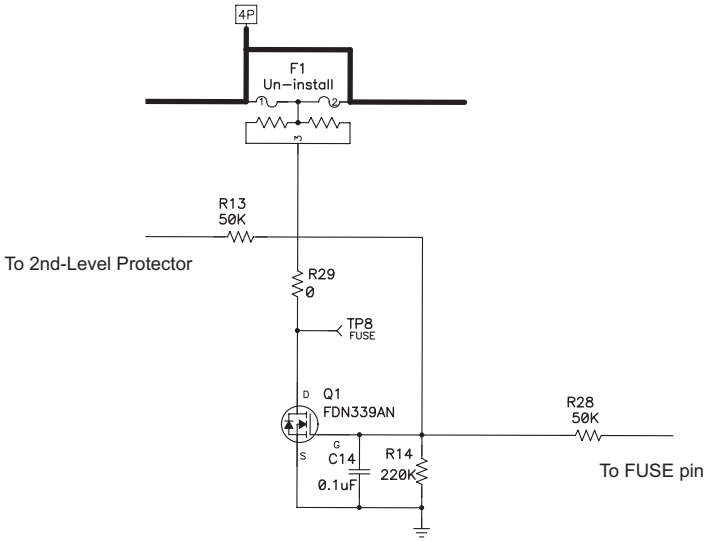

Figure 9. FUSE Circuit

9.2.2.1.3 Lithium-Ion Cell Connections

The important thing to remember about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in Figure 10 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important. The VC5 pin (a ground reference for cell voltage measurement), which is in the older generation devices, is not in the bq3050 device. Hence, the single-point connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

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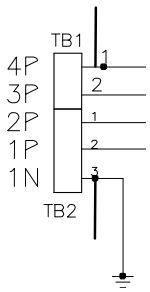

Figure 10. Lithium-Ion Cell Connections

9.2.2.1.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 75 ppm in order to minimize current measurement drift with temperature (Figure 11). Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq3050. Select the smallest value possible in order to minimize the negative voltage generated on the bq3050 V_{SS} node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. For a pack with two parallel cylindrical cells, 10 mΩ is generally ideal. Parallel resistors can be used as long as good Kelvin sensing is ensured.

The ground scheme of bq3050 is different from the older generation devices. In previous devices, the device ground (or low-current ground) is connected to the SRN side of the Rsense resistor pad. The bq3050, however, connects the low-current ground on the SRP side of the Rsense resistor pad, close to the battery 1N terminal (see *Lithium-Ion Cell Connections*). This is because the bq3050 has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.



Figure 11. Sense Resistor

9.2.2.1.5 ESD Mitigation

A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a tranzorb, such as the SMBJ2A, can be placed across the terminals to further improve ESD immunity.

9.2.2.2 Gas Gauge Circuit

The Gas Gauge Circuit includes the bq3050 and its peripheral components. These components are divided into the following groups: Differential Low-Pass Filter, Power Supply Decoupling/RBI, System Present, SMBus Communication, FUSE circuit, and LED.

9.2.2.2.1 Differential Low-Pass Filter

As shown in Figure 12, a differential filter must precede the current sense inputs of the gas gauge. This filter eliminates the effect of unwanted digital noise, which can cause offset in the measured current. Even the best differential amplifier has less common-mode rejection at high frequencies. Without a filter, the amplifier input stage may rectify a strong RF signal, which then may appear as a dc offset error.

Five percent tolerance of the components is adequate because capacitor C15 shunts C12/C13, and reduces AC common mode arising from component mismatch. It is also proven to reduce offset and noise error by maintaining µa symmetrical placement pattern and adding ground shielding for the differential filter network.

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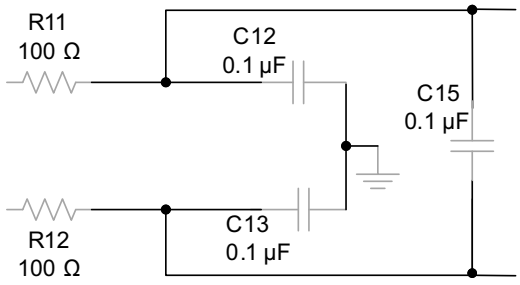

Figure 12. Differential Low-Pass Filter

9.2.2.2.2 Power Supply Decoupling and RBI

Power supply decoupling is important for optimal operation of the bq3050 advanced gas gauges. As shown in , a single 1.0-µF ceramic decoupling capacitor from REG33 to V_{SS} and REG25 to V_{SS} must be placed adjacent to the IC pins.

The RBI pin is used to supply backup RAM voltage during brief transient power outages. The partial reset mechanism makes use of the RAM to restore the critical CPU registers following a temporary loss of power. A standard 0.1-µF ceramic capacitor is connected from the RBI pin to ground, as shown in Figure 13.

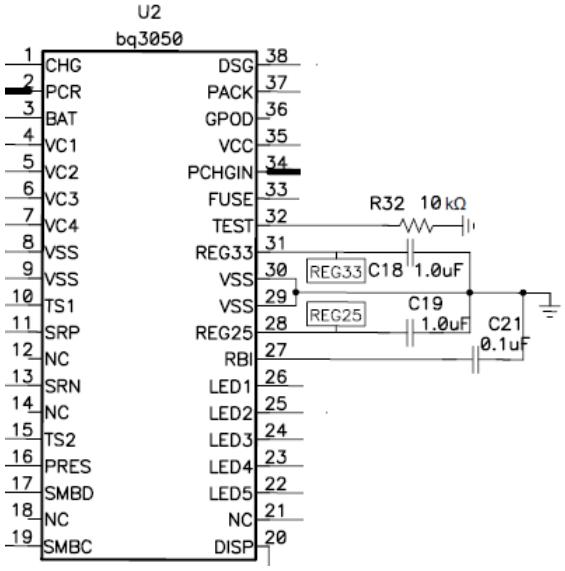

Figure 13. Power Supply Decoupling

9.2.2.2.3 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The PRES pin of the bq3050 is occasionally sampled to test for system present. To save power, an internal pullup resistor is provided by the gas gauge during a brief 4-µs sampling pulse once per second.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the PRES device pin reduces the external protection requirement to just R25 for an 8-kV ESD contact rating (Figure 14). However, if it is possible that the System Present signal may short to PACK+, then R18 and D3 must be included for high-voltage protection.

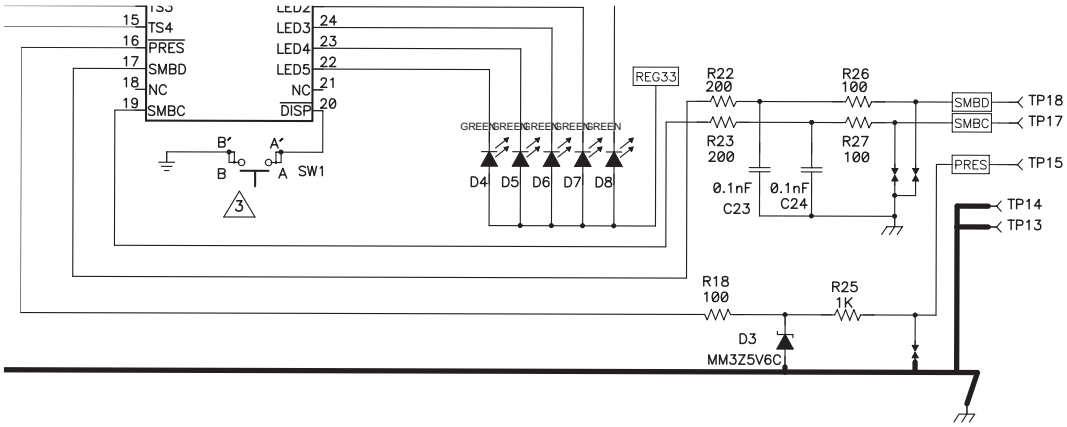

Figure 14. System Present ESD and Short Protection

9.2.2.2.4 SMBus Communication

Similar to the System Present pin, the SMBus clock and data pins have integrated high-voltage ESD protection circuits that reduce the need for external Zener diode protection. When using the circuit shown in Figure 15, the communication lines can withstand an 8-kV (contact) ESD strike. C23 and C24 are selected with a 100-pF value in order to meet the SMBus specifications. If it is desirable to provide increased protection with a larger input resistor and/or Zener diode, carefully investigate the signal quality of the SMBus signals under worst-case communication conditions.

The SMbus clock and data lines have internal pulldowns. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into sleep mode to conserve power.

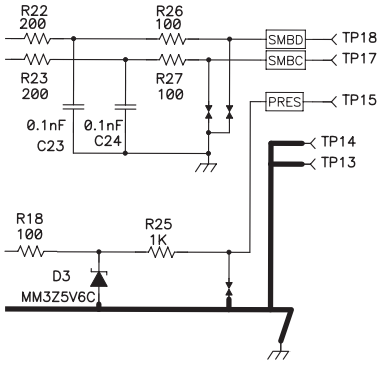

Figure 15. ESD Protection for SMB Communication

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9.2.2.2.5 FUSE Circuitry

The FUSE pin of the bq3050 is designed to ignite the chemical fuse if one of the various safety criteria is violated (Figure 16). The FUSE pin also monitors the state of the secondary-voltage protection IC. Q3 ignites the chemical fuse when its gate is high. The 7-V output of the bq29705 is divided by R13 and R14, which provides adequate gate drive for Q1 while guarding against excessive back current into the bq29705 if the FUSE signal is high.

Using C14 is generally a good practice, especially for RFI immunity. C14 may be removed, if desired, because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that may come from the SAFE output during the cell connection process.

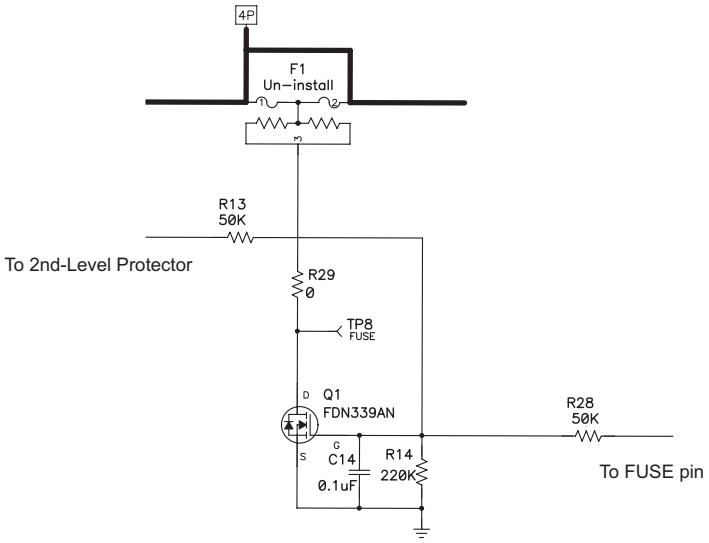

Figure 16. FUSE Circuit

When the bq3050 is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output. The new design makes it possible to use a higher Vgs FET for Q1. This improves the robustness of the system, as well as widens the choices for Q1.

9.2.2.2.6 PFIN Detection

As previously mentioned, the FUSE pin has a dual role on this device. When bq3050 is not commanded to ignite the chemical fuse, the FUSE pin defaults to sense the OUT pin status of the secondary voltage protector. When the secondary voltage protector ignites the chemical fuse, the high voltage is sensed by the FUSE pin, and the bq3050 sets the PFIN flag accordingly.

9.2.2.3 Secondary-Current Protection

The bq3050 provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following sections examine Cell and Battery Inputs, Pack and FET Control, Regulator Output, Temperature Output, and Cell Balancing.

9.2.2.3.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

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The internal cell balancing FETs in bq3050 provide about typically 310 Ω (310 Ω with cell voltage ≥ 2 V. The cell balancing FETs Rds-on reduced to typically 125 Ω with cell voltage ≥ 4 V), which can be used to bypass charge current in individual cells that may be overcharged with respect to the others (Figure 17). The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the bypass current value. The bq3050 device is designed to take up to 10-mA cell balancing current. Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing.

The BAT input uses a diode (D1) and 1-µF ceramic capacitor (C9) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described previously in *High-Current Path*, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

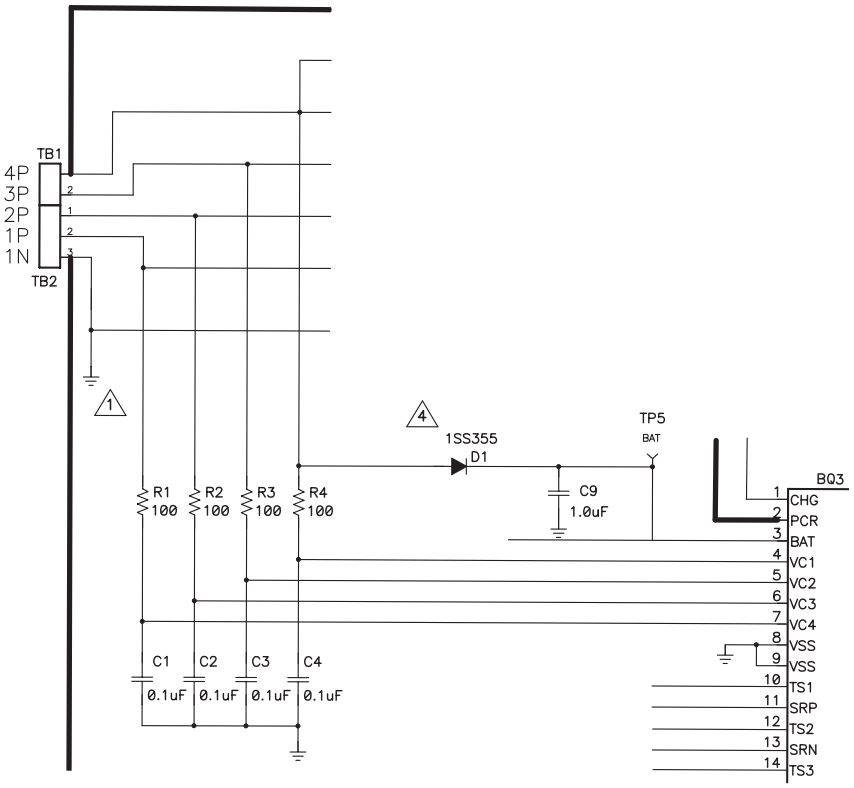

Figure 17. Cell and BAT Inputs

9.2.2.3.2 External Cell Balancing

Internal cell balancing can only support up to 10 mA. External cell balancing provides another option for faster cell balancing. For details, refer to the application note, *Fast Cell Balancing Using External MOSFET* (SLUA420).

9.2.2.3.3 PACK and FET Control

The PACK and V_{CC} inputs provide power to the bq305x from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 10-KΩ resistor, whereas the V_{CC} input uses a diode to guard against input transients and prevents malfunction of the date driver during short-circuit events (Figure 18).

The N-channel charge and discharge FETs are controlled with 5.1-KΩ series gate resistors, which provide a switching time constant of a few microseconds. The 3.01-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative.

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Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7000 as the reference schematic, the gate should be biased up to 3.3 V with a high-value resistor. The bq3050 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The pre-charge FET is integrated into the bq3050 device, allowing users to only connect an external pre-charge load resistor via the PCR pin through the PCHGIN input. The bq3050 device supports up to 100-mA of pre-charge current. When selecting the external load resistor, user should take into account the max charger voltage and the Rdson of the internal pre-charge FET.

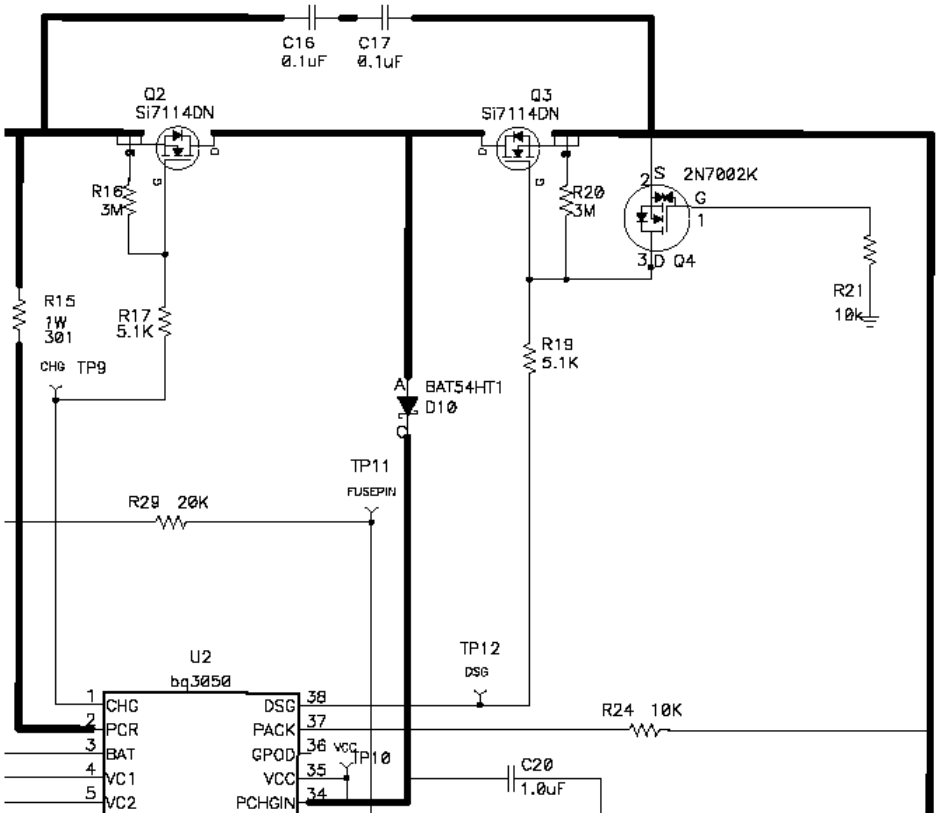

Figure 18. bq3050 PACK and FET Control

9.2.2.3.4 Regulator Output

As mentioned in *Power Supply Decoupling and RBI*, the two low-dropout regulators in the bq3050 require capacitive compensation on the output. The outputs must have a 1-µF ceramic capacitor placed close to the IC terminal pins.

9.2.2.3.5 Temperature Output

For the bq3050 device, TS1 and TS2 provide thermistor drive-under program control (Figure 19). Each pin can be enabled with an integrated 18-kΩ (typical) linearization pullup resistor to support the use of a 10-kΩ at 25°C (103) NTC external thermistor, such as a Mitsubishi BN35-3H103. The reference design includes two 10-kΩ thermistors: RT1 and RT2.

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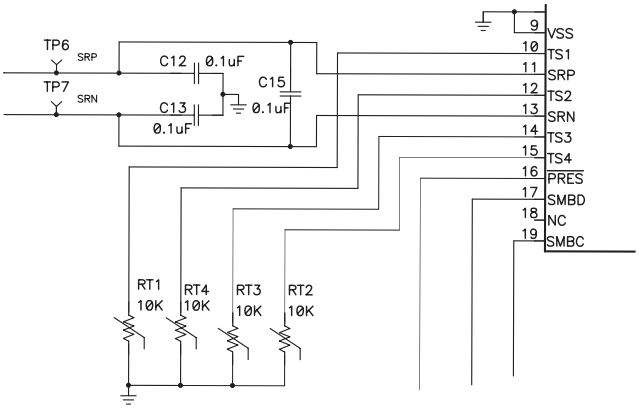

Figure 19. Thermistor Drive

9.2.2.3.6 LEDs

The LEDs do not need current-limiting resistors, because the bq3050 LED pins have a programmable current sink to simplify the design (Figure 20). The display switch pulls the bq3050 pin 20 to ground to generate an interrupt. The REG33 output powers the LEDs.

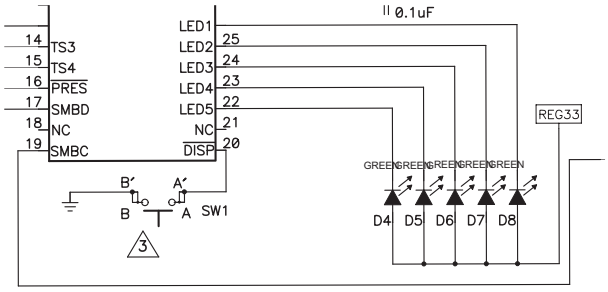

Figure 20. LEDs

9.2.2.3.7 Safety PTC Thermistor

The bq3050 device provides support for a safety PTC thermistor (Figure 21). The PTC thermistor is connected between the PTC pin and V_{SS}. It can be placed close to the CHG/DSG FETs to monitor the temperature. The PTC pin outputs a very small current, typical approximate 370 nA, and the PTC fault will be triggered at approximately 0.7 V typical. A PTC fault is one of the permanent failure modes. It can only be cleared by a POR.

To disable this feature, connect a 10-KΩ resistor between PTC and V_{SS}.

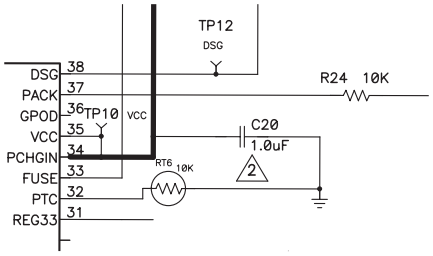

Figure 21. PTC Thermistor

9.2.2.4 Secondary-Overvoltage Protection

The bq29705 provides secondary-overvoltage protection and commands the chemical fuse to ignite if any cell exceeds the internally referenced threshold. The peripheral components are Cell Inputs and Time Delay Capacitor.

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9.2.2.4.1 Cell Inputs

An input filter is provided for each cell input. This comprises the resistors R5, R6, R7, and R9 along with capacitors C5, C6, C7, and C8 (Figure 22). This input network is completely independent of the filter network used as input to thebq3050. To ensure independent safety functionality, the two devices must have separate input filters.

Because the filter capacitors are implemented differentially, a low-voltage device can be used in each case.

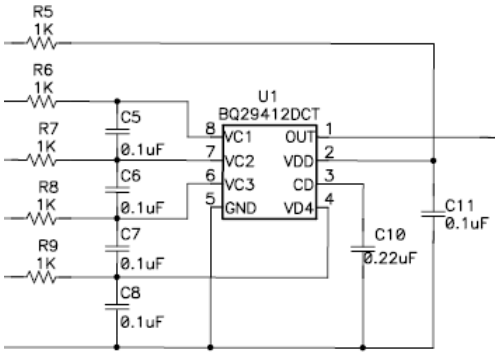

Figure 22. bq29705 Cell Inputs and Time-Delay Capacitor

9.2.2.4.2 Time-Delay Capacitor

C10 sets the time delay for activation of the output after any cell exceeds the threshold voltage. The time delay is calculated as td = 1.2 V × DelayCap (µF)/0.18 µA.

9.2.3 Application Curves

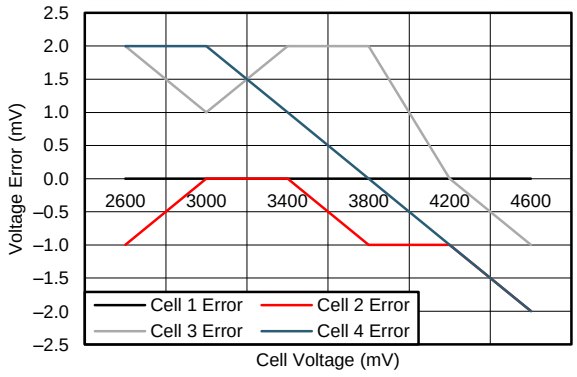

Figure 23. Cell Voltage Error Across Input Range at 25°C

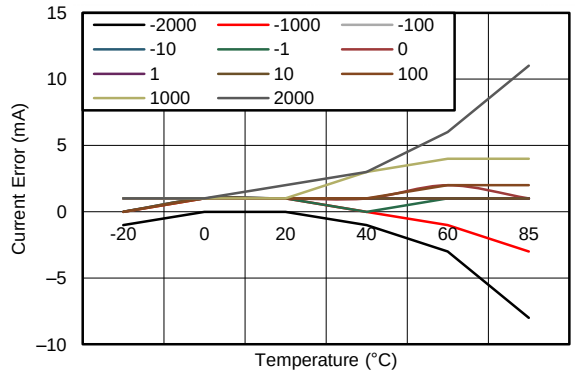

Figure 24. Current Error vs. Temperature

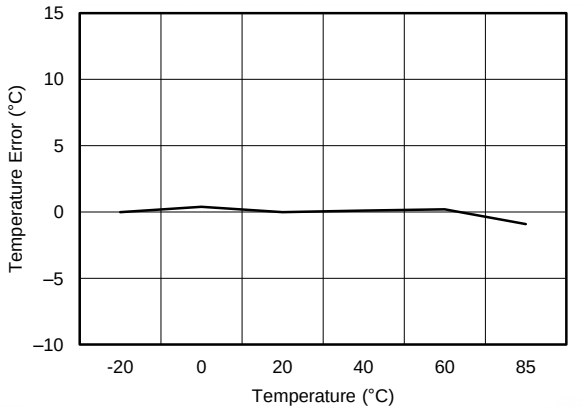

Figure 25. TSx Error vs. Temperature

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10 Power Supply Recommendations

Power supply decoupling is important for optimal operation of the bq3050 Gas Gauge. A single 1.0-µF ceramic decoupling capacitor from REG33 to VSS and REG25 to VSS must be placed adjacent to the integrated circuit (IC) pins.

The RBI pin is used to supply backup RAM voltage during brief transient-power outages. The partial reset mechanism makes use of RAM to restore the critical CPU registers following a temporary loss of power. A standard 0.1-µF ceramic capacitor is connected from the RBI pin to ground.

11 Layout

11.1 Layout Guidelines

The predominant layout concern for the bq3050 is related to the coulomb counter measurement. The external components and PCB layout surrounding the SRP and SRN pins should be carefully considered.

11.2 Layout Example

As shown in Figure 26, a differential filter must precede the current sense inputs of the gas gauge. This filter eliminates the effect of unwanted digital noise, which can cause offset in the measured current. Even the best differential amplifier has less common-mode rejection at high frequencies. Without a filter, the amplifier input stage may rectify a strong RF signal, which then may appear as a dc-offset error.

Five percent tolerance of the components is adequate, because capacitor C15 shunts C12 and C13 and reduces AC common mode arising from a component mismatch. It is important to locate C15 as close as possible to the gas gauge pins. The other components also must be relatively close to the IC. The ground connection of C12 and C13 must be close to the IC. It is also proven to reduce offset and noise error by maintaining a symmetrical placement pattern and adding ground shielding for the differential filter network.

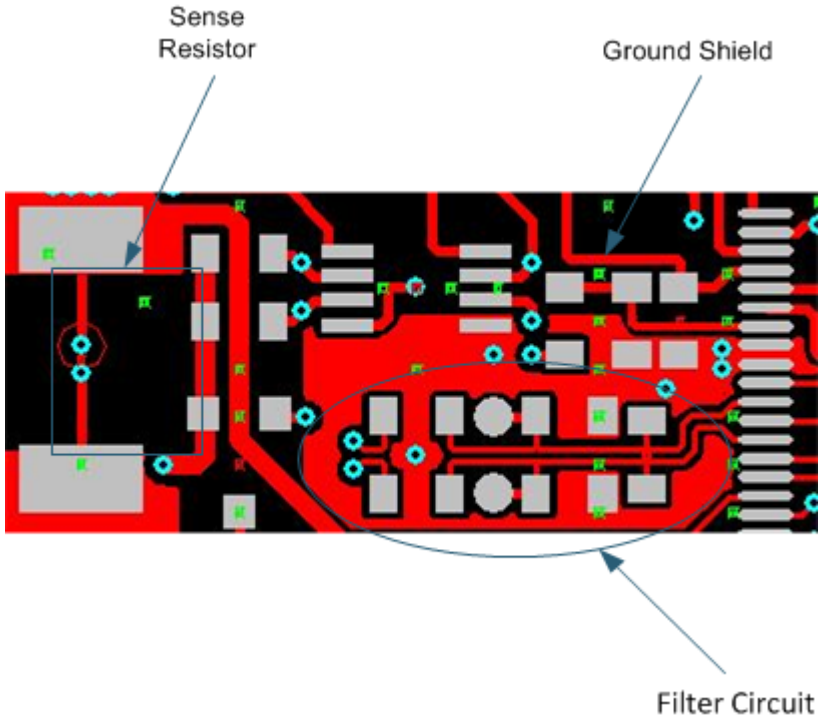

Figure 26. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *bq3050 Technical Reference Manual* (SLUU485)
- *Fast Cell Balancing Using External MOSFET* (SLUA420)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ3050DBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ3050	Samples
BQ3050DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ3050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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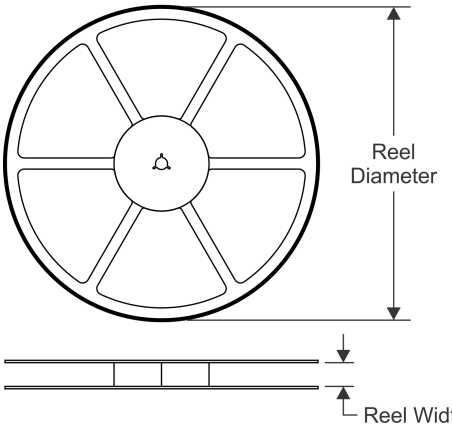
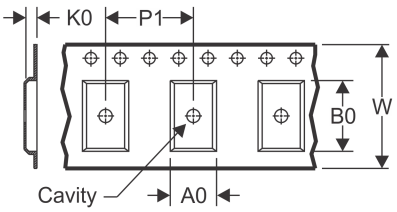
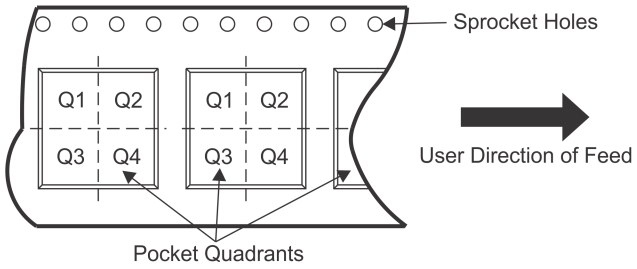


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

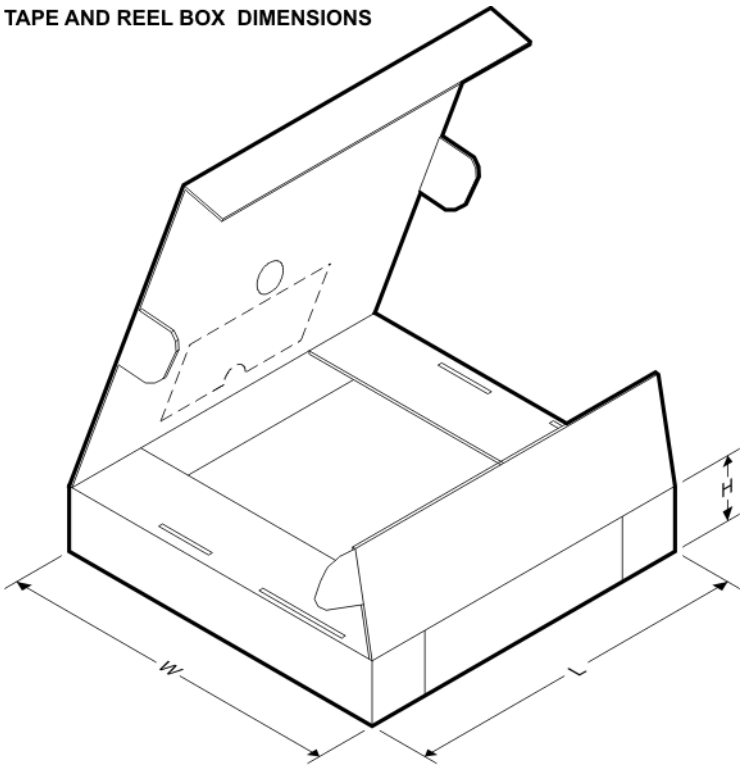
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ3050DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

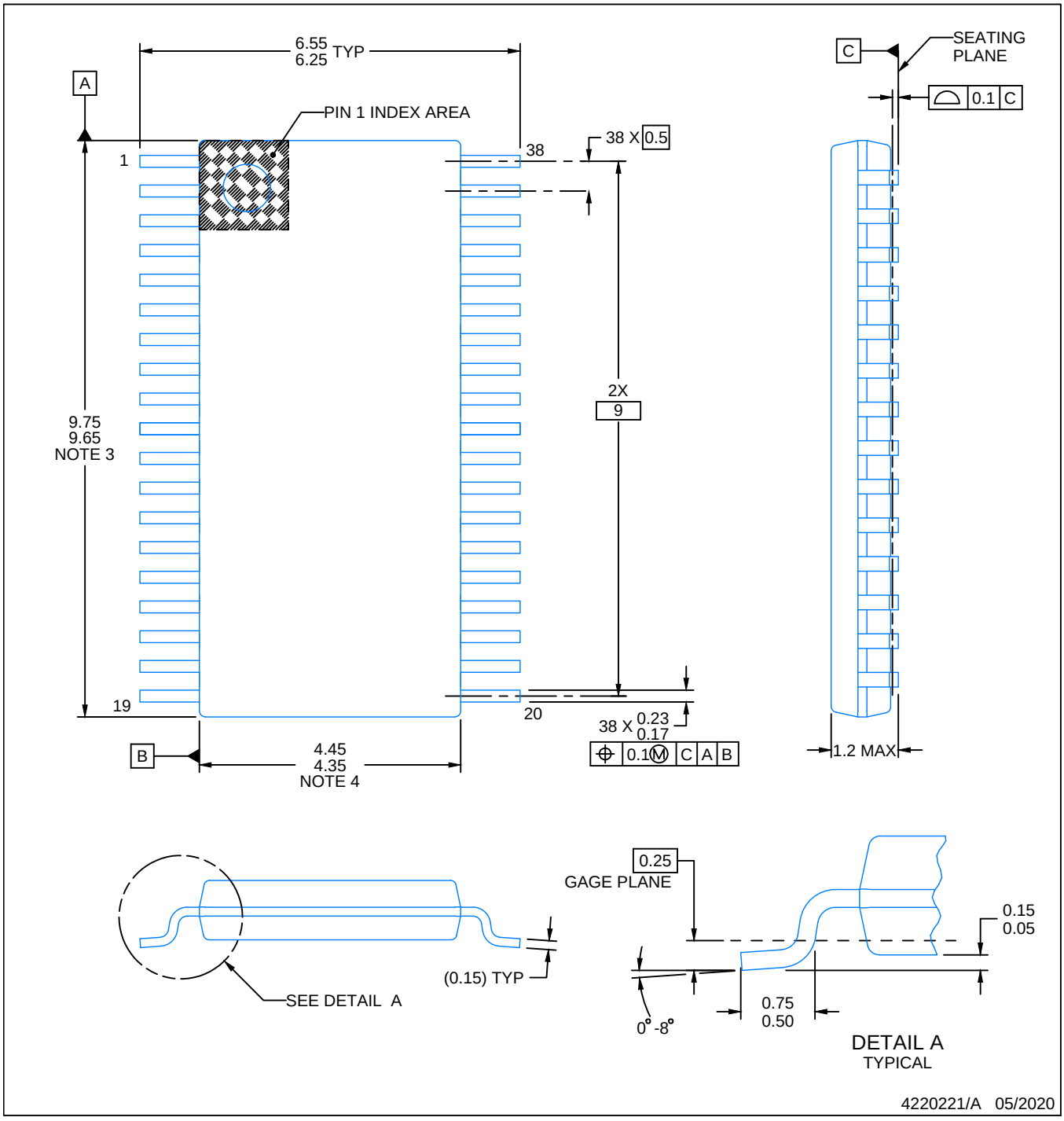
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ3050DBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DBT0038A

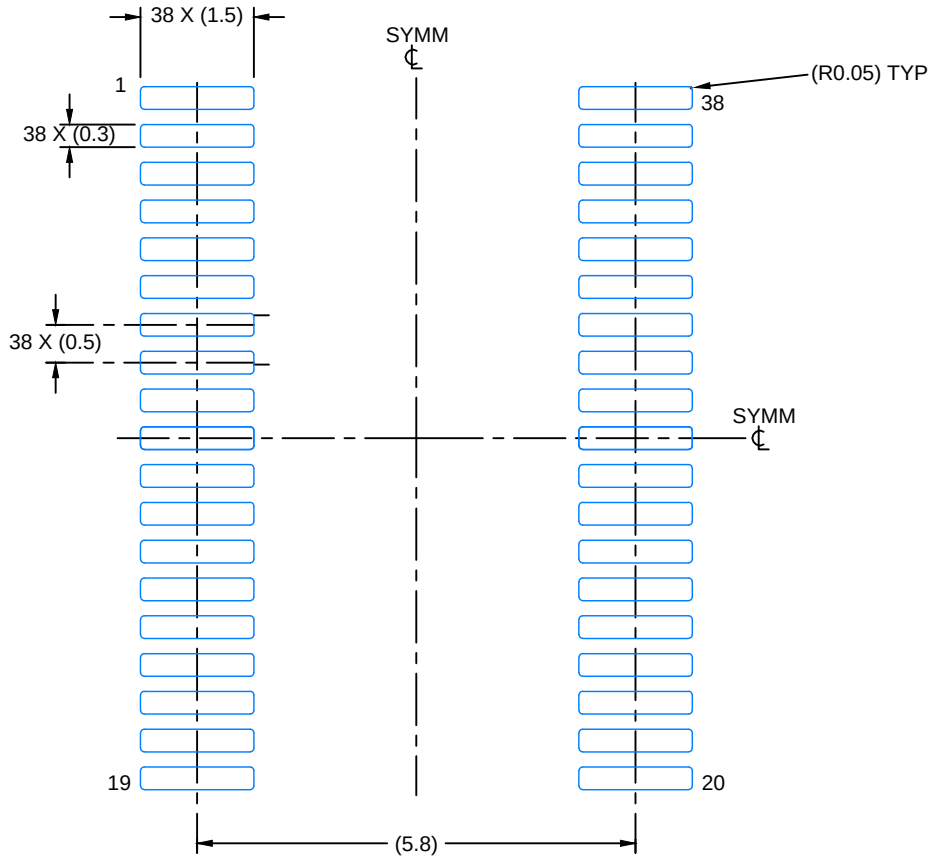
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

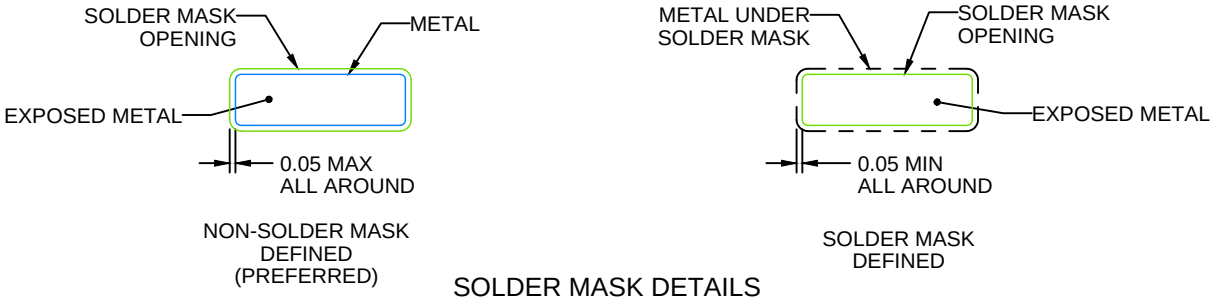


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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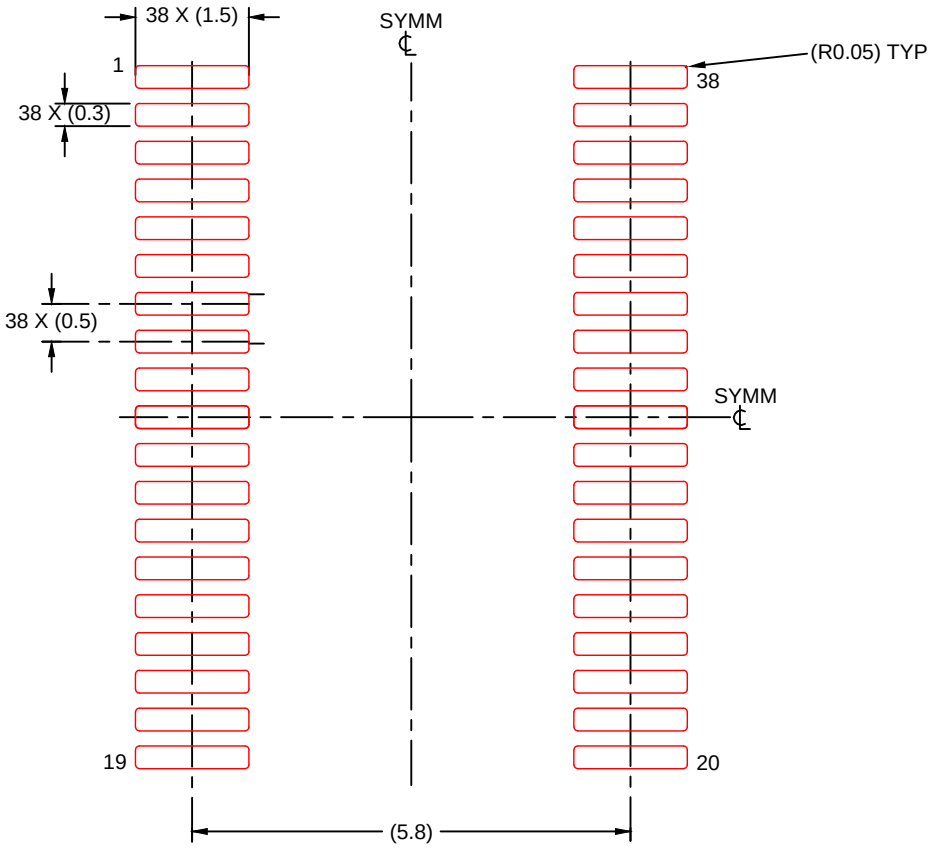
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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