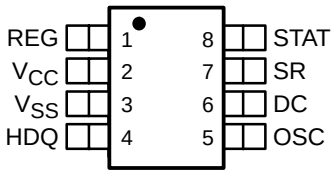
- **Multifunction Monitoring IC Designed to Work With an Intelligent Host Controller**
  - **Provides State-of-Charge Information for Rechargeable Batteries**
  - **Enhances Charge Termination**
- **Ideal for Single-Cell Li-Ion or 3-Cell NiMH Applications**
- **High-Accuracy Coulometric Charge and Discharge Current Integration With Offset Calibration**
- **32 Bytes of General-Purpose RAM**
- **96 Bytes of Flash (Including 32 Bytes of Shadow Flash)**
- **8 Bytes of ID ROM**
- **Internal Temperature Sensor Eliminates the Need for an External Thermistor**
- **Multifunction Digital Output Port**
- **High-Accuracy Internal Timebase Eliminates External Crystal Oscillator**
- **Low Power Consumption**
  - **Operating: <80 μA**
  - **Sleep: <1.5 μA**
- **Single-Wire HDQ Serial Interface**
- **Packaging: 8-Lead TSSOP**

PW PACKAGE
(TOP VIEW)



DC – Internal connection only. Do not connect

description

The bq2019 advanced battery-monitoring IC accurately measures the charge and discharge currents in a rechargeable battery pack. In pack integration, the bq2019 is the basis of a comprehensive battery-capacity management system in portable applications such as cellular phones, PDAs, or other portable products.

The bq2019 works with the host controller in the portable system to implement the battery management system. The host controller interprets the bq2019 data and communicates meaningful battery data to the end-user or power-management system.

The bq2019 provides 64 bytes of general-purpose flash memory, 8 bytes of ID ROM, and 32 bytes of flash-backed RAM for data storage. The nonvolatile memory can maintain formatted battery-monitor information, identification codes, warranty information, or other critical battery parameters when the battery is temporarily shorted or deeply discharged.

AVAILABLE OPTIONS

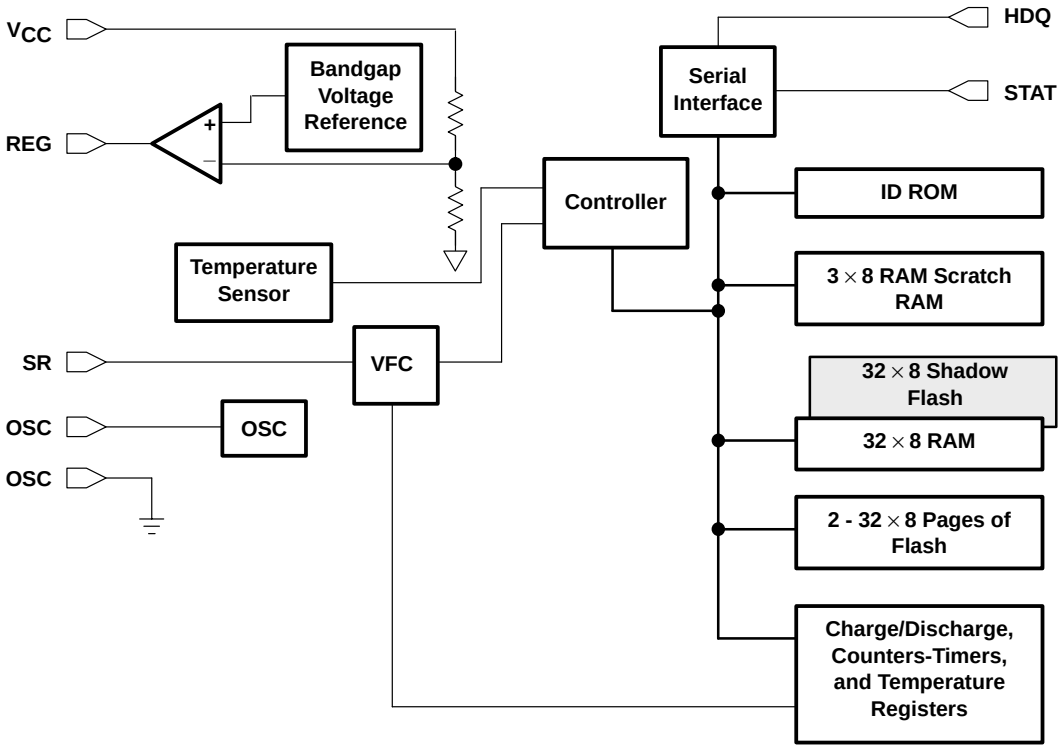
T_A	MARKING	PACKAGED DEVICE
		8-LEAD TSSOP (PW)
–20°C to 70°C	bq219	bq2019PW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
HDQ	4	I/O	Single-wire HDQ interface
DC	6	I	Internal connection only. Do not connect.
OSC	5	O	Time-base adjust for the oscillator
REG	1	O	Regulator output
SR	7	I	Current-sense input
STAT	8	O	Open-drain status output
V_{CC}	2	I	Supply voltage
V_{SS}	3		Ground

detailed description

REG (Regulator output)

REG is the output of the operational amplifier that drives an external pass N-channel JFET to provide an optional regulated supply. The supply is regulated at 4.75 V nominal.

HDQ (Data input/output)

HDQ is a single-wire serial communications interface port. This bidirectional input/output communicates the register information to the host.

STAT (Status Output)

STAT is a general-purpose output port; its state is controlled via the HDQ serial communications interface.

SR (Current sense inputs)

The bq2019 interprets charge and discharge activity by monitoring and integrating the voltage between SR and V_{SS}.

OSC (Time Base Adjust for the Oscillator)

OSC is a programmable current source that adjusts the internal time base by an external resistor.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{CC} with respect to GND) . . . . . –0.3 to 7 V
Input voltage, SR (all with respect to GND) . . . . . –0.3 V to V_{CC}+0.3 V
Output current (STAT pin) . . . . . 5 mA
Output current (REG pin) . . . . . 400 nA
Output current (HDQ pin) . . . . . 5 mA
Operating free-air temperature range, T_A . . . . . –20°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 s) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		2.8		5.5	V
Supply current, I_{CCOP}	V_{CC} = 5.5 V, flash programming not active		88	100	µA
	V_{CC} = 4.3 V, flash programming not active		80	90	µA
Sleep current, I_{SLEEP}	V_{CC} = 4.3 V, flash programming not active		1		µA
Flash programming supply current, I_{CCPROG}	V_{CC} = 5.5		16	25	mA
Flash erase supply current, $I_{CCERASE}$	V_{CC} = 5.5		16	25	mA
Operating ambient temperature, T_{OPR}		–20		70	°C

electrical characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

dc

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Digital output low HDQ pin	I_{OL} = 350 µA			0.4	V
I_{OL}	Digital output low sink current				350	µA
V_{IL}	Digital input low HDQ pin				0.7	V
V_{IH}	Digital input high HDQ pin	V_{CC} < 4.2 V	1.7			V
V_{IH}	Digital input high HDQ pin	V_{CC} > 4.2 V	1.9			R
$Z_{(SR)}$	SR input impedance	0.2 V < V_{SR} <V_{CC}	10			MΩ

ac

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power on reset delay	Delay time after V_{CC} is at least 2.8 V before HDQ communication is attempted.			500	ms

timer characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator current coefficient	Variation of oscillator frequency due to change in R_{OSC}			10	ppm/Ω
Timer accuracy error	R_{OSC} = 100 kΩ	–3%		3%	

temperature register characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reported temperature resolution			1		°K
Reported temperature accuracy	V_{CC} = 3.6 V	–3		3	°K
Reported temperature drift			–2		°K/V

REG pin characteristics over recommended operation temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator threshold		4.5	4.75	5	V
$V_{gs(off)}$	N-channel JFET for regulation	1.5		4.2	V

VFC characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		–100		100	mV
Charge/discharge gain	Temperature = 25°C, V_{CC} = 3.6 V	89	90.5	92	Hz/V
Supply voltage gain coefficient	–100 V < V_{SR} < 100 mV		0.5		%/V
Temperature gain coefficient			0.005		%/°C
Integrated nonlinearity	–100 V < V_{SR} < 100 mV		0.2%	0.5%	
Offset voltage		–500	–40	500	µV
Compensated offset	At calibrated temperature and voltage	–10	0	10	µV
	2.8 V ≤ V_{CC} ≤ 4.2 V	–25		25	

flash memory characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention				5	Years
Flash programming write-cycles		10000			Cycles
Byte programming time				90	µs
RAM-to-flash block programming time				1520	µs
Block-erase time				1520	µs

Standard serial communication (HDQ) timing specification over recommended operating temperature and supply voltage (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(B)}$	Break timing		190			µs
$t_{(BR)}$	Break recovery time		40			µs
$t_{(CYCH)}$	Host bit window		190			ns
$t_{(HW1)}$	Host sends 1		32		50	µs
$t_{(HW0)}$	Host sends 0		100		145	µs
$t_{(RSPS)}$	bq2019 to host response		190		320	µs
$t_{(CYCD)}$	bq2019 bit window		190		250	µs
$t_{(start\text{-}detect)}$	See Note 1		5			ns
$t_{(DW1)}$	bq2019 sends 1		32		50	µs
$t_{(DW0)}$	bq2019 sends 0		80		145	µs

NOTE 1: The HDQ engine of the bq2019 interests a 5-ns or longer glitch on HDQ as a bit start. A sufficient number of glitches 5 ns or longer could result in incorrect data being written to the device. The HDQ line should be properly deglitched to ensure that this does not occur.

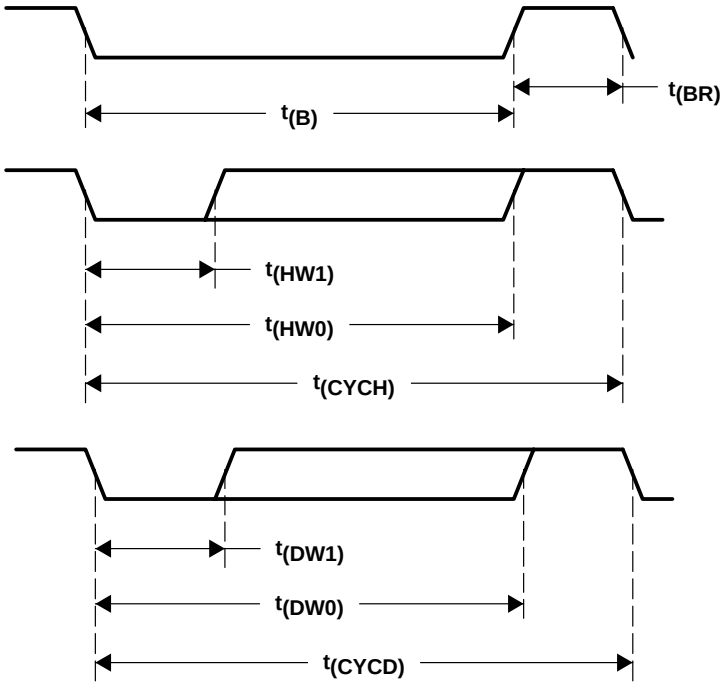


Figure 1. HDQ Timing Diagram

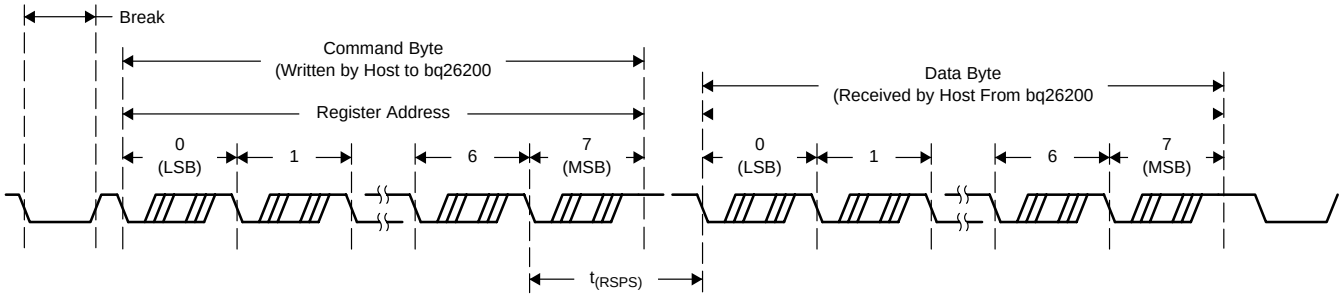
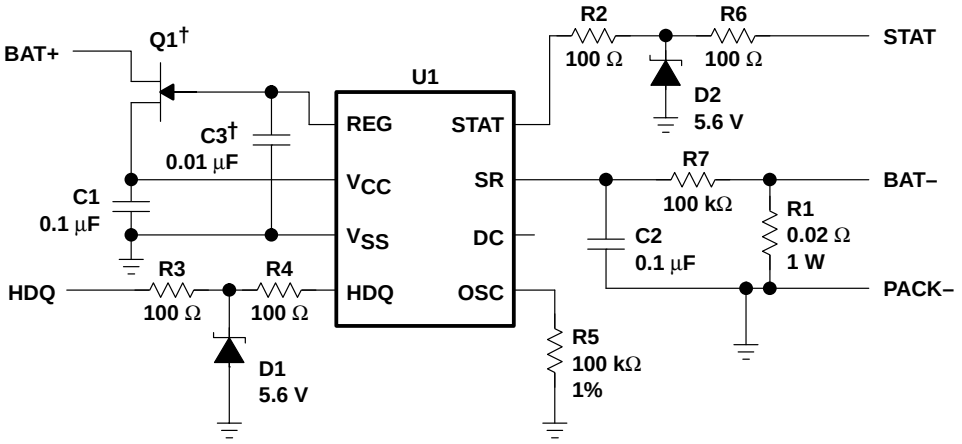


Figure 2. Typical Communication With the bq26200

APPLICATION INFORMATION



† Q1 and C3 are omitted and V_{CC} is connected to BAT+ for single cell lithium ion applications

functional description

The bq2019 measures the voltage drop across a low-value series-current sense-resistor between the SR and V_{SS} pins using a voltage to frequency converter. This information is placed into various internal counter and timer registers. Using information from the bq2019, the system host can determine the battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge currents. During pack storage periods, the use of an internal temperature sensor doubles the self-discharge count rate every 10° above 25°C.

Optionally, the VFC offset is calibrated and automatically compensated for in the charge counter registers. Access to the registers and control of the bq2019 is accomplished by a single-wire interface through a register-mapped command protocol that includes placing the device in the low-power mode, resetting the hardware register, programming flash from RAM, and transferring flash data to RAM.

The bq2019 can operate directly from three or four nickel-chemistry cells or a single Li-Ion cell as long as V_{CC} is between 2.8 V and 5.5 V. To reduce cost in multicell applications, power to the bq2019 may be regulated using a low-cost external FET with the REG pin.

REG output

The bq2019 can operate directly from three or four nickel-chemistry cells or from a single Li-Ion cell as long as V_{CC} is between 2.8 V and 5.5 V. To facilitate the power supply requirements of the bq2019, the REG output is used with an external low-threshold n-JFET when regulation from a higher source potential is required. The REG output remains active in sleep mode. For applications that do not need the REG output, operating current is reduced by turning off the operational amplifier with the DISREG bit in the MODE/WOE register. For more details, refer to the *MODE/WOE Register* section.

APPLICATION INFORMATION

REG output (continued)

charge and discharge count operation

Table 1 shows the main counters and registers of the bq2019. The bq2019 accumulates charge and discharge counts into two count registers: the charge count register (CCR) and the discharge count register (DCR). Charge and discharge counts are generated by sensing the voltage difference between SR and V_{SS}. The CCR or DCR independently counts, depending on the signal between pins SR and V_{SS} (V_{SR}).

During discharge, the DCR and the discharge time counter (DTC) are active. If V_{SR} is less than 0, indicating a discharge activity, the DCR counts at a rate equivalent to one count per 3.05 μVH, and the DTC counts at a rate of 1.138 counts per second (4096 counts = 1 hour). For example, if no rollover of the DTC register is incipient, a negative 24.42 mV signal between pins SR and V_{SS} produces 8000 DCR counts and 4096 DTC counts each hour. The amount of charge removed from the battery is easily calculated.

During charge, the CCR and the charge time counter (CTC) are active. If V_{SR} is greater than 0, indicating a charge, the CCR counts at a rate equivalent to one count per 3.05 μVH, and the CTC counts at a rate of 1.138 counts per seconds. In this case a +24.42 mV signal produces 8000 CCR counts and 4096 CTC counts (assuming no rollover) each hour.

The DTC and the CTC are 16-bit registers, with rollover beyond ffffh. If a rollover occurs, the corresponding bit in the MODE/WOE register is set, and the counter increments at 1/256 of the normal rate (16 counts per hour). While in normal operation, the internal RAM and flash registers of the bq2019 may be accessed over the HDQ pin, as described in the section *Communicating With the 2019*.

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate of 1 count every hour at a nominal 25°C. The SCR count rate doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10°C below 25°C down to 0°C. The value in SCR is useful in estimating the battery self-discharge on the basis of capacity and storage temperature conditions.

The offset register contained in the CAL/OFFCTH, OFFCTM and OFFCTL locations stores the bq2019 offset. At a period representing the amount of positive or negative offset, the bq2019 automatically adds an equivalent count to either the CCR or DCR registers. The maximum uncalibrated offset for the bq2019 is ±500 μV. Care should be taken to ensure proper PCB layout. Using OFR, the system host can cancel most of the effects of bq2019 offset for greater resolution and accuracy.

Table 1 shows the bq2019 register address map. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.

Table 1. bq2019 Counters

NAME	DESCRIPTION	RANGE	RAM SIZE
DCR	Discharge count register	$V_{SR} < V_{SS}$ (Max. = –100 mV) 3.05 μV/LSB	16-bit
CCR	Charge count register	$V_{SR} > V_{SR}$ (Max. = +100 mV) 3.05 μV/LSB	16-bit
SCR	Self-discharge count register	1 count/hour at 25°C	16-bit
DTC	Discharge time counter	1 count/0.8789s (default) 1 count/225s if STD is set	16-bit
CTC	Charge time counter	1 count/0.8789s (default) 1 count/225s if STC is set	16-bit

APPLICATION INFORMATION

REG output (continued)

low-power operation

The bq2019 begins low-power operation in response to the host issuing the sleep command. Before entering the low-power state, the host processor should write the command to transfer the registers to flash. After the sleep command is sent and the charge/discharge activity is less than the value indicated by the WOE bits shown in Table 3, the chip clock is powered down and data-acquisition functions cease except for self-discharge updates. Setting the WOE bits to 0 causes the device to enter sleep mode, regardless of the level of charge/discharge activity. During device sleep the bq2019 periodically wakes briefly to update the temperature registers and self-discharge rate. The bq2019 wakes on either a low-to-high or high-to-low transition on the HDQ pin.

Table 2. Operational States

MODE	ACTIVE REGISTERS
Normal	CCR, DCR, CTC, DTC, SCR
Sleep	SCR

Table 3. WOE Thresholds

$WOE_{3–1}$ (HEX)	V_{WOE} (mV)
0h	NA
1h	3.516
2h	1.758
3h	1.172
4h	0.879
5h	0.703
6h	0.586
7h	0.502

APPLICATION INFORMATION

REG output (continued)

current sense offset

calibration

The host enables bq2019 current sense offset calibration by one of two methods. The first method is resetting the CALREQ bit in the CAL/OFFCTH register to 1. The second method is by issuing the calibrate and power-down command to the FCMD register. In both cases, when $|V_{SR}|<V_{WOE}$, the bq2019 enters calibration mode. When calibration is complete, the $\overline{\text{CALOK}}$ bit is set to 0 by the bq2019. The bq2019 performs offset calibration by measuring the time between two like-polarity VFC pulses and placing this value in the OFFCTH, OFFCTM, and OFFCTL registers. The LSB of the OFFCTH, OFFCTM, and OFFCTL registers is 9.76 ms. If polarity of the second pulse received is opposite that of the first pulse received, then calibration resets and begins again automatically. If during calibrating no pulses occur within 21.3 minutes, or if 21.3 minutes elapse after the first pulse, then the bq2019 times out and assumes the offset is 4.29 μV.

Any external signal present between SR and V_{SS} affects the calibration as calculated by the bq2019. The TVOS bit is optionally available to isolate any unwanted residual current (such as bq2019 operational current through the sense resistor) from the offset current measurements. This is done by internally shorting the SR pin during calibration. When the TVOS bit is set to 1, the bq2019 shorts the SR pin to V_{SS} in response to the value written to the bit.

compensation

After offset calibration, two methods to compensate for current-sense offset are available. The first method is to have the bq2019 automatically compensate for current offset. After a successful calibration (i.e., $\overline{\text{CALOK}}$ is 0), the bq2019 automatically compensates for offset when COMPEN bit is set to 1. The bq2019 then periodically increments either the charge or discharge counter register, depending on the state of the CHGOFF bit. This period is calculated by multiplying the OFFCTH, OFFCTM, and OFFCTL registers by 9.76 ms.

The second method is for the host to periodically read the OFFCTH, OFFCTM, and OFFCTL registers and adjust battery capacity.

gas gauge control registers

The host maintains the charge and discharge and the self-discharge count registers (CCR, CTC, DCR, DTC, and SCR). To facilitate this maintenance, the bq2019 CLR register resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq2019 completes the reset, the corresponding bit in the CLR register is automatically reset to 0. Clearing the DTC or CTC registers clears the MODE/WOE register bits STC/STD and sets the CTC/DTC count rates to the default value of 1.138 counts per second.

device temperature measurement

The bq2019 reports die temperature in units of °K in 9 bits through registers TMPL and TMPH[0]. Refer to the TMP register description for more details.

register interface

Information is exchanged between host system and the bq2019 through the data-register interface (see Table 4). The register set consists of a 122-location address space of 8-bit bytes segmented into

- 8 bytes of factory-programmed ID ROM
- 32 bytes of flash-shadowed RAM
- 64 bytes of general-purpose flash
- 18 special function registers

APPLICATION INFORMATION

register interface (continued)

Table 4. bq2019 Registers

HDQ ADDRESS	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x78–0x7F	IDROM	8 bytes of factory-programmed ROM							
0x77	CAL/OFFCTH	COMPEN	CALREQ	$\overline{\text{CALOK}}$	CHGOFF	Flash-shadowed VFC offset bits 19–16			
0x76	OFFCTM	Flash-shadowed offset register bits 15–8							
0x75	OFFCTL	Flash-shadowed offset register bits 7–0							
0x74	—	Reserved							
0x73	—	Reserved							
0x72	—	Reserved							
0x71		Reserved							
0x70	FPA	Program address byte							
0x6F	FPD	Flash program data byte							
0x6E	DCRH	Discharge count register high byte							
0x6D	DCRL	Discharge count register low byte							
0x6C	CCRH	Charge count register high byte							
0x6B	CCRL	Charge count register low byte							
0x6A	SCRH	Self-discharge count register high byte							
0x69	SCRL	Self-discharge count register low byte							
0x68	DTCH	Discharge timer counter register high byte							
0x67	DTCL	Discharge timer count register low byte							
0x66	CTCH	Charge timer counter register high byte							
0x65	CTCL	Charge timer counter register low byte							
0x64	MODE/WOE	TVOS	DISREG	STC	STD	WOE2	WOE1	WOE0	BIT0
0x63	CLR	RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR
0x62	FCMD	Flash/control command register							
0x61	TMPH	Reserved						TEMP[8]	
0x60	TMPL	TEMP[7:0]							
0x40–0x5F	Flash	PAGE2, 32 bytes of flash							
0x20–0x3F	Flash	PAGE1, 32 bytes of flash							
0x00–0x1F	RAM/flash	PAGE0, 32 bytes of flash-shadowed RAM							

memory

ID ROM

The bq2019 has 8 bytes of ID ROM. This data field can be factory programmed to the customer request, insuring a unique and secure product serialization. Contact your Texas Instruments representative for details.

flash-shadowed RAM

The host system has direct access to read and modify 32 bytes of RAM. These 32 bytes are shadowed by 32 bytes of flash to provide nonvolatile storage of battery conditions. The information stored in RAM is transferred to flash, and the information stored in flash is transferred to RAM by writing a single command into the flash command register (FCMD). When a power-on-reset occurs, PAGE0 of flash and three flash-shadowed offset bytes are transferred to RAM. (The host is responsible for storing offset value in flash.) For more details, refer to the *flash command register* section.

APPLICATION INFORMATION

memory (continued)

flash memory

In addition to the flash-shadowed RAM, the bq2019 has 64 bytes of flash. The flash can store specific battery pack parameters, such as charge per VFC pulse, battery chemistry, and self-discharge rates.

flash programming

The two banks of direct flash are programmed one byte at a time, but the single bank of flash-shadowed RAM can be programmed one page at a time or by writing the RAM-to-flash transfer code into the flash command register (FCMD). This programming is performed by writing the desired code into the flash command register, FCMD (address 0x62), the host may transfer data between flash and RAM, page erase the flash, place the device into the low power mode, or perform VFC offset measurement. For more details, refer to the *flash command register* section. Summaries of the flash command codes are shown in Table 5.

Table 5. Flash Command Code Summary

COMMAND CODE (HEX)	DESCRIPTION
0x0F	Program byte
0x40	Erase page 0 flash
0x41	Erase page 1 flash
0x42	Erase page 2 flash
0x43	Erase offset control shadow flash
0x45	Transfer page 0 RAM to page 0 flash
0x48	Transfer page 0 flash to page 0 RAM
0xF6	Power down
0xF7	Calibrate VFC and power down

single-byte programming

To program an individual byte in flash, the byte of data is first written into the FPD register while the address to be programmed is written into the FPA register. The program byte command, 0x0F is then written to the FCMD. The result of this sequence is that the contents of the FPD register are logically ANDed with the contents of the flash address pointed to by the FPA register.

RAM-to-flash transfer

The content of the flash that shadows the user RAM is logically ANDed to the RAM contents when the RAM-to-flash transfer command is sent. If new data are to be written over old data, then it is necessary to first erase the flash page that is being updated and restore all necessary data.

APPLICATION INFORMATION

communicating with the bq2019

The bq2019 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, use the interface to access various bq2019 registers. The HDQ pin requires an external pullup or pulldown resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq2019. The command directs the bq2019 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte. The communication protocol asynchronous return-to-one is referenced to V_{SS}.

Command and data bytes consist of a stream of eight bits with a maximum transmission rate of 5 Kbits/s. The least-significant bit of a command or data byte is transmitted first. Data input from the bq2019 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART can also communicate with the bq2019. If a communication time-out occurs (for example, if the host waits longer than t_{CYCB} for the bq2019 to respond or if this is the first access command), then a BREAK should be sent by the host. The host may then resend the command. The bq2019 detects a BREAK when the HDQ pin is driven to a logic-low state for a time t_B or greater. The HDQ pin then returns to its normal ready-high logic state for a time t_{BR} The bq2019 is then ready for a command from the host processor.

The return-to-one data-bit frame consists of three distinct sections. The first section starts the transmission by either the host or the bq2019 taking the HDQ pin to a logic-low state for a period $t_{STRH,B.}$. The next section is the actual data transmission, where the data should be valid by a period $t_{DSU,B,}$ after the negative edge that starts communication. The data should be held for a period $t_{\Delta V}$ /$t_{\Delta H}$ to allow the host or bq2019 to sample the data bit. The final section stops the transmission by returning the HDQ pin to a logic-high state by at least a period $t_{SSU,B}$ after the negative edge used to start communication. The final logic-high state should be held until a period, $t_{CYCH,B}$, to allow time to ensure that the bit transmission ceased properly. The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq2019 always occurs with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2019 OFR register.

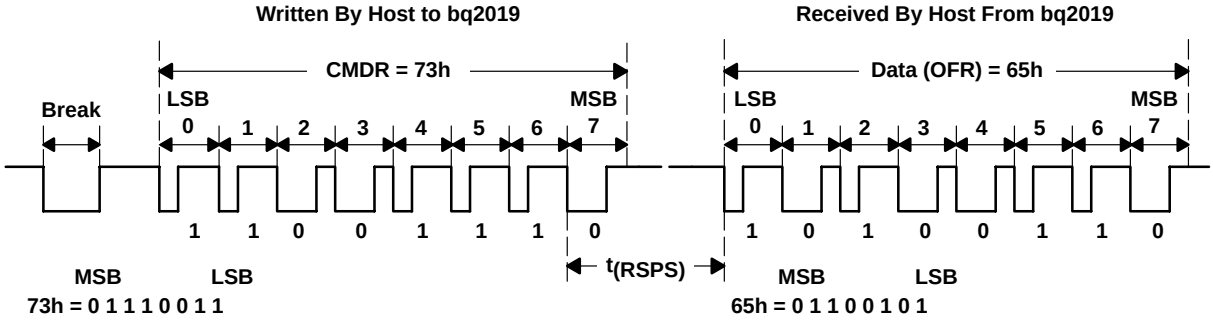


Figure 3. Communication Sequence

APPLICATION INFORMATION

communicating with the bq2019 (continued)

command byte

The command byte of the bq2019 consists of eight contiguous valid command bits. The command byte contains two fields: W/R command and address. The W/R bit of the command register determines whether the command is a read or a write command, and the address field containing bit AD6-AD0 indicates the address to be read or written. The command byte values are shown in the following table:

COMMAND BYTE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

W/R Indicates whether the command byte is a read or write command. A 1 indicates a write command and that the following eight bits should be written to the register specified by the address field of the command byte, while a 0 indicates that the command is a read. On a read command, the bq2019 outputs the requested register contents specified by the address field portion of the command byte.

AD6–AD0 The seven bits labeled AD6–AD0 containing the address portion of the register to be accessed.

APPLICATION INFORMATION

bq2019 registers

register maintenance

The host system is responsible for register maintenance. To facilitate this maintenance, the bq2019 clear register (TMP/CLR) resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq2019 completes the reset, the corresponding bit in the TMP/CLR register automatically resets to 0, saving the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of 1 count per 0.8789 s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of 1 count per 0.8789 s.

register map

HDQ ADDRESS	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x78–0x7F	IDROM	8 bytes of factory-programmed ROM							
0x77	CAL/	COMPEN	CALREQ	$\overline{\text{CALOK}}$		CHG OFF	Flash-shadowed VFC offset bits 19–16		
0x76	OFFCTM	Flash-shadowed offset register bits 15–8							
0x75	OFFCTL	Flash-shadowed offset register bits 7–0							
0x74	—	Reserved							
0x73	—	Reserved							
0x72	—	Reserved							
0x71		Reserved							
0x70	FPA	Program address byte							
0x6F	FPD	Flash program data byte							
0x6E	DCRH	Discharge count register high byte							
0x6D	DCRL	Discharge count register low byte							
0x6C	CCRH	Charge count register high byte							
0x6B	CCRL	Charge count register low byte							
0x6A	SCRH	Self-discharge count register high byte							
0x69	SCRL	Self-discharge count register low byte							
0x68	DTCH	Discharge timer counter register high byte							
0x67	DTCL	Discharge timer count register low byte							
0x66	CTCH	Charge timer counter register high byte							
0x65	CTCL	Charge timer counter register low byte							
0x64	MODE/WOE	TVOS	DISREG	STC	STD	WOE2	WOE1	WOE0	BIT0
0x63	CLR	RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR
0x62	FCMD	Flash/control command register							
0x61	TMPH	Reserved						TEMP[8]	
0x60	TMPL	TEMP[7:0]							
0x40–0x5F	Flash	PAGE2, 32 bytes of flash							
0x20–0x3F	Flash	PAGE1, 32 bytes of flash							
0x00–0x1F	RAM/	PAGE0, 32 bytes of flash-shadowed RAM							

APPLICATION INFORMATION

register descriptions

IDROM register

The factory programmed 64 bits of ID ROM are located in the eight-byte locations addressed 0x78–0x7f. These bits can be programmed to a customer's specification. Contact your Texas Instruments representative for details.

calibration and offset registers (CAL/OFFCTH, OFFCTM, OFFCTL)

The CAL/OFFCTH register (address 0x77) enables offset compensation, initiates offset calibration, and indicates that calibration was successful. The register also contains partial-offset correction information. The OFFCTM, and OFFCTL registers (addresses 0x76 and 0x75) contain the balance of the offset correction information used during current offset compensation.

CAL/OFFCTH							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMPEN	CALREQ	$\overline{\text{CALOK}}$	CHGOFF	Flash-shadowed offset bits 19–16			

OFFCTM							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Flash-shadowed offset bits 15–8							

OFFCTL							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Flash-shadowed offset bits 7–0							

COMPEN The COMPEN bit enables offset compensation. Offset compensation automatically occurs when COMPEN is set to 1 and a successful calibration has occurred ($\overline{\text{CALOK}}$ = 0). When cleared, compensation is disabled. COMPEN is cleared on power-on-reset.

CALREQ CALREQ bit requests current offset calibration. When this bit is set to 1, the bq2019 waits for the condition $|V_{SR}| < V_{WOE}$. When this condition is satisfied, the bq2019 starts calibration. After calibration is complete, the bq2019 sets the $\overline{\text{CALOK}}$ bit to 0. The CALREQ bit is cleared on power-on-reset and after a successful calibration.

$\overline{\text{CALOK}}$ $\overline{\text{CALOK}}$ bit (read-only) indicates that successful offset calibration has been performed. The $\overline{\text{CALOK}}$ bit is cleared by the bq2019 when the host sets the CALREQ bit. After calibration is complete, the bq2019 sets the $\overline{\text{CALOK}}$ to 0.

CHGOFF CHGOFF bit indicates the polarity of the offset. If the CHGOFF bit is set, the measured offset is positive. The DCR register is incremented if the COMPEN bit is set. If the CHGOFF bit is cleared, the measured offset is negative and the CCR is incremented If the COMPEN bit is set.

OFFCT[19..0] The 20 OFFCT bits indicate the time between instances of incrementing a count into either the CCR or the DCR registers, depending on the state of the CHGOFF. The LSB of this register is 9.76 ms.

APPLICATION INFORMATION

register descriptions (continued)

flash program address register (FPA)

The FPA byte register (address = 0x70) points to the flash address location that is programmed when the program flash command is issued. This byte is used with the FPD and FCMD register to program an individual byte in flash memory.

flash program data register (FPD)

The FPD byte register (address = 0x6F) contains the data to be programmed into the flash address location pointed to by the contents of the FPA register. When the program flash command is issued, the contents of the FPD register are ANDed with the contents of the byte pointed to by the FPA and then stored into that location.

discharge count registers (DCRH/DCRL)

The DCRH high-byte register (address = 0x6E) and the DCRL low-byte register (address = 0x6D) contain the count of the discharge and are incremented whenever $V_{SR} < V_{SS}$. These registers continue to count beyond ffffh, so proper register maintenance by the host system is necessary. The CLR register forces the reset of both the DCRH and DCRL to zero.

charge count registers (CCRH/CCRL)

The CCRH high-byte register (address = 0x6C) and the CCRL low-byte register (address = 0x6B) contain the count of the charge, and are incremented whenever $V_{SR} > V_{SS}$. These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The CLR register forces the reset of both the CCRH and CCRL to zero.

self-discharge count registers (SCRH/SCRL)

The SCRH high-byte register (address = 0x6A) and the SCRL low-byte register (address = 0x69) contain the self-discharge count. This register is continually updated in both the normal operating and sleep modes of the bq2019. The counts in these registers are incremented on the basis of time and temperature. The SCR counts at a rate of 1 count per hour at 20–30°C. The count rate doubles every 10°C up to a maximum of 16 counts/hour at temperatures above 60°C. The count rate halves every 10°C below 20–30°C to a minimum of 1 count/8 hours at temperature below 0°C. These registers continue to count beyond ffffh, so proper register maintenance is required by the host system. The CLR register forces the reset of both the SCRH and SCRL to zero. During device sleep the bq2019 periodically wakes briefly to maintain the self-discharge registers.

discharge time count registers (DTCH/DTCL)

The DTCH high-byte register (address = 0x68) and the DTCL low-byte register (address = 0x67) determine the length of time the $V_{SR} < V_{SS}$ indicating a discharge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the DTCH/DTCL register continues to count beyond ffffh, the STD bit is set in the MODE/WOE register, indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

NOTE:

If a second rollover occurs, STD is cleared. Access to the bq2019 should be timed to clear DTCH/DTCL more often than every 170 days. The CLR register forces the reset of both the DTCH and DTCL to zero.

APPLICATION INFORMATION

register descriptions (continued)

charge-time count registers (CTCH/CTCL)

The CTCH high-byte register (address = 0x66) and the CTCL low-byte register (address = 0x65) determine the length of time the $V_{SR} > V_{SS}$, indicating a charge activity. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond ffffh, the STC bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

NOTE:

If a second rollover occurs, STC is cleared. Access to the bq2019 should be timed to clear CTCH/CTCL more often than every 170 days. The CLR register forces the reset of both the CTCH and CTCL to zero.

mode, wake-up enable register (MODE/WOE)

As described below, the Mode/WOE register (address = 0x64) contains the offset isolation bit, regulator disable, the STC and STD bits, and wake-up enable information.

MODE/WOE BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TVOS	DISREG	STC	STD	WOE2	WOE1	WOE0	BIT0

TVOS The TVOS bit internally shorts the SR pin to V_{SS}. This bit is available to optionally isolate any unwanted residual current (such as bq2019 operational current through the sense resistor) from the offset current measurements. When the TVOS bit is set to 1, the bq2019 shorts the SR pin to V_{SS}. When TVOS is 0, the SR pin is not shorted.

NOTE:

TVOS should be set to 0 for normal charge counting operation.

DISREG DISREG is the disable regulator bit, which turns off the internal operational amplifier used in the regulator circuit. In applications where the regulator is not used, the DISREG bit can be set to reduce the bq2019 supply current requirements. A 1 turns off the amplifier, whereas a 0 turns the amplifier on.

STC & STD The slow time charge (STC) and slow time discharge (STD) flags indicate whether the CTC or DTC registers have rolled over beyond ffffh. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover.

WOE[2..0] The wake-up output enable (WOE) bits (bits 3–1) indicate the voltage level required on the SR pin so that the bq2019 enters sleep mode after a power-down command is issued. Whenever $|V_{SR}| < V_{WOE}$, the bq2019 enters sleep mode after either the power-down or the calibrate and power-down commands have been issued. On bq2019 power-on reset, these bits are set to 1. Setting all of these bits to zero causes the device to enter sleep mode, regardless of the SR pin voltage. Refer to Table 3 for the various WOE values.

BIT0 BIT0 is a reserved bit and must always be set to 0. This bit is cleared on power-on-reset.

APPLICATION INFORMATION

register descriptions (continued)

clear register (CLR)

The bits in the CLR register (address 0x63) clear the DCR, CCR, SCR, DTC, and CTC registers and reset the bq2019 by forcing a power-on-reset and setting the state of the STAT pin as described below:

CLR BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR

RSVD RSVD bit is reserved for future use and should *not* be modified by the host.

POR POR bit indicates a power-on-reset has occurred. This bit is set when V_{CC} has gone below the POR level. This bit can be also set and cleared by the host, but no functions are affected.

STAT STAT bit (bit 5) sets the state of the open drain output of the STAT pin. A 1 turns off the open drain output, while a 0 turn the output on. This bit is set to 1 on power-on-reset.

CTC CTC bit (bit 4) clears the CTCH and CTCL registers and the STC bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the CTC bit is cleared. This bit is cleared on power-on-reset.

DTC DTC bit (bit 3) clears the DTCH and DTCL registers and the STD bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the DTC bit is cleared. This bit is cleared on power-on-reset.

SCR SCR bit (bit 2) clears both the SCRH and SCRL registers. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.

CCR CCR bit (bit 1) clears both the CCRH and CCRL registers Writing a 1 to this bit clears the CCRH and CCRL registers. After these registers are cleared, the CCR bit is cleared. This bit is cleared on power-on-reset.

DCR DCR bit (bit 0) clears both the DCRH and DCRL registers to 0. Writing a 1 to this bit clears the DCRH and DCRL register. Then the DCR bit is cleared. This bit is cleared on power-on-reset.

APPLICATION INFORMATION

register descriptions (continued)

flash command register (FCMD)

The FCMD register (address 0x62) is the flash command register that programs a single flash byte-location, performs flash page erase, transfers RAM to flash and flash to RAM, enters sleep mode, and calibrates the VFC and power-down. These functions are performed by writing the desired command code to the FCMD register. After the bq2019 has finished executing the issued command, the flash command register is cleared.

0x0F Program byte command code. This code ANDs the contents of the FPD register with the contents of flash byte location pointed to by the contents of the FPA register.

0x40 Erase page 0 command code. This code erases all the bytes of flash from address 0x00 to 0x1F.

0x41 Erase page 1 command code. This code erases all the bytes of flash from address 0x20 to 0x3F.

0x42 Erase page 2 command code. This code erases all the bytes of flash from address 0x40 to 0x5F.

0x43 Erase offset control register shadow flash. This code erases the 3 bytes of flash that shadow the Offset Control Register located at HDQ address 0x75–0x77.

0x45 RAM-to-flash transfer code. This code programs the contents of the RAM into Page 0 flash, addresses 0x00 though 0x1F.

0x48 flash to RAM transfer code. This code copies the contents of the Page 0 flash into RAM.

0xF6 Power-Down code. This code places the bq2019 into the sleep mode when the conditions are met as indicated by the WOE bits in the MODE/WOE register. The part remains in sleep mode until a high-to-low or low-to-high transition occurs on the HDQ pin.

0xF7 Calibrate VFC and power-down code. This command code will initiate a calibration once V_{SR} drops below Vwoe. If the HDQ line toggles low to high to high to low before calibration completes, the device will NOT enter the low power mode. Sending this code must be the last HDQ communication if the device is to go into SLEEP mode.

temperature registers (TMPH, TMPL)

The TMPH (address 0x61) and the TMPL registers (address 0x60) reports die temperature in hex format in units of °K, with an accuracy of typically ±3°K. The temperature is reported as 9 bits of data, using all 8 bits of the TMPL register and LSB of the TMPH register. The temperature should be read as the concatenation of TMPH[0] and TMPL[7:0].

The 7 MSBs of TMPH, TMPH[7:1], are cleared on POR. The bits are reserved and should be written to 0 if the host attempts to write to the TMPH register. The 7 bits should also be masked off when reading the temperature to ensure that incorrect data is not used when calculating the temperature.

ERRATA

Issue : This errata ONLY applies if page 1 (address 0x20– 0x3F) or page 2 (address 0x40– 0x5F) of the embedded flash memory is read through the HDQ interface. If your specific application or method of use does not involve reading from any location on page 1 or page 2 of flash memory, please disregard this erratum.

Description:

This errata ONLY applies if page 1 (address 0x20– 0x3F) or page 2 (address 0x40– 0x5F) of flash memory is read through the HDQ interface. Under rare conditions, the read operation may return 0xFF data for locations on page 1 or page 2. However, this is only an issue with the READ operation. There is no impact on the content or the integrity of the data stored in page 1 or page 2 of the flash memory.

This document also describes two simple methods of safeguarding against this condition. Both methods are implemented on the host system software. No hardware modifications are required.

Safeguarding Method Number One:

This method ONLY applies if the user does not ever write to any location on page 0 (0x00–0x1F). This method uses a flash to RAM transfer sequence in order to clear any potential read issues.

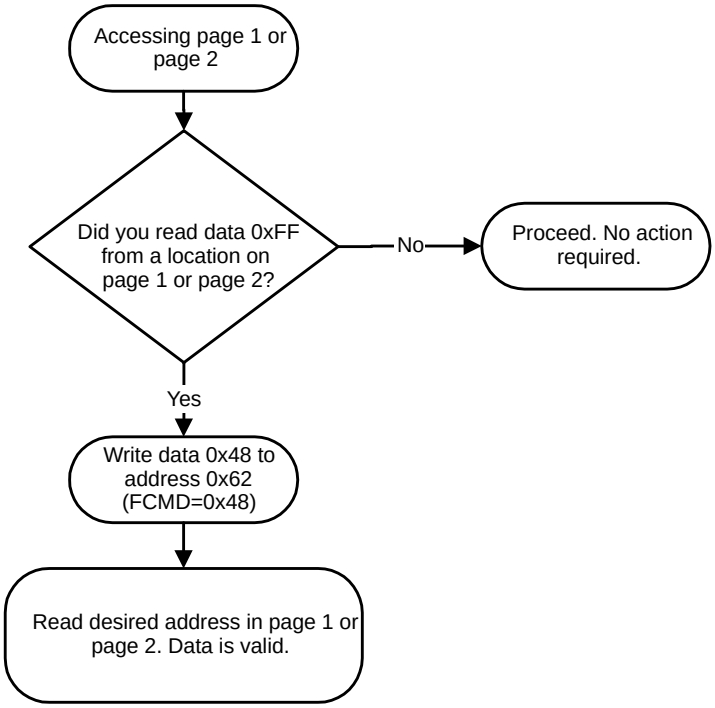


Figure 1. Procedure Flow for Safeguarding Method Number One

Safeguarding Method Number One:

For all applications that write to page 0, please proceed to Safeguarding Method Number Two.

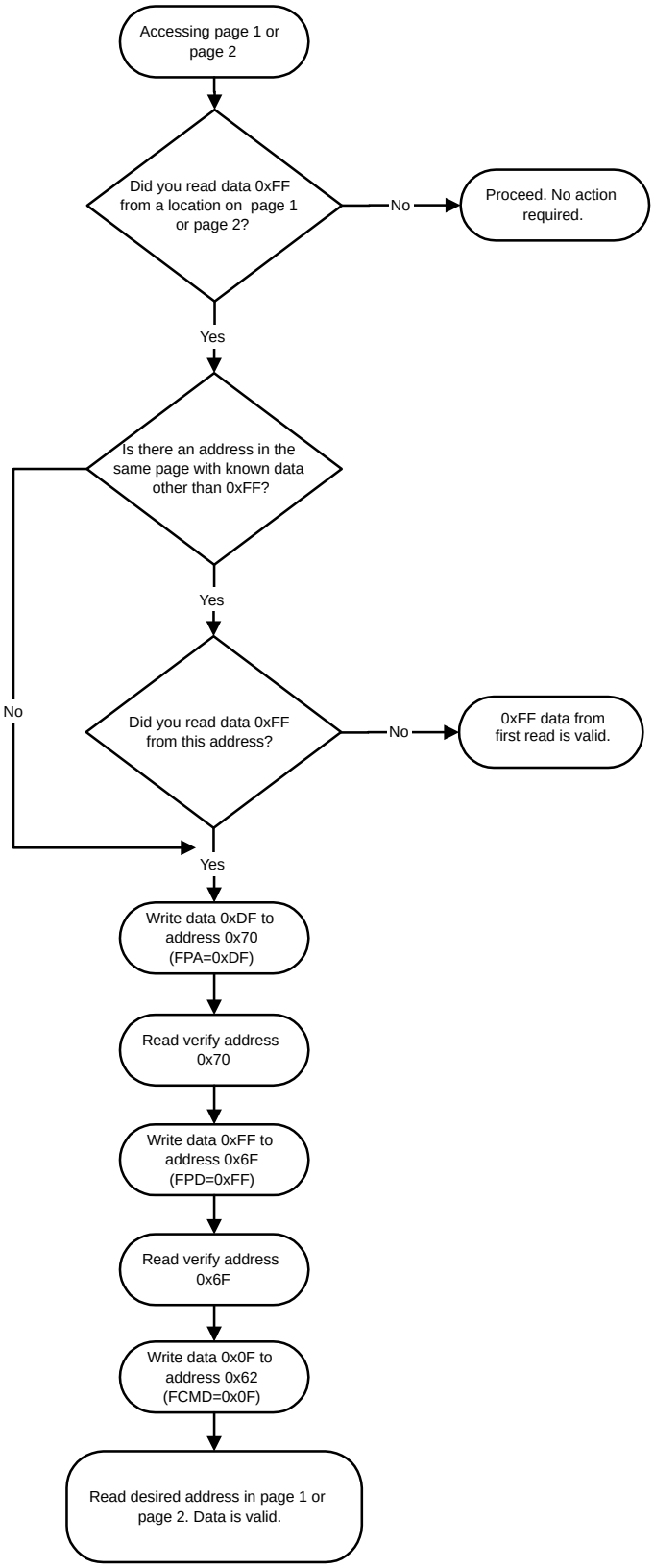


Figure 2. Procedure Flow for Safeguarding Method Number Two

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2019PW	ACTIVE	TSSOP	PW	8	100	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ219	Samples
BQ2019PWG4	ACTIVE	TSSOP	PW	8	100	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ219	Samples
BQ2019PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ219	Samples
BQ2019PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ219	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

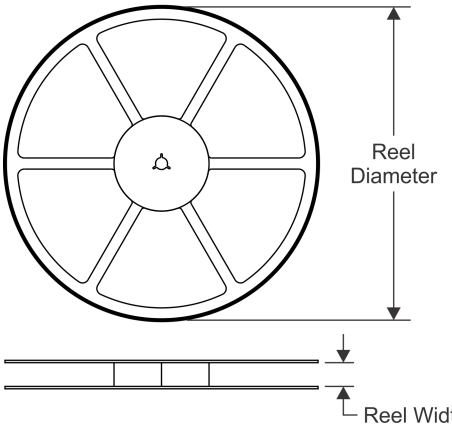
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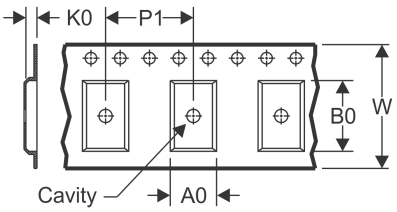
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

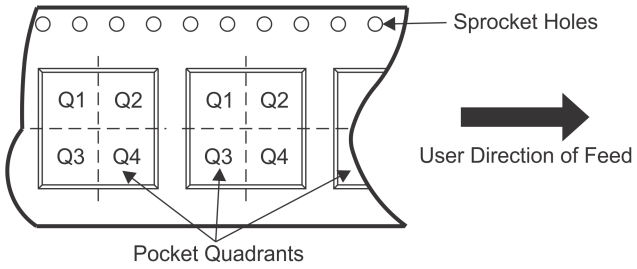


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

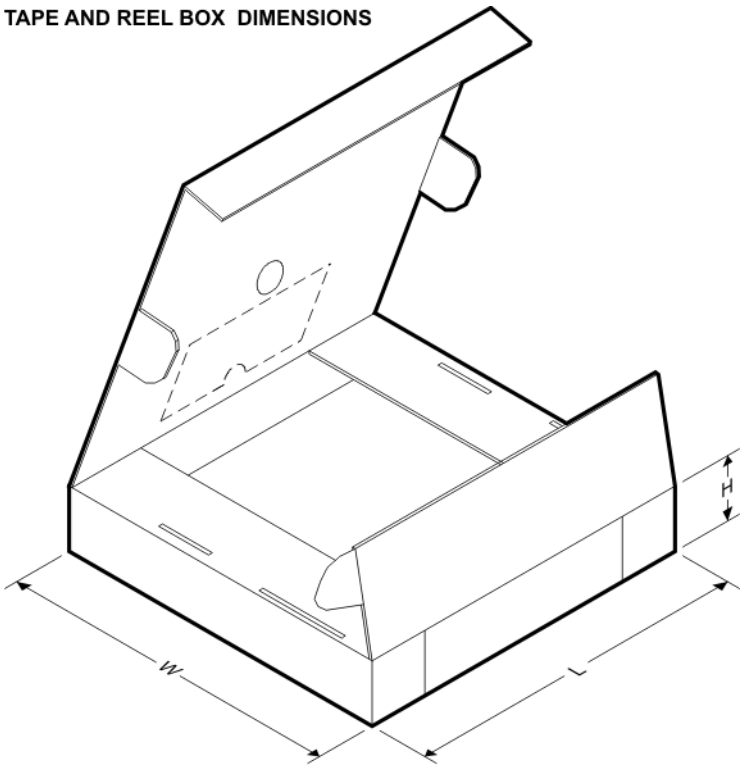
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2019PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

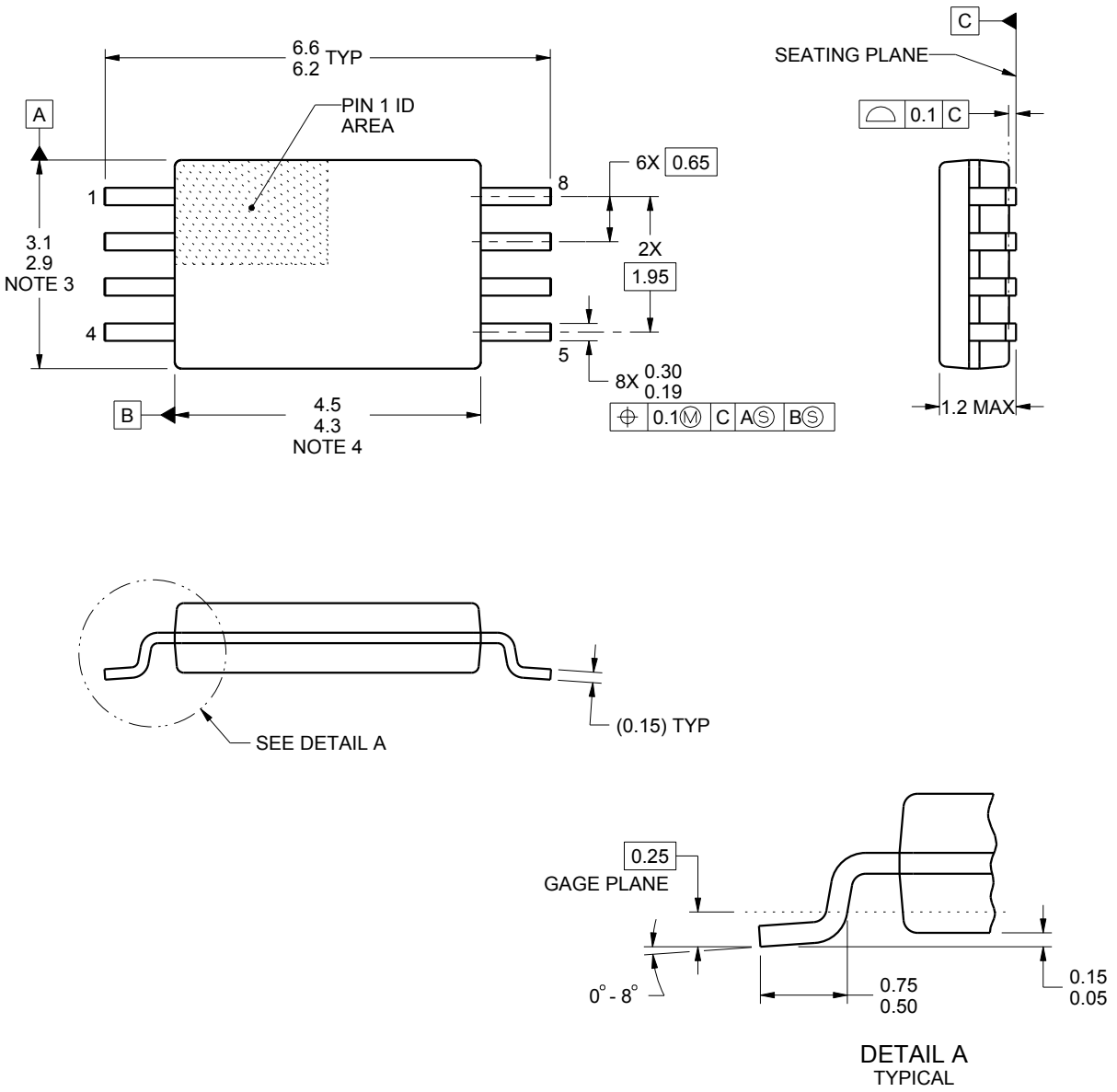
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2019PWR	TSSOP	PW	8	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0008A

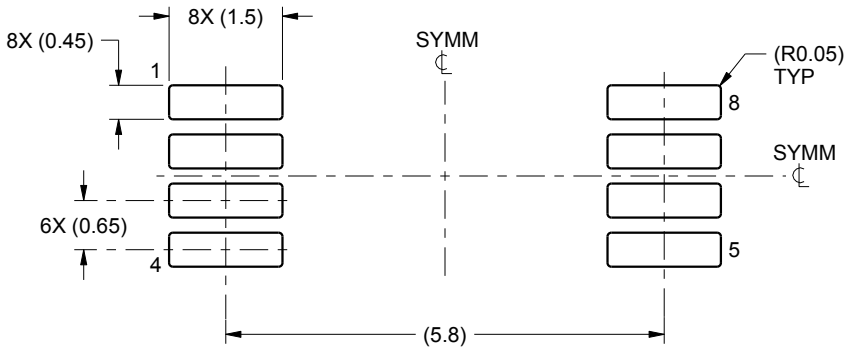
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

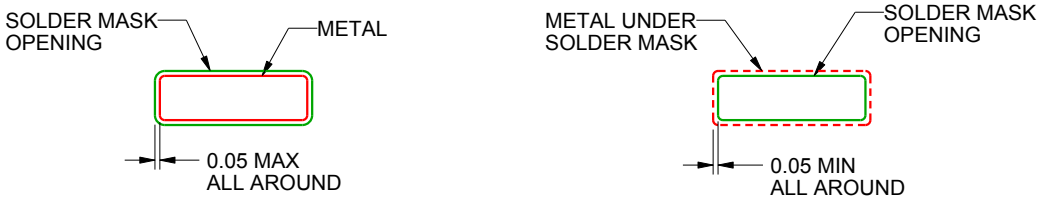


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

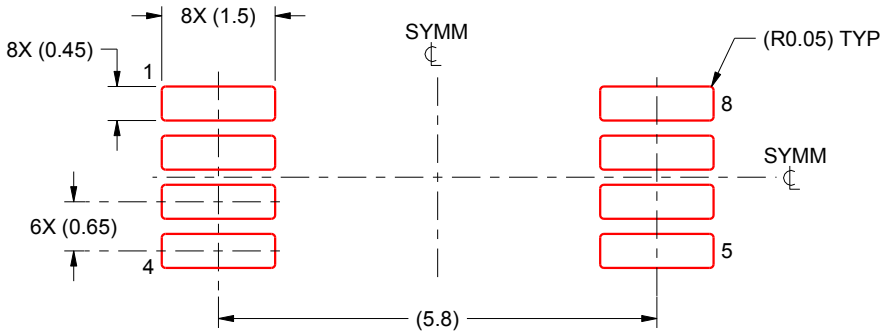


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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