UNITRODE

bq2012

Gas Gauge IC With Slow-Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow SOIC

General Description

The bq2012 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

The bq2012 includes a charge control output that, when used with other full-charge safety termination methods, can provide a cost-effective means of controlling charge based on the battery's charge state.

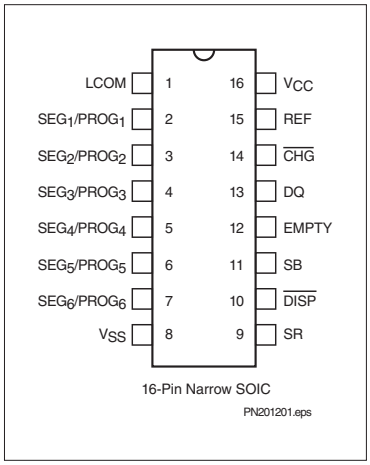
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2012 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2012 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2012 gas gauge data registers.

The bq2012 may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



9/96 B

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
$SEG_6/PROG_6$	LED segment 6/ program 6 input
REF	Voltage reference output
$\overline{CHG}$	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the selfdischarge compensation rate shown in Table 1.

$PROG_6$ **Display mode selection (dual function with SEG_6)**

This three-level pin defines the display operation shown in Table 1.

$\overline{CHG}$ **Charge control output**

This open-drain output becomes active low when charging is allowed. Valid charging conditions are described in the Charge Control section.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop (V_{SRO}) as seen by the bq2012 is $V_{SR} + V_{OS}$ (see Table 5).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq$ -4mV. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2012 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2012 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2012 using the LED display capability as a charge-state indicator. The bq2012 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2012 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

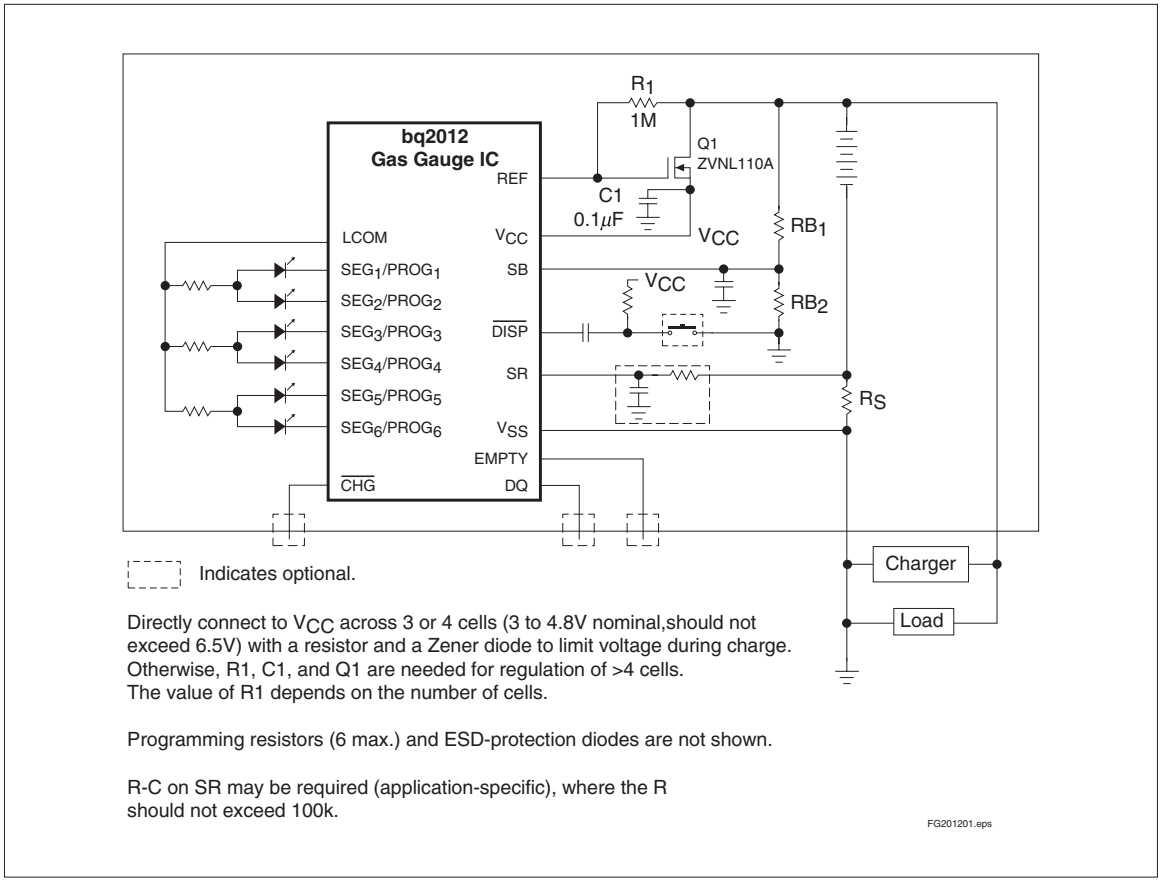


Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2012 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2012 are fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

During discharge and charge, the bq2012 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after $V_{SR} >$ -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs. The bq2012 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2012 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Register Reset section.

Temperature

The bq2012 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2012 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2012.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 100K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2012. The bq2012 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2012 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the programmed full count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2012 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) ∗ sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

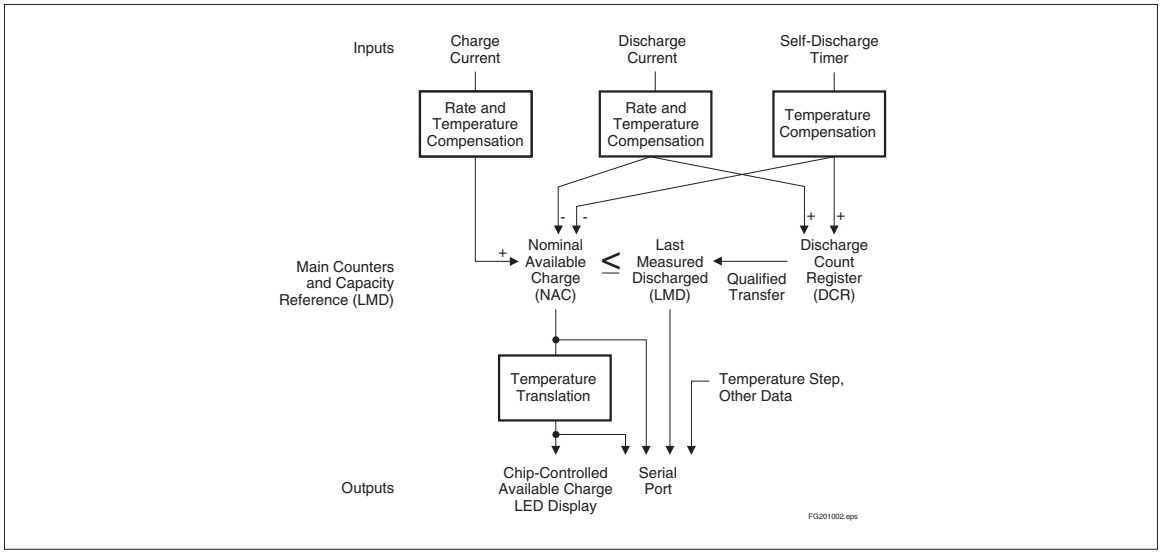


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = $\frac{C}{64}$
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh ∗ 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2012 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2012 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Self-discharge disabled	NAC = PFC on reset	LED disabled
Z	$\frac{NAC}{64}$	Absolute	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	$\frac{NAC}{47}$	Relative	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2012 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} is equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.56	2.8	mV

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization ($PROG_6$ = Z or low) and on reaching EDV1. NAC is set to PFC on initialization if $PROG_6$ = high. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. DCR stops counting when EDV1 is reached. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   No valid charge initiations (charges greater than 256 NAC counts; where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

   The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

   The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2012 increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates the LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2012 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRQ} is 375µV.

Charge Control

Charge control is provided by the $\overline{CHG}$ output. This output is asserted continuously when:

NAC < 0.94 ∗ LMD and
0.95V < V_{SB} < 2.25V and
0°C < Temp < 50°C and
BRM = 0

This output is asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) when the above conditions are not met and:

NAC < LMD and
0.95V < V_{SB} < 2.25V and
Temp < 50°C and
BRM = 0

This output is also asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) for a 2-hour top-off period after:

NAC = LMD and
Temp < 50°C and
0.95V < V_{SB} < 2.25V and
BRM = 0

This output is inactive when:

NAC = LMD (after a 2-hour top-off period) or
Temp > 50°C or
V_{SB} < 0.95V or
V_{SB} > 2.25V or
BRM = 1

The top-off timer (2 hours) is reset to allow another top-off after the battery is discharged to 0.8 ∗ LMD ($PROG_6$ = L) or 0.8 ∗ PFC ($PROG_6$ = Z or H).

Caution: The charge control output ($\overline{CHG}$) should be used with other forms of charge termination such as ΔT/Δt and -ΔV.

If charge terminates due to maximum temperature, the battery temperature must fall typically 10°C below 50°C before the charge output becomes active again.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2012 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{64} * NAC$ or $\frac{1}{47} * NAC$ per day or disabled as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2012 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge are compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Compensation factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150mV < V_{SR} < 0$.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $\frac{1}{64} * NAC$ or $\frac{1}{47} * NAC$ per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	$NAC/256$	$NAC/188$
10–20°C	$NAC/128$	$NAC/94$
20–30°C	$NAC/64$	$NAC/47$
30–40°C	$NAC/32$	$NAC/23.5$
40–50°C	$NAC/16$	$NAC/11.8$
50–60°C	$NAC/8$	$NAC/5.88$

Digital Magnitude Filter

The bq2012 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see DCR description). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2012

The bq2012 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2012 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2012 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2012. The command directs the bq2012 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2012 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2012. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2012 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2012 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2012 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2012 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2012 NAC register.

bq2012 Registers

The bq2012 command and status registers are listed in Table 6 and described in the following sections.

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Table 6. bq2012 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	$\overline{CHG}$	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

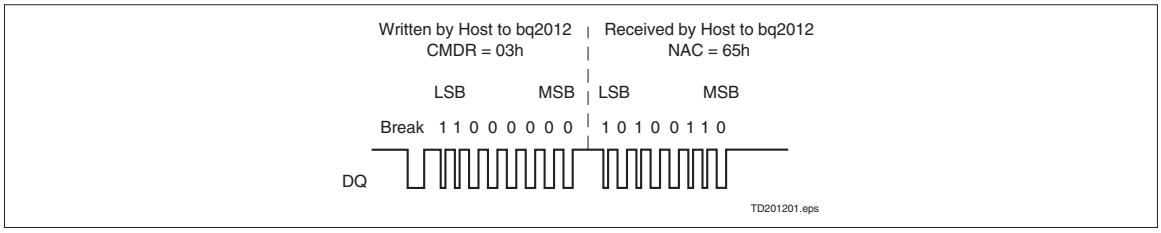


Figure 3. Typical Communication With the bq2012

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2012. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2012 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2012 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2012 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1 V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2012 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2012 is discharged from NAC = LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***charge control*** flag, $\overline{CHG}$, is asserted whenever the $\overline{CHG}$ pin is asserted (see the charge control section on page 7 for a description of the $\overline{CHG}$ pin function).

The $\overline{CHG}$ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	$\overline{CHG}$	-	-

Where $\overline{CHG}$ is:

0 When the $\overline{CHG}$ pin is asserted active low, signifying that the bq2012 is in a state to allow charge activity.

1 When the $\overline{CHG}$ pin is high-impedance, signifying that no charge activity should take place.

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDV1. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2012 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown in Table 7.

The bq2012 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2012. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2012 detects a valid EDV1, NACH and NACL are reset to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2012 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2012. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2012 uses as a measured full reference. The bq2012 adjusts LMD based on the measured discharge capacity

of the battery from full to empty. In this way the bq2012 updates the capacity of the battery. LMD is set to PFC during a bq2012 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2012 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared when V_{SR} > -250mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2012. The segment drivers, $SEG_{1–6}$, have a corresponding PPD register location, $PPD_{1–6}$. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2012. The segment drivers, $SEG_{1–6}$, have a corresponding PPU register location, $PPU_{1–6}$. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2012 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected if NAC < 0.94 ∗ LMD. When NAC ≥ 0.94 ∗ LMD, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC is discharged below 0.94 ∗ LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2012. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2012 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2012.*

Resetting the bq2012 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC when $PROG_6$ = H.

Display

The bq2012 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2012 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with the sixth segment representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the $SEG_{1–6}$ outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or V_{SRO} > V_{SRQ}. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2012 can operate directly from three or four cells. To facilitate the power supply requirements of the bq2012, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2012 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	7.0	V	
All other pins	Relative to V_{SS}	-0.3	7.0	V	
REF	Relative to V_{SS}	-0.3	8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2012 application note for details).
T_{OPR}	Operating temperature	0	70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, $V_{SR} + V_{OS}$ (see note 2)
V_{ORD}	Overload threshold	-230	-250	-280	mV	SR, $V_{SR} + V_{OS}$
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Notes:
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See “LayoutConsiderations.”
2. Proper threshold measurements require V_{CC} to be more than 1.5V greater than the desired signal value.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP}$ = V_{CC}
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY, $\overline{CHG}$
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

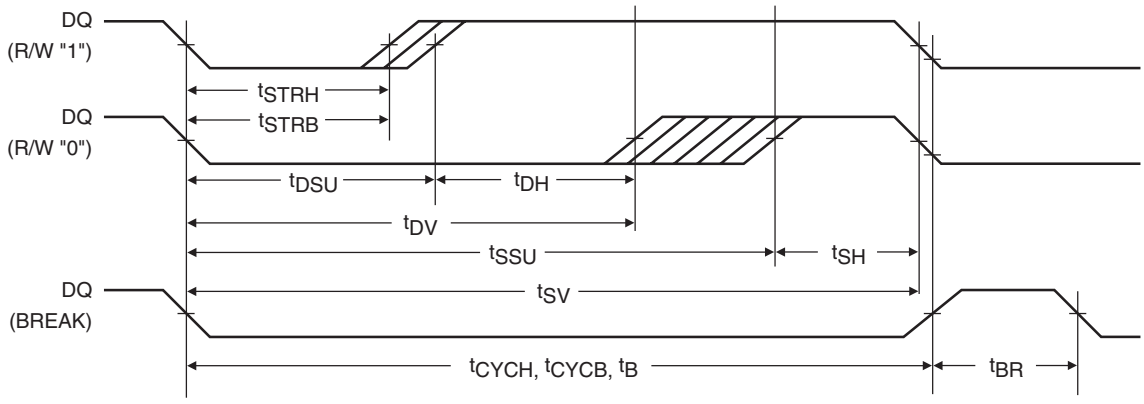
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2012	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2012 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2012	5	-	-	ns	
t_{STRB}	Start hold, bq2012 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

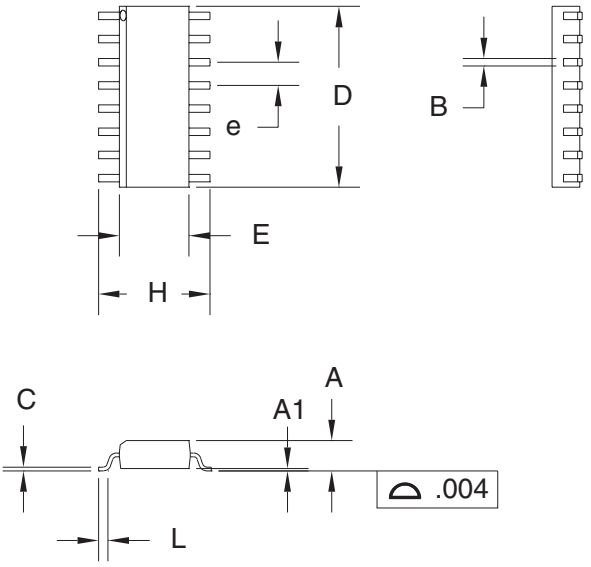
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



TD201002.eps

16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	7	Addition to Table 2	Added bottom row

Note: Change 1 = Sept. 1996 B changes from July 1994.

Ordering Information

bq2012

Temperature Range:
blank = Commercial (0 to +70°C)

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2012 Gas Gauge IC

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2012SN-D107	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2012 D107	Samples
BQ2012SN-D107G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2012 D107	Samples
BQ2012SN-D107TR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2012 D107	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

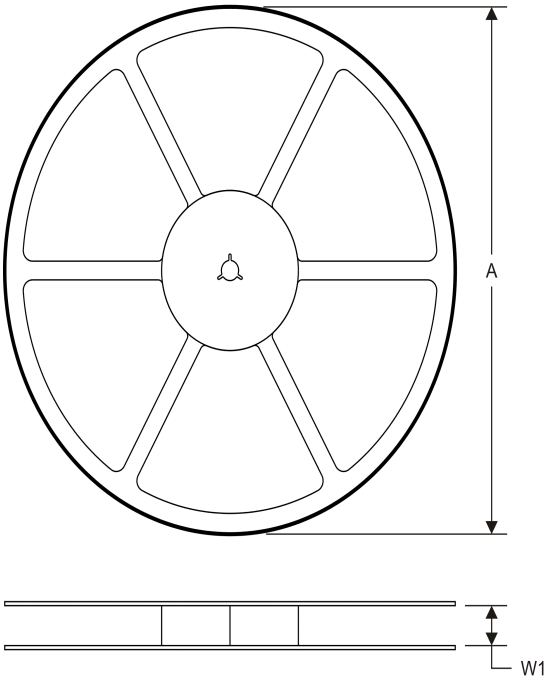
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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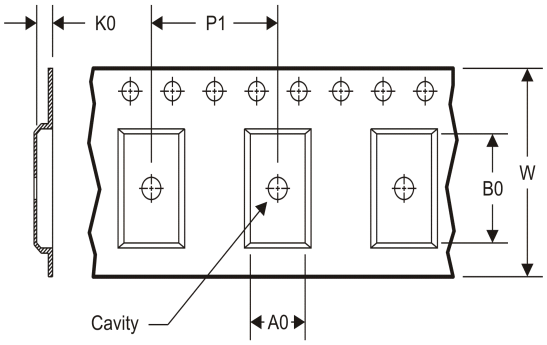
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



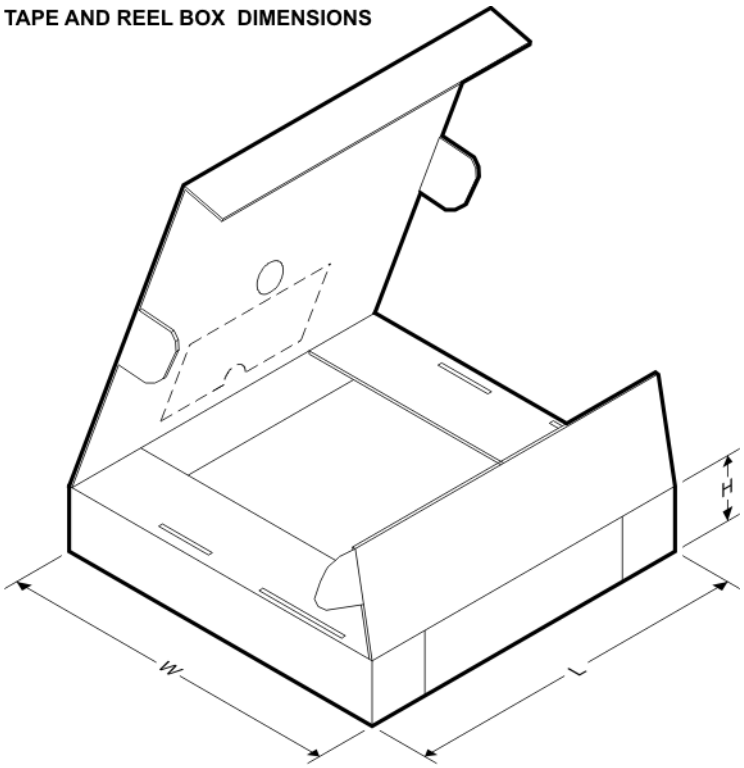
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2012SN-D107TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

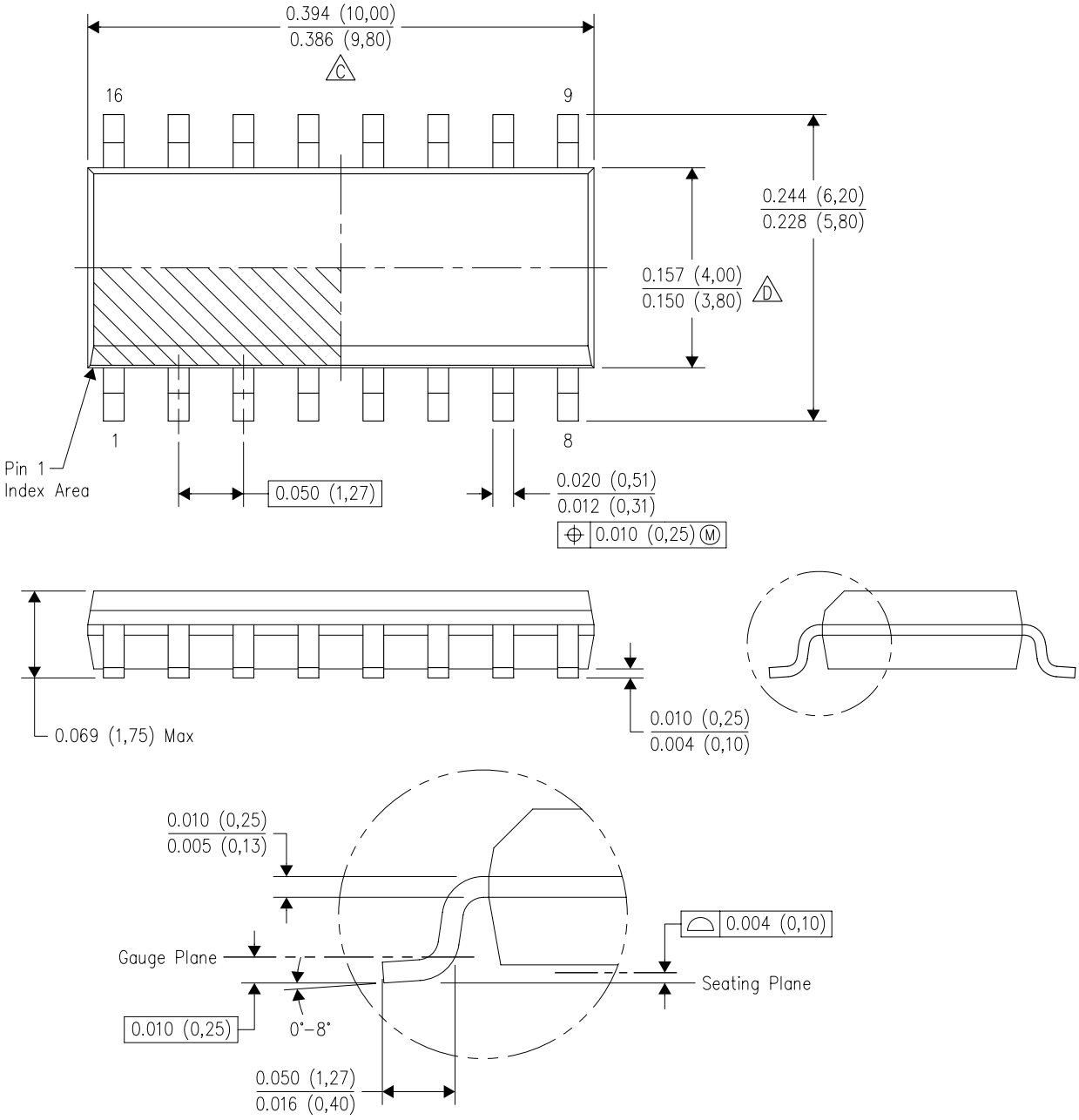
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2012SN-D107TR	SOIC	D	16	2500	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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