DESCRIPTION

The BL8521 is a synchronous, 1.4MHz, fix frequency PWM Buck converter. It is ideal for powering portable equipment that powered by a single cell Lithium-ion batter, or USB port.

The BL8521 can provide up to 3A of load current with output voltage as low as 0.8V. It can operate at 100% duty cycle for low dropout application.

With its peak current mode control and outside compensation, the BL8521 is stable with ceramic capacitors and small inductors.

BL8521 comprises a cycle-by-cycle current limit and thermal shutdown to protect itself from fault application.

BL8521 is available in DFN 3x3 -10 package.

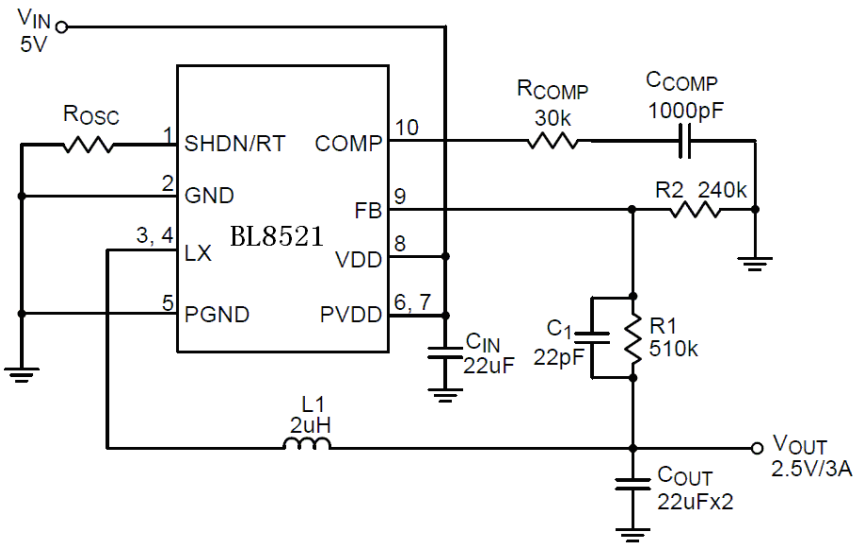
FEATURES

- Adjustable Output Voltage, 0.8 - Vin
- High efficiency, up to 96%
- Output voltage accuracy 2%
- 0.1ohm Rdson of internal MOSFET
- 3A maximum output current
- Up to 1.5MHz fix switching frequency
- 5.5V maximum operation voltage
- Short circuit protection
- Thermal shutdown protection
- 10mV Load regulation at 3A load
- Compatible with ceramic output capacitor
- Excellent load transient performance
- In-rush current suppression
- Reverse current suppression for light load
- Available in DFN3x3-10 package

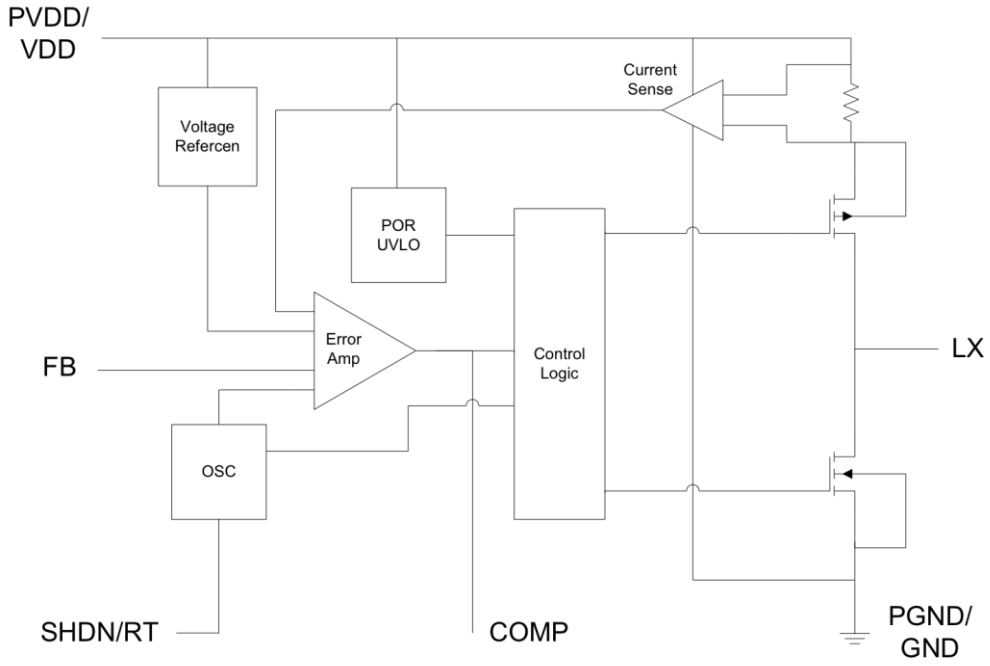
APPLICATIONS

- 3G network modem
- Smart phone, PDA
- Digital camera
- LCDTV
- Portable devices

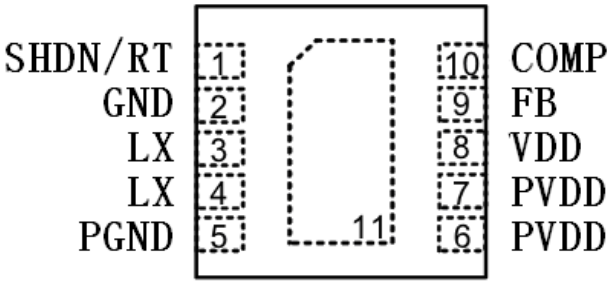
TYPICAL APPLICATION



BLOCK DIAGRAM



PIN CONFIGURATION



DFN3x3-10

PIN NO.	PIN NAME	PIN FUNCTION
1	SHDN/RT	Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency. Forcing this pin to VDD causes the device to be shut down.
2	GND	Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.
3,4	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
5	PGND	Power Ground. Connect this pin close to the negative terminal of CIN and COUT.
6,7	PVDD	Power Input Supply. Decouple this pin to PGND with a capacitor.
8	VDD	Signal Input Supply. Decouple this pin to GND with a capacitor. Normally VDD is equal to PVDD.
9	FB	Feedback Pin. This pin Receives the feedback voltage from a resistive divider connected across the output.
10	COMP	Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.

ABSOLUTE MAXIMUM RATING

Supply Input Voltage, VDD, PVDD ---------- –0.3V to 6V
LX Pin Switch Voltage ---------- –0.3V to (PVDD + 0.3V)
Other I/O Pin Voltages ---------- –0.3V to (VDD + 0.3V)
LX Pin Switch Current ---------- 3.5A
Power Dissipation, P_D @ T_A = 25°C ,DFN-10L 3x3 ---------- 900mW
Package Thermal Resistance,DFN-10L3x3, θ_{JA} ---------- 110°C/W
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- –65°C to 150°C
ESD HBM (Human Body Mode) ---------- 2kV

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage ---------- 3.6 to 5.5V
Output Voltage Range ----------0.8V to Vin
Junction Temperature Range ---------- –40°C to 125°C
Ambient Temperature Range ---------- –40°C to 85°C

ELECTRICAL CHARACTERISTICS

(VDD=5V, T_A=25°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD_Max	Maximum Input Voltage			5.5		V
I_{IN}	Supply Current	Vfb=0.9		500	1000	μA
		In Shutdown			1	μA
LSON	Low side NMOS Rdson			100	200	mΩ
HSON	High side PMOS Rdson			100	220	mΩ
Vref	Feedback Voltage		0.784	0.8	0.816	V
Ifb	Feedback Leakage current		-5	0.1	5	μA
REGlin	Line Regulation	Vin=4V to 5.5V	0	0.1	0.3	%/V
REGload	Load Regulation	Iout=1 to 3A	0	0.03	0.1	%/A
Fsoc	Switching Frequency	R_{RT}=180K	1.44	1.8	2.16	MHz
		R_{RT}=330K	0.86	1.15	1.44	MHz
Ilimit	Peak Current Limit		3.2	4		A
SHDN_V	Shutdown Voltage		Vin-0.7V		Vin	V
UVLO_rise	Power on minimum Vin voltage	Increase Vin until IC work	3.42	3.6	3.78	V
UVLO_fall	Power off Vin under voltage lock out	Decrease Vin until IC shut off	1.98		2.37	V

APPLICATION INFORMATION

The basic BL8521 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Output Voltage Programming

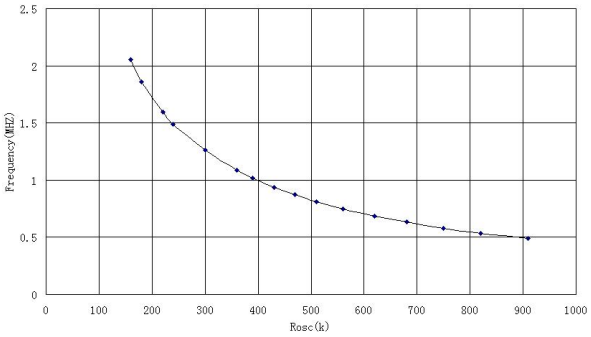
The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = V_{REF} \times (1 + R1/R2),$$

where V_{REF} equals to 0.8V typical.

RT Pin Resistor Selection to set Frequency

The resistor connected between RT pin and Gnd is used to set the oscillation frequency of BL8521. The relation between RT resistor and frequency is shown below:



Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current $\otimes I_L$ increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I = [V_{OUT}/(f \times L)] \times [1 - V_{OUT}/V_{IN}]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is $\otimes I = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = [V_{OUT}/f \times \Delta I_{L(MAX)}] \times [1 - V_{OUT}/V_{IN(MAX)}]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded.

This results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling

requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. δI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The COMP pin external components and output capacitor shown in Typical Application Circuit will provide adequate compensation for most applications.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement.

Efficiency can be expressed as :
Efficiency = 100% – (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{DD} quiescent current and I^2R losses.

The V_{DD} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load current. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{DD} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge δQ moves from V_{DD} to ground. The resulting $\delta Q/\delta t$ is the current out of V_{DD} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(QT+QB)$ where QT and QB are the gate charges of the internal top and bottom switches.

Both the DC bias and gate charge losses are proportional to V_{DD} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, RSW and external inductor RL. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows :

$R_{SW} = R_{DS(ON)}TOP \times D + R_{DS(ON)}BOT \times (1"D)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add RSW to RL and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and

inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the BL8521 does not dissipate much heat due to its high efficiency. But, in applications where it is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of The temperature rise is given by: $T_R = P_D \times \theta_{JA}$ Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by :
$T_J = T_A + T_R$ Where T_A is the ambient temperature.

As an example, consider the BL8521 in dropout at an input voltage of 3.3V, a load current of 2A and an ambient temperature of 70°C. The $R_{DS(ON)}$ of the P-Channel switch at 70°C is approximately 121m∧. Therefore, power dissipated by the part the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance. To avoid the BL8521 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part.

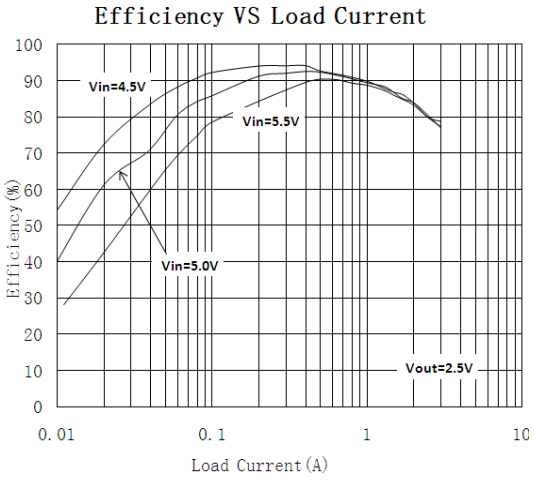
is :
$P_D = (I_{LOAD})_2 (R_{DS(ON)}) = (2A)^2 (121m\wedge) = 0.484W$

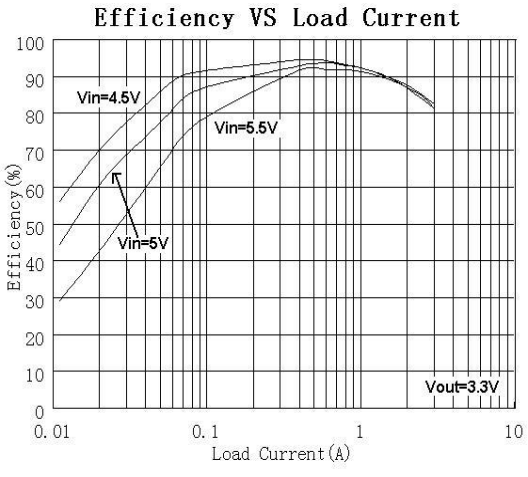
For the DFN3x3 package, the θ_{JA} is 110°C /W. Thus the junction temperature of the regulator is :
TJ = 70°C + (0.484W) (110°C /W) = 123.24°C
Which is below the maximum junction temperature of 125°C.

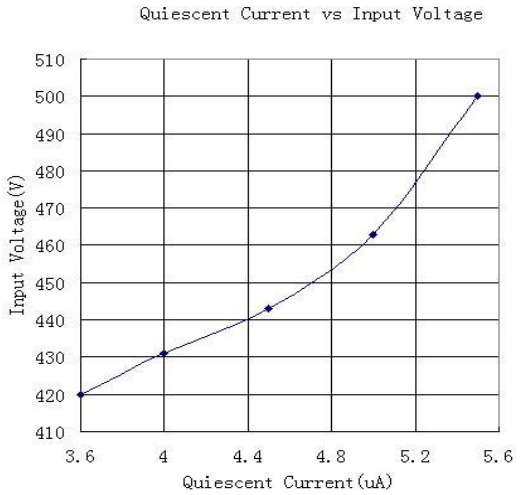
Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

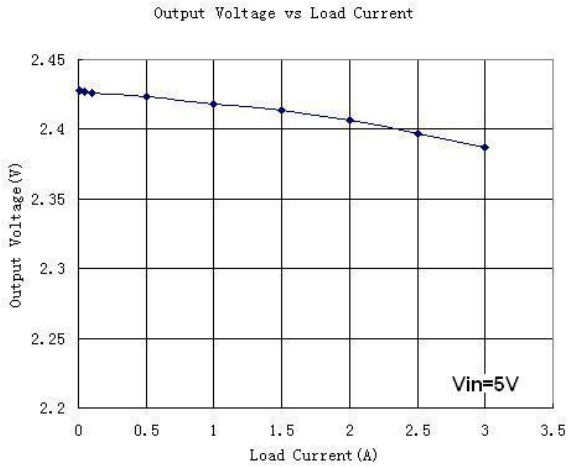
ELECTRICAL PERFOMANCE

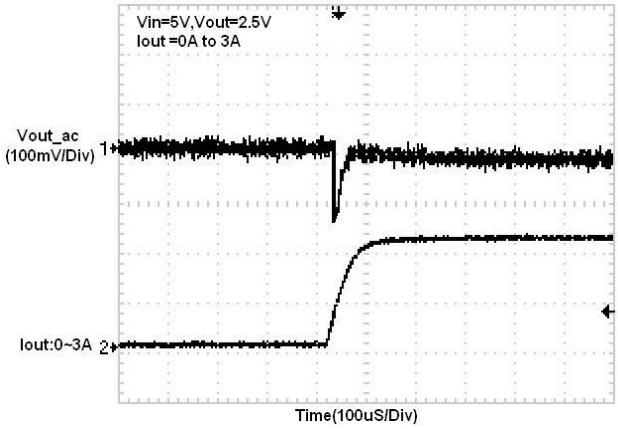
(VDD=5V, VOUT=2.5V, T_A=25°C, unless otherwise specified)

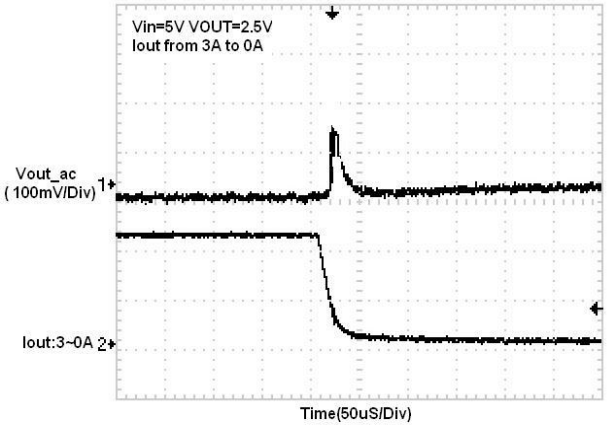


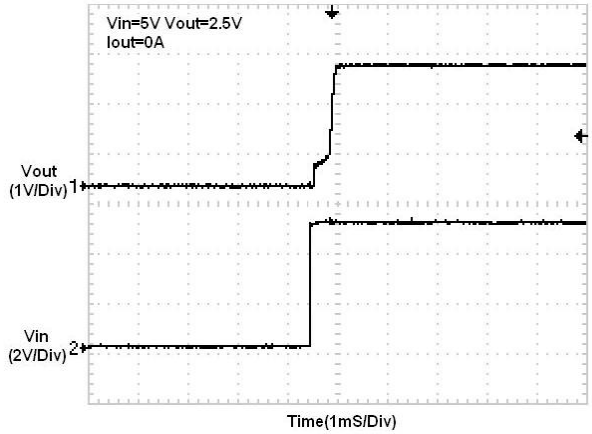


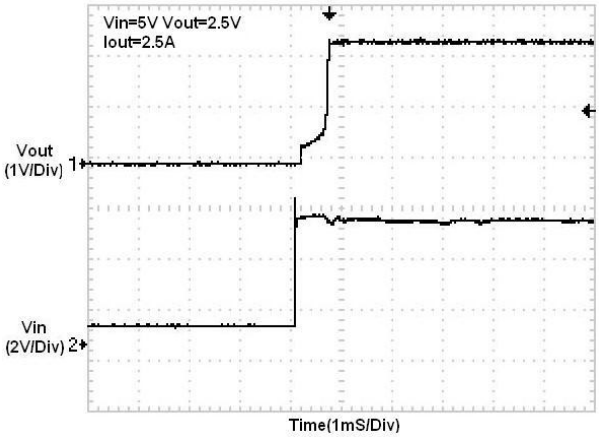

Quiescent Current vs Input Voltage
Input Voltage(V)
510
500
490
480
470
460
450
440
430
420
410
3.6
4
4.4
4.8
5.2
5.6
Quiescent Current(uA)


Output Voltage vs Load Current
Output Voltage(V)
2.45
2.4
2.35
2.3
2.25
2.2
Vin=5V
0
0.5
1
1.5
2
2.5
3
3.5
Load Current(A)


Vin=5V,Vout=2.5V
Iout =0A to 3A
Vout_ac
(100mV/Div) 1
Iout:0~3A 2
Time(100uS/Div)

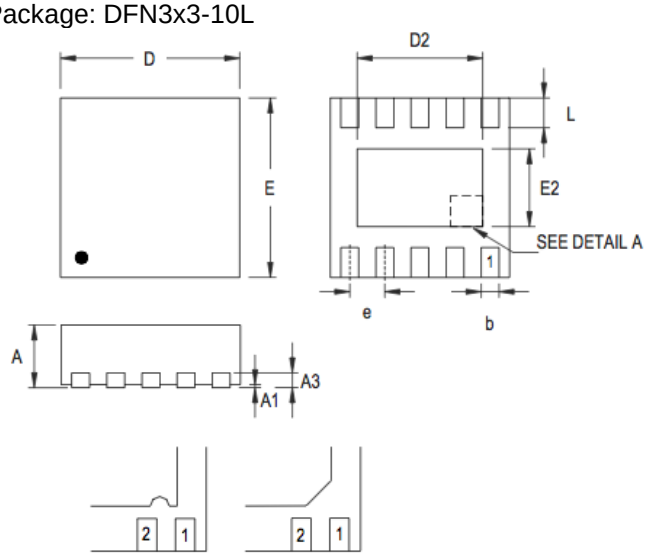

Vin=5V VOUT=2.5V
Iout from 3A to 0A
Vout_ac
(100mV/Div) 1
Iout:3~0A 2
Time(50uS/Div)


Vin=5V Vout=2.5V
Iout=0A
Vout
(1V/Div) 1
Vin
(2V/Div) 2
Time(1mS/Div)


Vin=5V Vout=2.5V
Iout=2.5A
Vout
(1V/Div) 1
Vin
(2V/Div) 2
Time(1mS/Div)

PACKAGE DIMENSION

Package: DFN3x3-10L



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Symbol	Dimensions in Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018