



BGS8L5

SiGe:C low-noise amplifier MMIC with bypass switch for LTE

Rev. 1 — 2 March 2018

Product data sheet

1 General description

The BGS8L5 is a Low-Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a small plastic 6-pin thin leadless package.

The BGS8L5 delivers system-optimized gain for diversity applications where sensitivity improvement is required. The high linearity of this low noise device ensures the required receive sensitivity independent of cellular transmit power level in Frequency Division Duplex (FDD) systems. When receive signal strength is sufficient, the BGS8L5 can be switched off to operate in bypass mode at increased IP_{3i} level. Supply current is 1 μ A, to lower power consumption. The BGS8L5 is internally AC coupled and requires only one external matching inductor.

The BGS8L5 is optimized for 617 MHz to 960 MHz.

2 Features and benefits

- Operating frequency from 617 MHz to 960 MHz
- Noise figure = 0.8 dB
- Gain 13.7 dB
- High input 1 dB compression point of -4.5 dBm
- High in band IP_{3i} of -1 dBm
- Bypass switch insertion loss of 2.1 dB
- Supply voltage 1.5 V to 3.1 V
- Integrated RF supply decoupling
- Optimized performance at a supply current of 4.9 mA
- Bypass mode current consumption < 1 μ A
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and output AC coupled through DC blocking capacitors
- Integrated matching for the output
- ESD protection on all pins
- Low Bill of Materials (BOM)
- 6 pins leadless package: 1.1 mm x 0.7 mm x 0.37 mm: 0.40 mm pitch
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level of 1



3 Applications

- LNA for LTE reception in smart phones
- feature phones
- tablet PCs
- RF front-end modules

4 Quick reference data

Table 1. Quick reference data

$f = 882\text{ MHz}$; $V_{CC} = 2.8\text{ V}$; $V_{I(CTRL)} > 0.8\text{ V}$; $T_{amb} = 25\text{ °C}$. Input matched to $50\text{ }\Omega$ using application diagram from [Figure 3](#) and component values as in [Table 10](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	in gain mode	-	4.9	6.0	mA
		in bypass mode	-	-	1	μA
G_p	power gain	in gain mode	-	13.7	-	dB
		in bypass mode	-	-2.1	-	dB
NF	noise figure	[1]	-	0.8	-	dB
$P_{I(1\text{ dB})}$	input power at 1 dB gain compression		-	-4.5	-	dBm
$IP3_i$	input third-order intercept point	$\Delta f = 1\text{ MHz}$	-	-1.0	-	dBm

[1] PCB losses are subtracted

5 Ordering information

Table 2. Ordering information

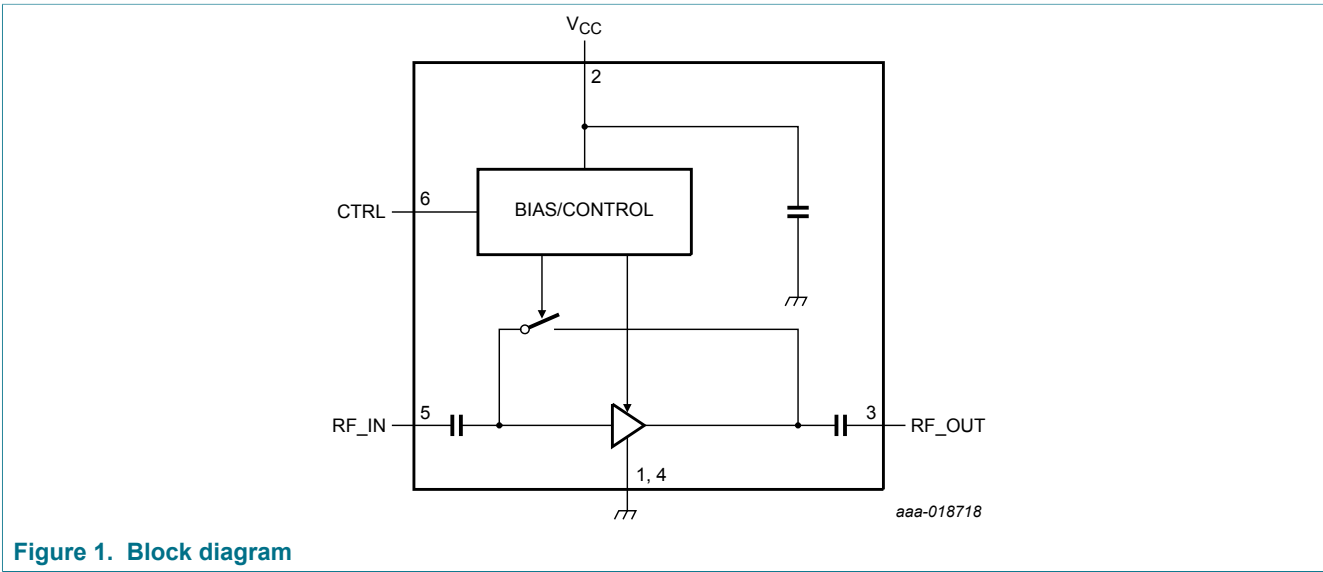
Type number	Package		
	Name	Description	Version
BGS8L5	XSON6	plastic extremely thin small outline package: no leads; 6 terminals; body 1.1. x 0.7 x 0.37 mm	SOT1232

6 Marking

Table 3. Marking codes

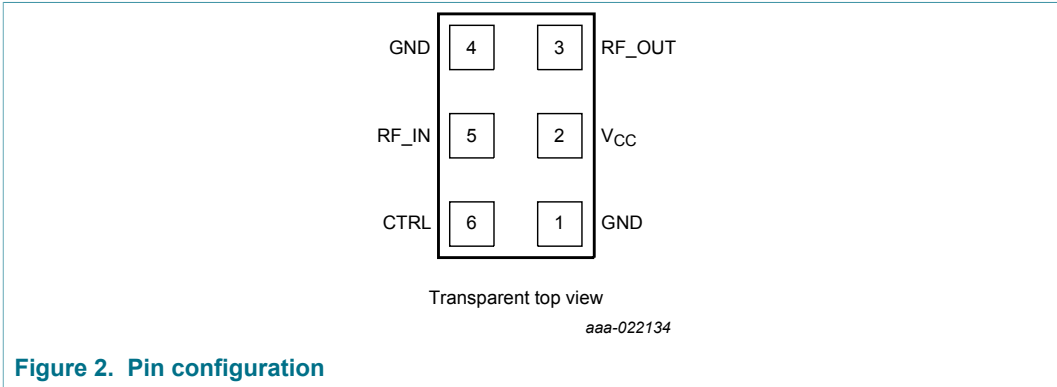
Type number	Marking code
BGS8L5	S

7 Block diagram



8 Pinning information

8.1 Pinning



8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
1	GND	RF ground
2	V _{CC}	supply voltage
3	RF_OUT	RF output
4	GND	RF ground
5	RF_IN	RF input
6	CTRL	gain control, switch between gain and bypass mode

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+5.0	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6 \text{ V}$	-0.5	+5.0	V
$V_{I(RF_IN)}$	input voltage on pin RF_IN	DC [1]	-0.5	+0.6	V
$V_{I(RF_OUT)}$	input voltage on pin RF_OUT	DC, $V_{I(RF_OUT)} < V_{CC} + 0.6 \text{ V}$ [1]	-0.5	+5.0	V
P_i	input power	RF	-	26	dBm
		[2]	-	23	dBm
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	+150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001 [3]	-	±2	kV
		Charged Device Model (CDM) according to ANSI/ESDA/JEDEC Standard JS-002	-	±1	kV

[1] The RF input and output are AC coupled through internal DC Blocking capacitors.

[2] $f = 880 \text{ MHz}$, 200 Hrs at $T_{amb} = 100 \text{ °C}$

[3] HBM ESD protection level is according to JS-001 Classification 2 (2000 V to < 4000 V)

10 Operating conditions

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		-40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	bypass mode	-	-	0.25	V
		gain mode	0.8	-	-	V

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

12 Characteristics

Table 8. Characteristics

703 MHz ≤ f ≤ 960 MHz; V_{CC} = 1.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from [Figure 3](#) and component values as in [Table 10](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain Mode						
I _{CC}	supply current	V _{I(CTRL)} > 0.8 V	-	4.7	6.0	mA
G _p	power gain	f = 637 MHz	-	15.5	-	dB
		f = 740 MHz	-	14.5	-	dB
		f = 882 MHz	-	13.5	-	dB
		f = 943 MHz	-	13.0	-	dB
ΔG/ΔT	gain variation with temperature		-	-0.01	-	dB/°C
NF	noise figure	f = 637 MHz [1]	-	0.8	-	dB
		f = 740 MHz [1]	-	0.8	-	dB
		f = 882 MHz [1]	-	0.8	-	dB
		f = 943 MHz [1]	-	0.85	-	dB
P _{I(1dB)}	input power at 1 dB gain compression	f = 637 MHz	-	-10	-	dBm
		f = 740 MHz	-	-9	-	dBm
		f = 882 MHz	-	-8	-	dBm
		f = 943 MHz	-	-7	-	dBm
IP _{3i}	input third-order intercept point	f = 637 MHz, Δf = 1 MHz	-	-3	-	dBm
		f = 740 MHz, Δf = 1 MHz	-	-2	-	dBm
		f = 882 MHz, Δf = 1 MHz	-	-1	-	dBm
		f = 943 MHz, Δf = 1 MHz	-	0	-	dBm
RL _{in}	input return loss	f = 637 MHz	-	14	-	dB
		f = 740 MHz	-	10	-	dB
		f = 882 MHz	-	15	-	dB
		f = 943 MHz	-	16	-	dB
RL _{out}	output return loss	f = 637 MHz	-	9	-	dB
		f = 740 MHz	-	10	-	dB
		f = 882 MHz	-	9	-	dB
		f = 943 MHz	-	9	-	dB

SiGe:C low-noise amplifier MMIC with bypass switch for LTE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ISL	isolation	f = 637 MHz	-	23	-	dB
		f = 740 MHz	-	23	-	dB
		f = 882 MHz	-	23	-	dB
		f = 943 MHz	-	23	-	dB
K	Rollett stability factor		1	-	-	
t _{on}	turn-on time	Time from V _{I(CTRL)} ON, to 90 % of the gain	-	-	4	μs
t _{off}	turn-off time	Time from V _{I(CTRL)} OFF, to 10 % of the gain	-	-	1	μs
Bypass Mode						
I _{CC}	supply current	V _{I(CTRL)} < 0.25 V	-	-	1.0	μA
G _p	power gain	f = 637 MHz	-	-2.0	-	dB
		f = 740 MHz	-	-2.0	-	dB
		f = 882 MHz	-	-2.2	-	dB
		f = 943 MHz	-	-2.5	-	dB
RL _{in}	input return loss	f = 637 MHz	-	11	-	dB
		f = 740 MHz	-	13	-	dB
		f = 882 MHz	-	10	-	dB
		f = 943 MHz	-	9	-	dB
RL _{out}	output return loss	f = 637 MHz	-	7	-	dB
		f = 740 MHz	-	9	-	dB
		f = 882 MHz	-	8	-	dB
		f = 943 MHz	-	7	-	dB

[1] PCB losses are subtracted.

Table 9. Characteristics

703 MHz ≤ f ≤ 960 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from [Figure 3](#) and component values as in [Table 10](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain Mode						
I _{CC}	supply current	V _{I(CTRL)} > 0.8 V	-	4.9	6.0	mA
G _p	power gain	f = 637 MHz	-	15.7	-	dB
		f = 740 MHz	-	14.7	-	dB
		f = 882 MHz	-	13.7	-	dB
		f = 943 MHz	-	13.1	-	dB
ΔG/ΔT	gain variation with temperature		-	-0.01	-	dB/°C
NF	noise figure	f = 637 MHz [1]	-	0.8	-	dB
		f = 740 MHz [1]	-	0.8	-	dB
		f = 882 MHz [1]	-	0.8	-	dB
		f = 943 MHz [1]	-	0.85	-	dB
P _{I(1dB)}	input power at 1 dB gain compression	f = 637 MHz	-	-5.0	-	dBm
		f = 740 MHz	-	-4.5	-	dBm
		f = 882 MHz	-	-4.5	-	dBm
		f = 943 MHz	-	-4.5	-	dBm
IP3 _i	input third-order intercept point	f = 637 MHz, Δf = 1 MHz	-	-3	-	dBm
		f = 740 MHz, Δf = 1 MHz	-	-2	-	dBm
		f = 882 MHz, Δf = 1 MHz	-	-1	-	dBm
		f = 943 MHz, Δf = 1 MHz	-	0	-	dBm
RL _{in}	input return loss	f = 637 MHz	-	14	-	dB
		f = 740 MHz	-	10	-	dB
		f = 882 MHz	-	16	-	dB
		f = 943 MHz	-	17	-	dB
RL _{out}	output return loss	f = 637 MHz	-	9	-	dB
		f = 740 MHz	-	10	-	dB
		f = 882 MHz	-	9	-	dB
		f = 943 MHz	-	9	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ISL	isolation	f = 637 MHz	-	23	-	dB
		f = 740 MHz	-	23	-	dB
		f = 882 MHz	-	23	-	dB
		f = 943 MHz	-	23	-	dB
K	Rollett stability factor		1	-	-	-
t _{on}	turn-on time	Time from V _{I(CTRL)} ON, to 90 % of the gain	-	-	4	µs
t _{off}	turn-off time	Time from V _{I(CTRL)} OFF, to 10 % of the gain	-	-	1	µs
Bypass Mode						
I _{CC}	supply current	V _{I(CTRL)} < 0.25 V	-	-	1.0	µA
G _p	power gain	f = 637 MHz	-	-1.9	-	dB
		f = 740 MHz	-	-1.8	-	dB
		f = 882 MHz	-	-2.1	-	dB
		f = 943 MHz	-	-2.4	-	dB
RL _{in}	input return loss	f = 637 MHz	-	11	-	dB
		f = 740 MHz	-	13	-	dB
		f = 882 MHz	-	10	-	dB
		f = 943 MHz	-	9	-	dB
RL _{out}	output return loss	f = 637 MHz	-	7	-	dB
		f = 740 MHz	-	9	-	dB
		f = 882 MHz	-	8	-	dB
		f = 943 MHz	-	7	-	dB

[1] PCB losses are subtracted.

13 Application information

13.1 LTE LNA

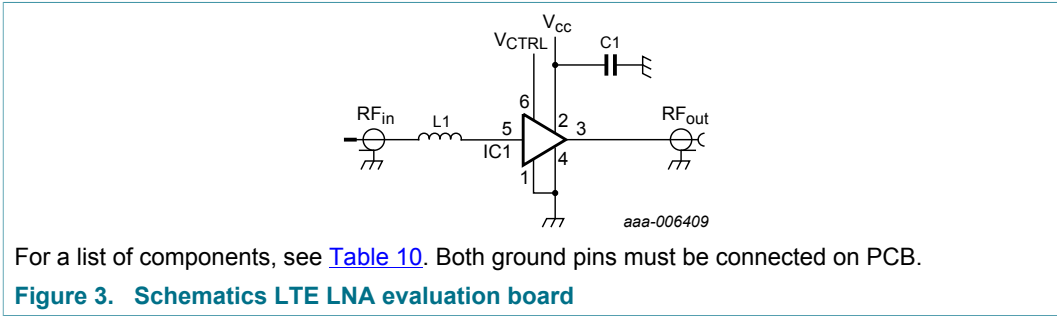


Table 10. List of components

For schematics, see [Figure 3](#)

Component	Description	Value	Remarks
C ₁	decoupling capacitor	1 μF	The total capacitance on the V _{CC} node must be at least 1 μF. It must be positioned at a short distance from the V _{CC} pin (preferably within 15 mm). Typically, such capacitance is already present at the output of the V _{CC} voltage regulator.
IC1	BGS8L5		NXP
L1	high-quality matching inductor	15 nH	617 < f < 652 MHz Murata LQW15A
		8.7 nH	703 < f < 960 MHz Murata LQW15A

14 Package outline

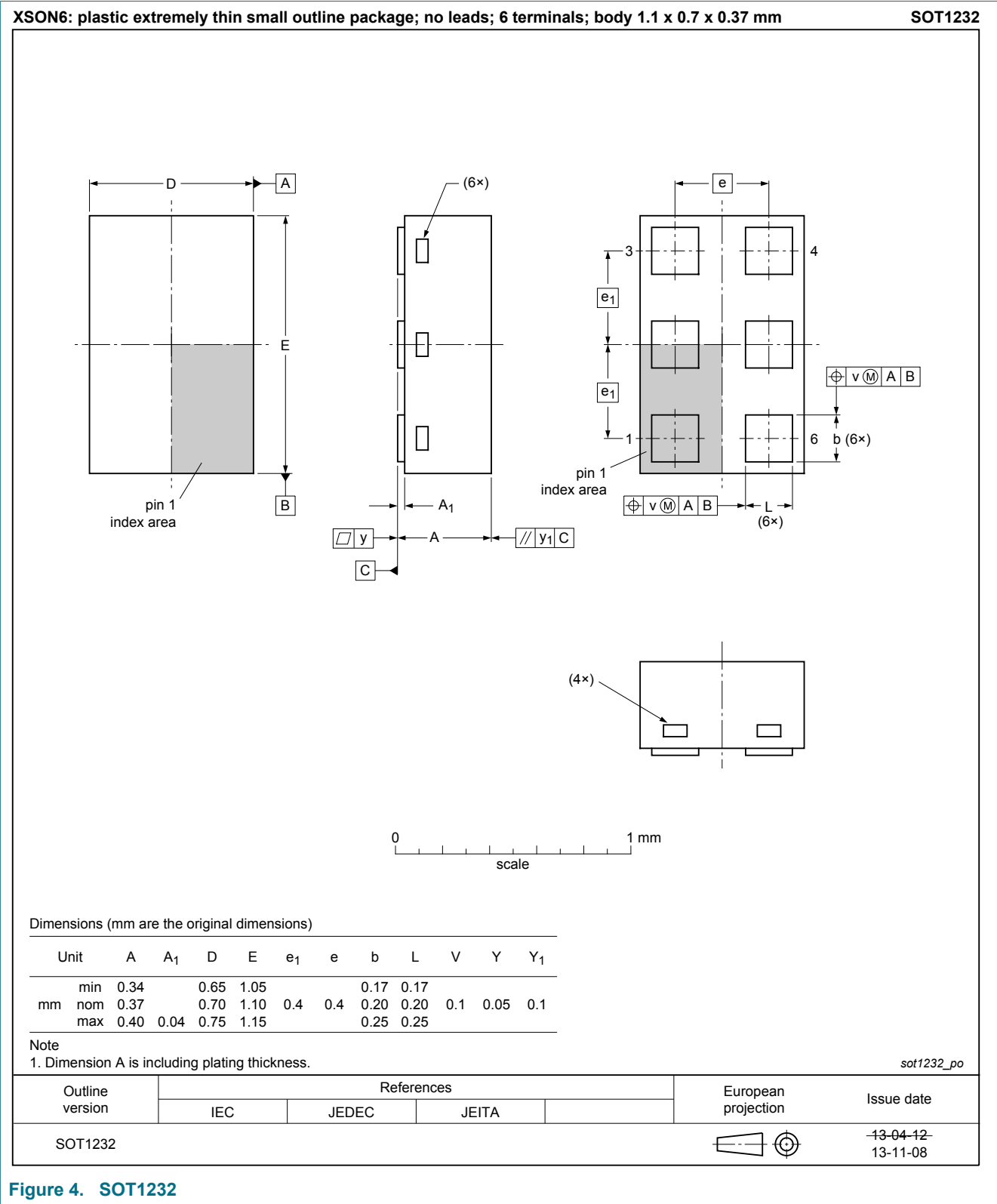


Figure 4. SOT1232

15 Handling information

Table 11. Caution

	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.
---	--

16 Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
MMIC	Monolithic Microwave Integrated Circuit
MUF	Molded Underfill
LTE	Long-Term Evolution
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon

17 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8L5 v.1	20180302	product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for

such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Quick reference data	2
5	Ordering information	2
6	Marking	3
7	Block diagram	3
8	Pinning information	4
8.1	Pinning	4
8.2	Pin description	4
9	Limiting values	5
10	Operating conditions	5
11	Thermal characteristics	5
12	Characteristics	6
13	Application information	10
13.1	LTE LNA	10
14	Package outline	11
15	Handling information	12
16	Abbreviations	12
17	Revision history	12
18	Legal information	13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2018.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 2 March 2018
Document identifier: BGS8L5