Synchronous Buck Converter Integrated FET

BD9109FVM-LB

General Description

This is the product guarantees long time support in Industrial market.

ROHM's high efficiency step-down switching regulators (BD9109FVM-LB) is a power supply designed to produce a low voltage including 3.3 volts from 5 volts power supply line. Offers high efficiency with our original pulse skip control technology and synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

Features

- Long Time Support Product for Industrial Applications.
- Fast Transient Response with Current Mode PWM Control System.
- Highly Efficiency with Synchronous Rectifier (Nch/Pch FET) and SLLM™ (Simple Light Load Mode)
- Soft-Start Function.
- Thermal Protection and ULVO Functions.
- Short-Current Protection Circuit with Time Delay Function.
- Shutdown Function

Applications

- Industrial Equipment
- Power supply for LSI including DSP, Micro computer and ASIC
- Secondary Power Supply

Key Specifications

- Input Voltage Range: 4.5V to 5.5V
- Output Voltage Range: 3.30V ± 2%
- Output Current: 0.8A(Max)
- Switching Frequency: 1MHz(Typ)
- Pch FET On Resistance: 350m(Typ)
- Nch FET On Resistance: 250m(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -25°C to +85°C

Package

	W(Typ) x D(Typ) x H(Max)
MSOP8	2.90mm x4.00mm x 0.90mm



MSOP8

Typical Application Circuit

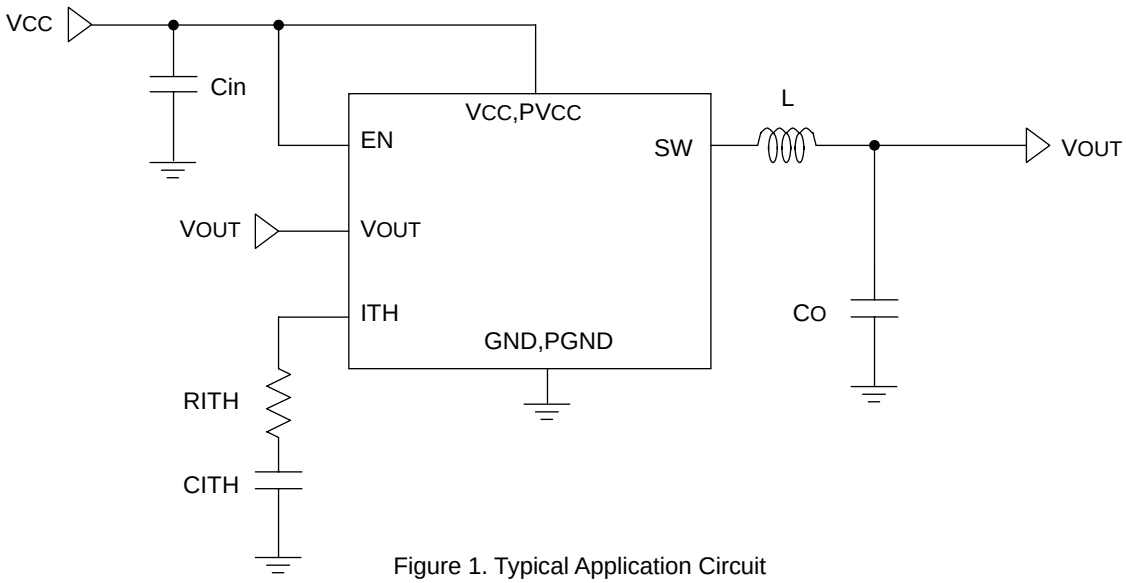


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

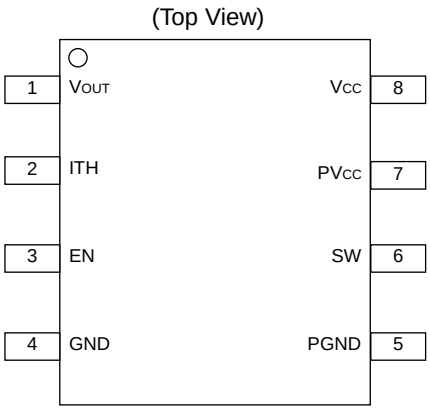


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	V_{OUT}	Output voltage detect pin
2	ITH	GmAmp output pin/Connected phase compensation capacitor
3	EN	Enable pin(Active High)
4	GND	Ground
5	PGND	Nch FET source pin
6	SW	Pch/Nch FET drain output pin
7	PV_{CC}	Pch FET source pin
8	V_{CC}	V_{CC} power supply input pin

Block Diagram

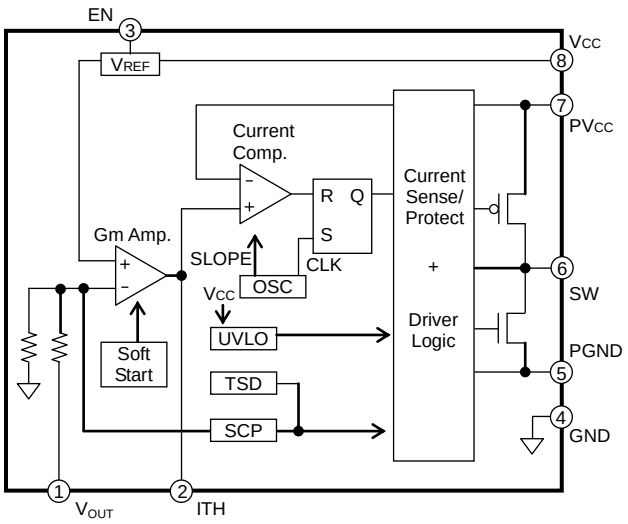


Figure 3. Block Diagram

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Description of Block

BD9109FVM-LB is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM™ (Simple Light Load Mode) operation for lighter load to improve efficiency.

○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

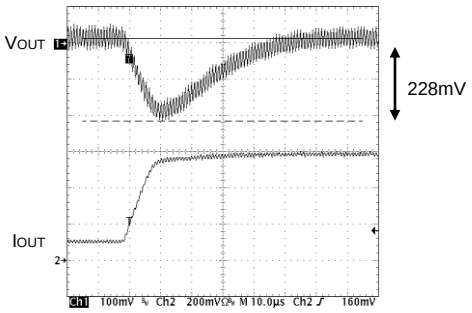
○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

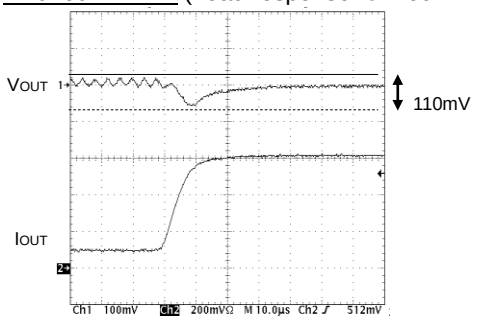
・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 1 MHz. SET signal form OSC turns ON a P-channel MOS FET (while a N-channel MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the P-channel MOS FET (while a N-channel MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

Conventional product (VOUT of which is 3.3 volts)



BD9109FVM-LB (Load response IO=100mA→600mA)



Voltage drop due to sudden change in load was reduced by about 50%.

Figure 4. Comparison of transient response

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Description of Block – continued

・SLLM™ (Simple Light Load Mode) control

When the control mode is shifted from PWM for heavier load to the one for lighter load or vise versa, the switching pulse is designed to turn OFF with the device held operated in normal PWM control loop, which allows linear operation without voltage drop or deterioration in transient response during the mode switching from light load to heavy load or vise versa.

Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed that the RESET signal is held issued if shifted to the light load mode, with which the switching is tuned OFF and the switching pulses are thinned out under control. Activating the switching intermittently reduces the switching dissipation and improves the efficiency.

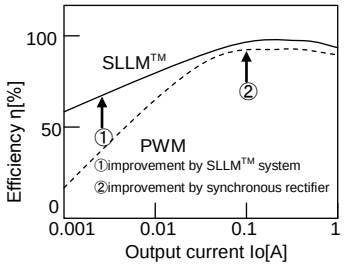


Figure 5. Efficiency

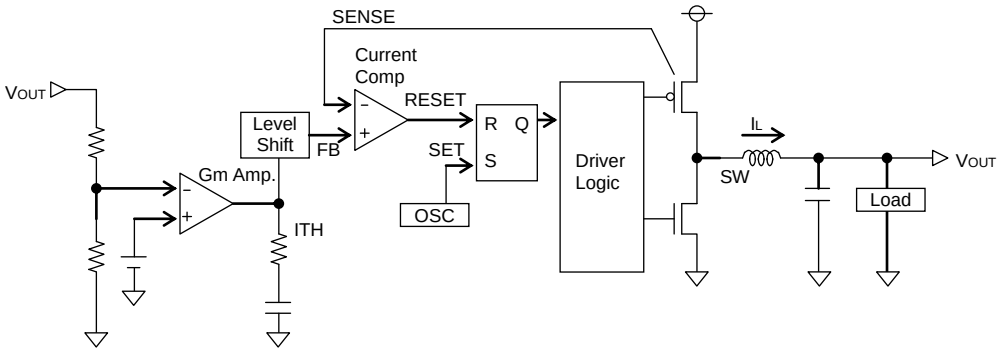


Figure 6. Diagram of current mode PWM control

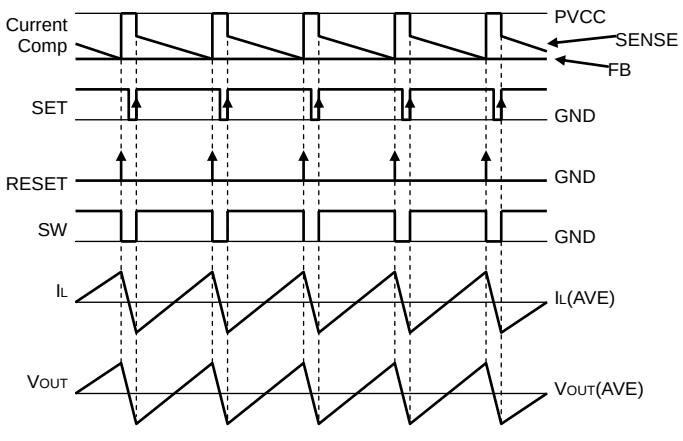


Figure 7 . PWM switching timing chart

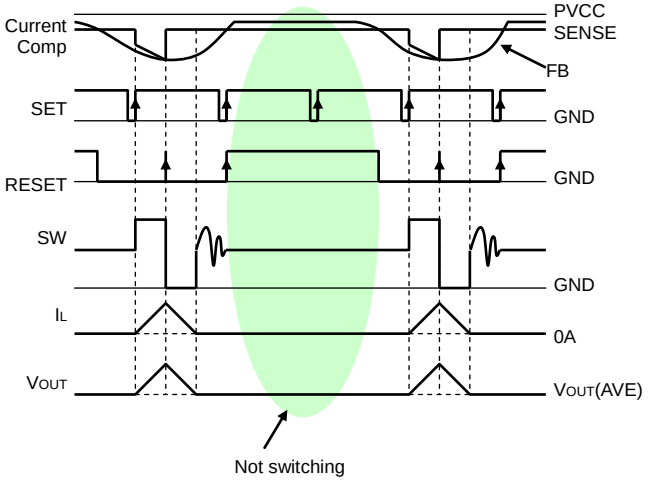


Figure 8. SLLM™ switching timing chart

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Description of Block – continued

- Soft-start function
  EN terminal shifted to “High” activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.
- Shutdown function
  With EN terminal shifted to “Low”, the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0 μA (Typ).
- UVLO function
  Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied. And the hysteresis width of 50 to 300 mV (Typ) is provided to prevent output chattering.

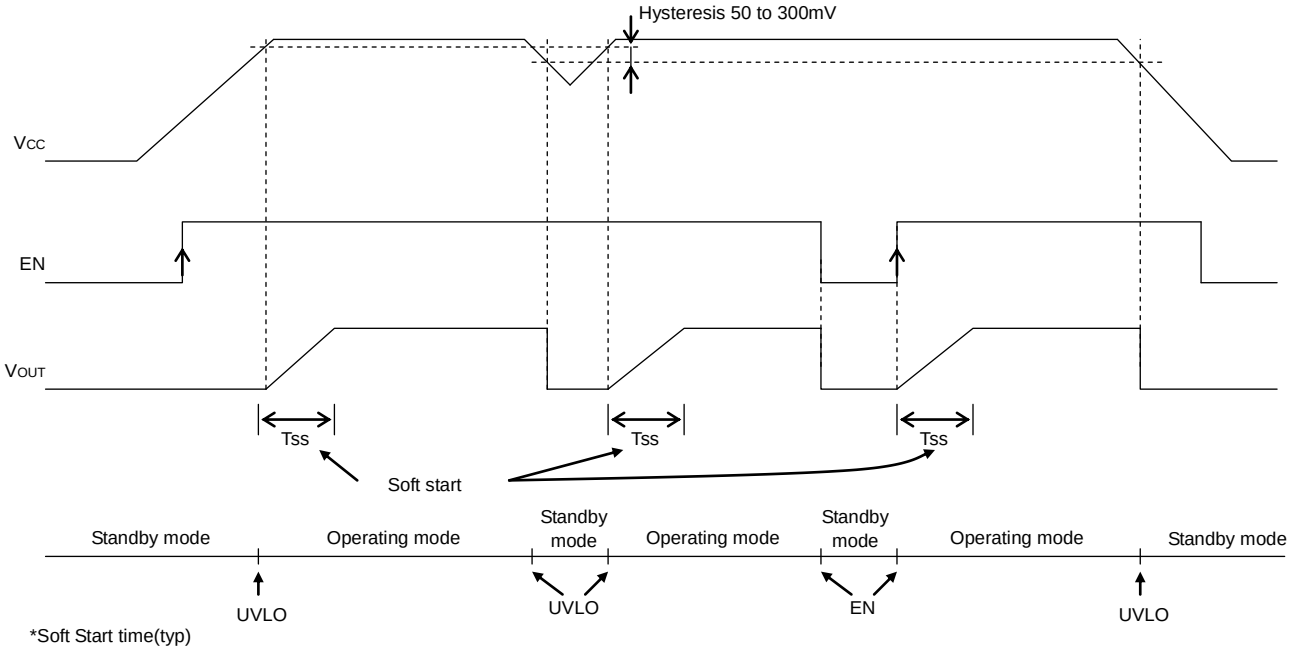


Figure 9 . Soft start, Shutdown, UVLO timing chart

	BD9109FVM-LB	Unit
Tss	1	msec

- Short-current protection circuit with time delay function
  Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time(T_{LATCH}) or more. The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

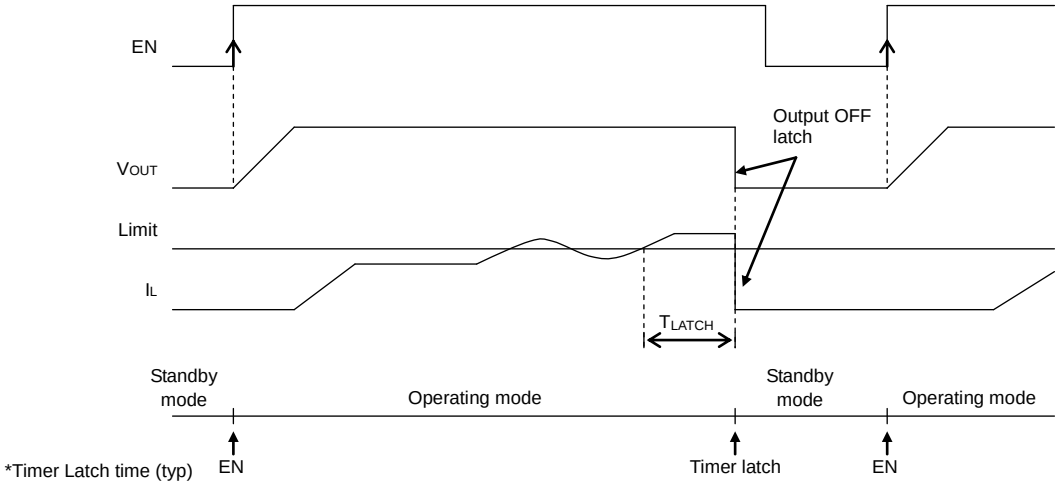


Figure 10 . Short-current protection circuit with time delay timing char

	BD9109FVM-LB	Unit
T_{LATCH}	2	msec

In addition to current limit circuit, output short detect circuit is built in on BD9109FVM-LB. If output voltage fall below 2V(typ, BD9109FVM-LB) output voltage will hold turned OFF.

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Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Rating	Unit
VCC Voltage	VCC	-0.3 to +7 (Note 1)	V
PVCC Voltage	PVCC	-0.3 to +7 (Note 1)	V
EN Voltage	EN	-0.3 to +7	V
SW, ITH Voltage	SW,ITH	-0.3 to +7	V
Power Dissipation 1	Pd1	387.5 (Note 2)	mW
Power Dissipation 2	Pd2	587.4 (Note 3)	mW
Operating Temperature Range	Topr	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
EN Voltage	Tjmax	+150	°C

(Note 1) Pd should not be exceeded.
(Note 2) Derating in done 3.1mW/℃ for temperatures above Ta=25℃
(Note 3) Derating in done 4.7mW/℃ for temperatures above Ta=25℃,Mounted on 70mm×70mm×1.6mm Glass Epoxy PCB.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions(Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
VCC voltage	VCC (Note 4)	4.5	5.0	5.5	V
PVCC voltage	PVCC (Note 4)	4.5	5.0	5.5	V
EN voltage	EN	0	-	VCC	V
SW average output current	Isw (Note 4)	-	-	0.8	A

(Note 4) Pd should not be exceeded.

Electrical Characteristics(Unless otherwise specified Ta=25°C VCC=PVCC=5V EN=VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby current	ISTB	-	0	10	μA	EN=GND
Bias current	ICC	-	250	400	μA	
EN Low voltage	VENL	-	GND	0.8	V	Standby mode
EN High voltage	VENH	2.0	VCC	-	V	Active mode
EN input current	IEN	-	1	10	μA	VEN=5V
Oscillation frequency	FOSC	0.8	1	1.2	MHz	
Pch FET ON resistance (Note 5)	RONP	-	0.35	0.60	Ω	PVCC=5V
Nch FET ON resistance (Note 5)	RONN	-	0.25	0.50	Ω	PVCC=5V
Output voltage	VOUT	3.234	3.300	3.366	V	
ITH sink current	ITHSI	10	20	-	μA	VOUT =H
ITH source current	ITHSO	10	20	-	μA	VOUT =L
UVLO threshold voltage	VUVLO1	3.6	3.8	4.0	V	VCC=H→L
UVLO hysteresis voltage	VUVLO2	3.65	3.9	4.2	V	VCC=L→H
Soft start time	TSS	0.5	1	2	ms	
Timer latch time	TLATCH	1	2	3	ms	SCP/TSD operated
Output Short circuit Threshold Voltage	VSCP	-	2	2.7	V	VOUT =H→L

(Note 5) Outgoing inspection is not done on all products

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Typical Performance Curves

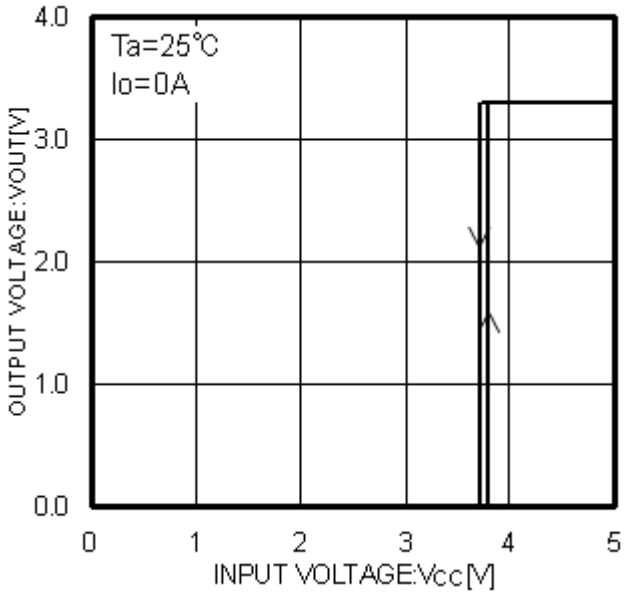


Figure 11. V_{OUT} VS V_{CC}

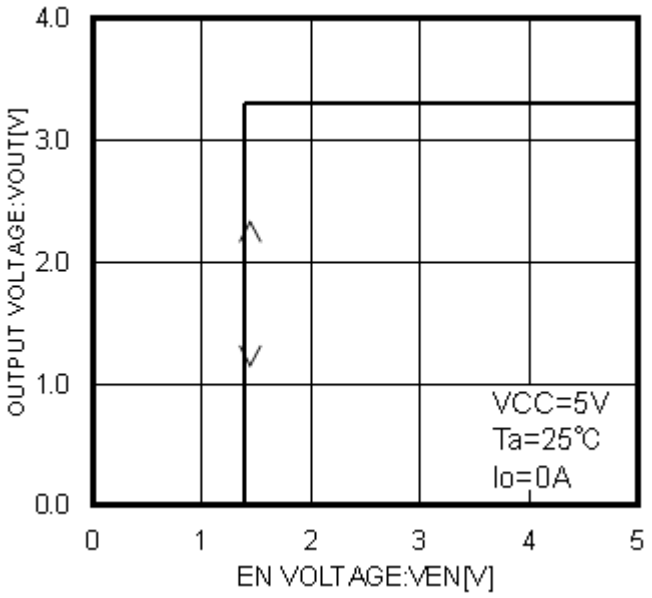


Figure 12. V_{OUT} VS V_{EN}

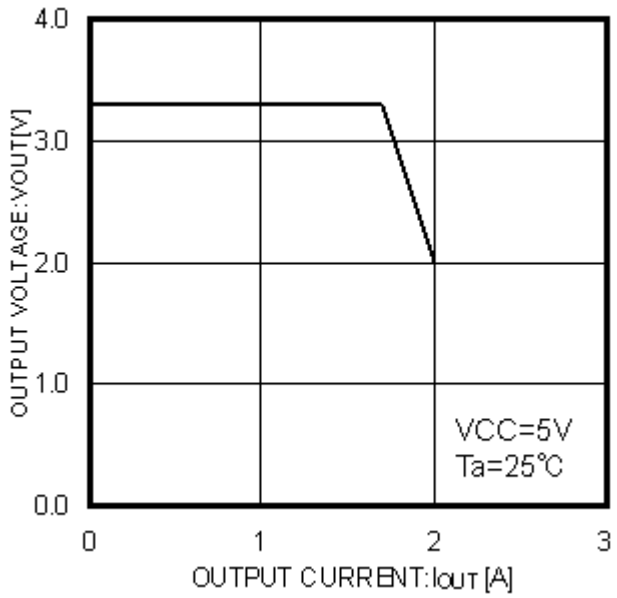


Figure 13. V_{OUT} VS I_{OUT}

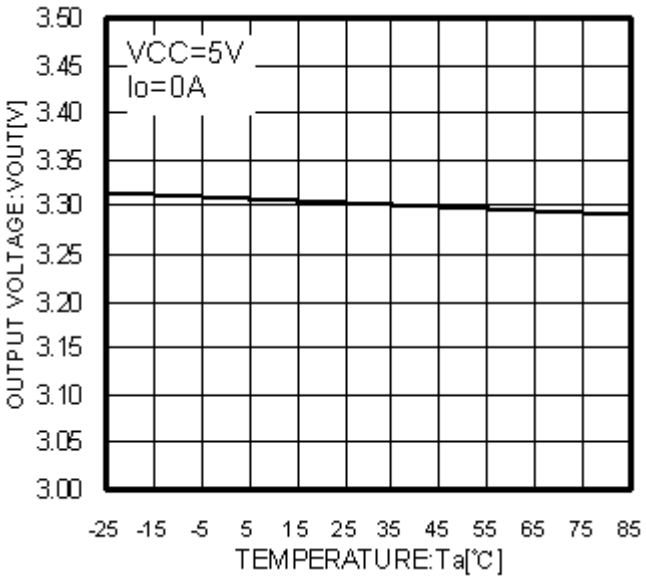


Figure 14. V_{OUT} VS Ta

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Typical Performance Curves - continued

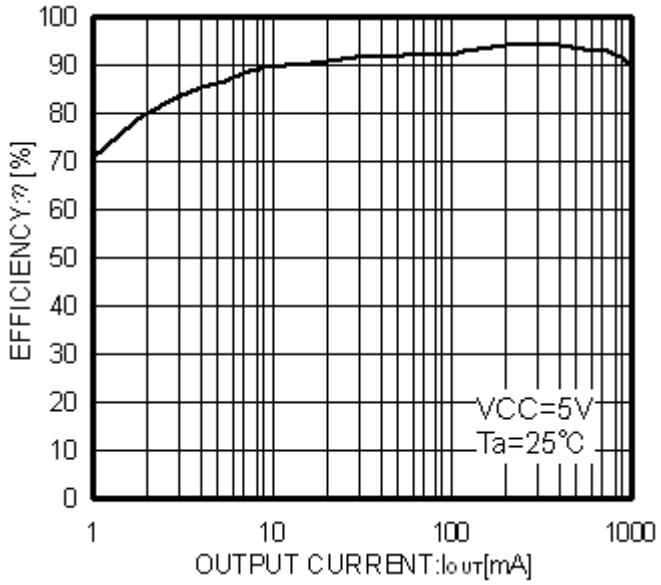


Figure 15. Efficiency

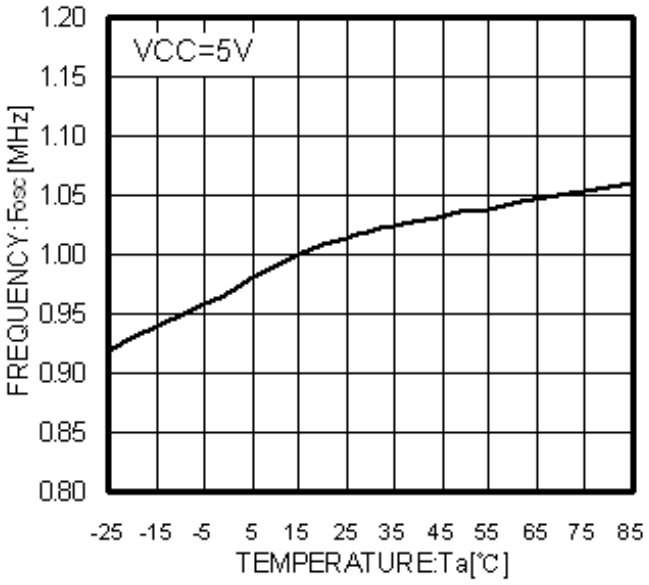


Figure 16. fosc VS Ta

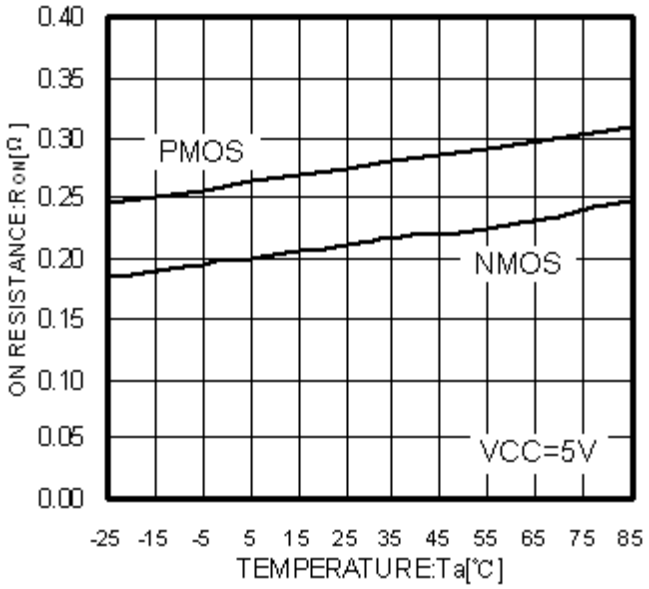


Figure 17. R_{ONN}, R_{ONP} VS Ta

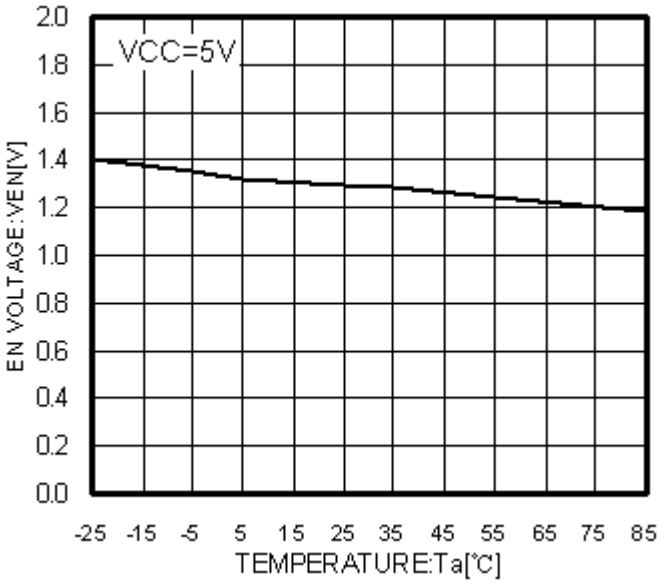


Figure 18. V_{EN} VS Ta

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Typical Performance Curves - continued

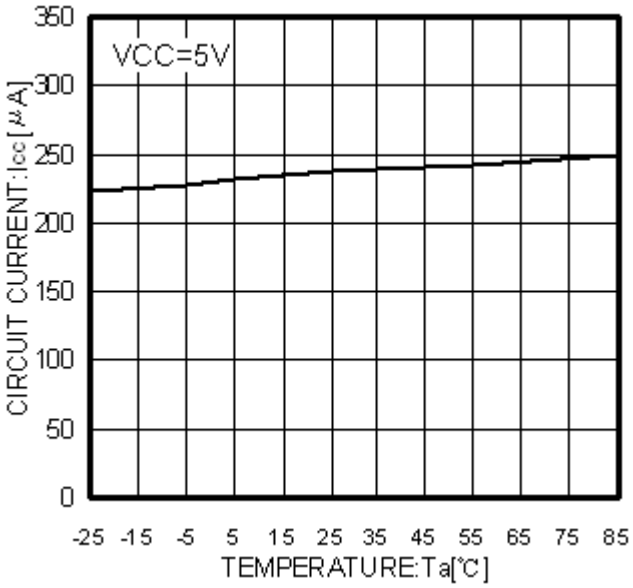


Figure 19. I_{CC} VS Ta

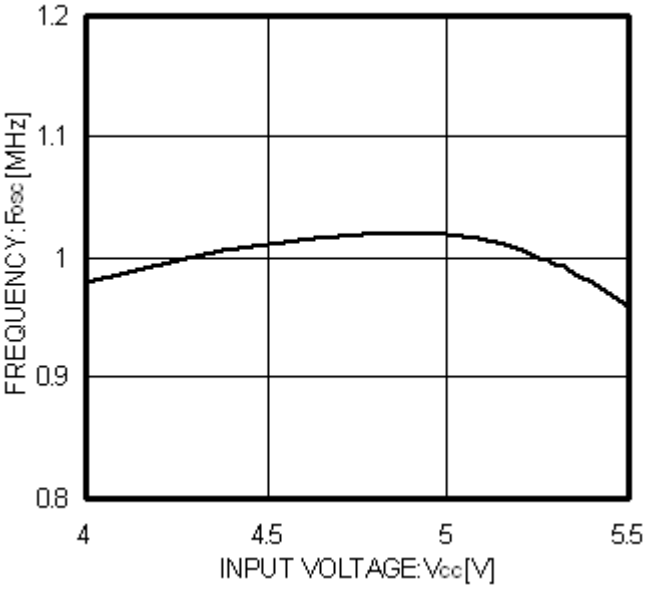


Figure 20. fosc VS V_{CC}

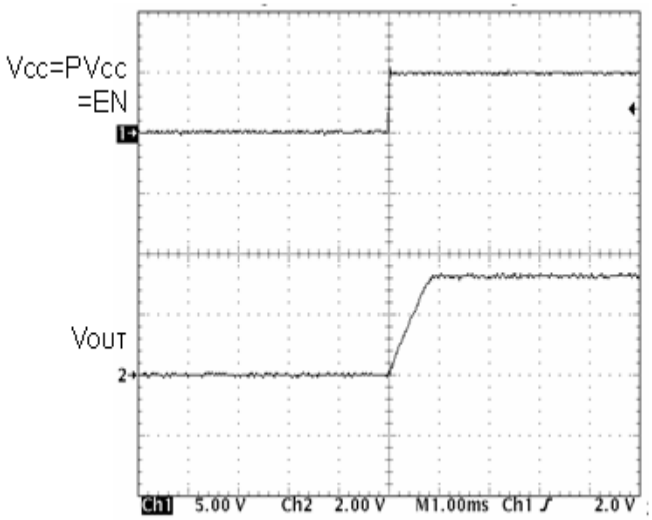


Figure 21. Soft start waveform

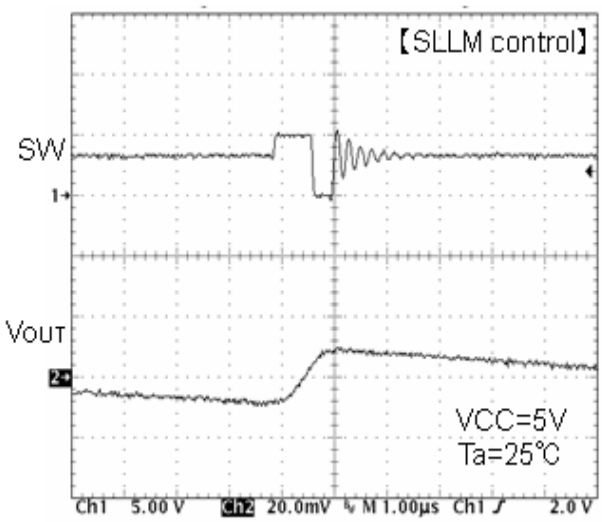


Figure 22. SW waveform Io=10mA

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Typical Performance Curves - continued

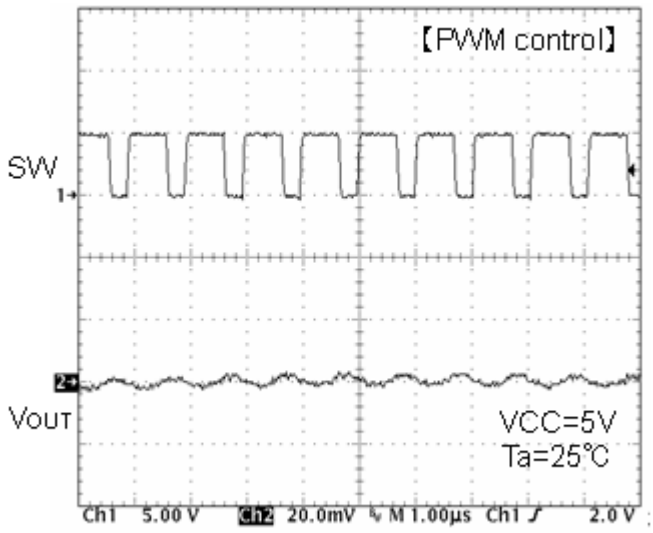


Figure 23. SW waveform Io=200mA

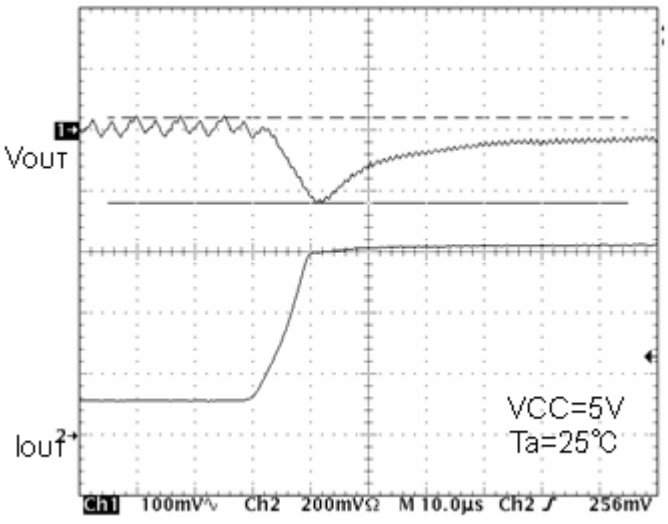


Figure 24. Transient response
Io=100mA→600mA(10µs)

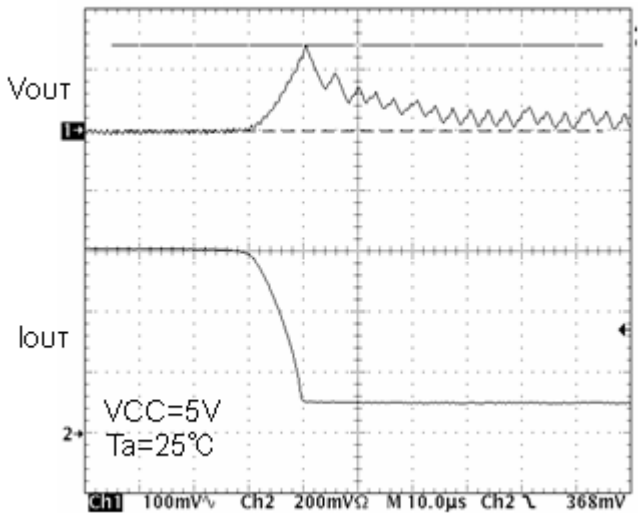


Figure 25. Transient response
Io=600mA→100mA(10µs)

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Application Example

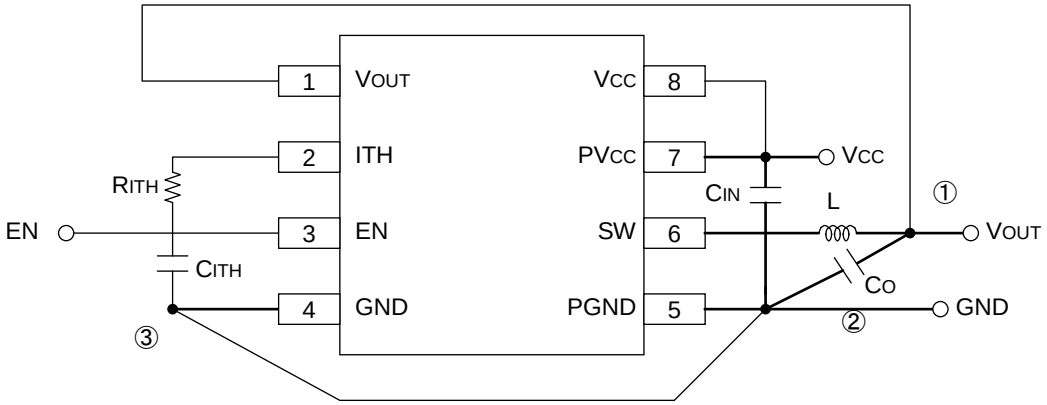


Figure 26. Board layout

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.
② Lay out the input ceramic capacitor CIN closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.
③ Lay out CITH and RITH between the pins ITH and GND as neat as possible with least necessary wiring.

Recommended Component Lists With Above Applications

Symbol	Part	Value	Manufacturer	Series
L	Coil	4.7µH	Sumida	CMD6D11B
			TDK	VLF5014AT-4R7M1R1
CIN	Ceramic capacitor	10µF	Kyocera	CM316X5R106K10A
CO	Ceramic capacitor	10µF	Kyocera	CM316X5R106K10A
CITH	Ceramic capacitor	330pF	murata	GRM18 Series
RITH	Resistance	30kΩ	Rohm	MCR10 3002

The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode established between the SW and PGND pins.

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Selection of Components Externally Connected

1. Selection of inductor (L)

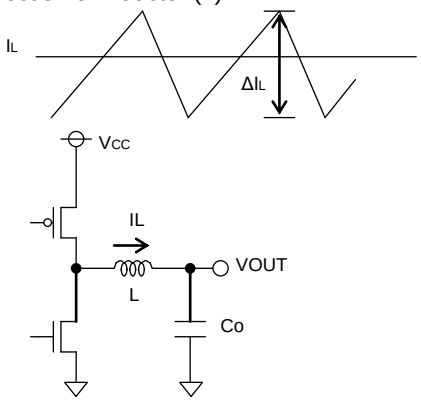


Figure 27. Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f}\ [A] \cdots (1)$$

Appropriate ripple current at output should be 30% more or less of the maximum output current.

$$\Delta I_L = 0.3\times I_{OUT}max\ [A] \cdots (2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L\times V_{CC}\times f}\ [H] \cdots (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5V, V_{OUT}=3.3V, f=1MHz, ΔI_L=0.3×0.8A=0.24A, for example,

$$L = \frac{(5-3.3)\times 3.3}{0.24\times 5\times 1M} = 4.675\mu \rightarrow 4.7[\mu H]$$

Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (C_O)

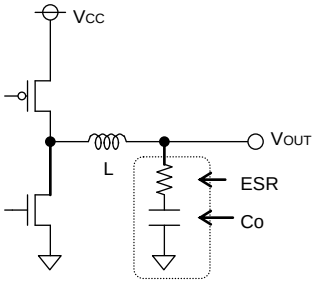


Figure 28. Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage. Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR\ [V] \cdots (4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

*Rating of the capacitor should be determined allowing sufficient margin against output voltage. Less ESR allows reduction in output ripple voltage.

As the output rise time must be designed to fall within the soft-start time, the capacitance of output capacitor should be determined with consideration on the requirements of equation (5):

$$Co \leqq \frac{T_{SS}\times(I_{limit}-I_{OUT})}{V_{OUT}}\ [F] \cdots (5)$$

Tss: Soft-start time
I_{limit}: Over current detection level, 2A(Typ)

For instance, and if V_{OUT}=3.3V, I_{OUT}=0.8A, and T_{SS}=1ms,

$$Co \leqq \frac{1m\times(2-0.8)}{3.3} \fallingdotseq 364\ [\mu F]$$

Inappropriate capacitance may cause problem in startup. A 10 µF to 100 µF ceramic capacitor is recommended.

3. Selection of input capacitor (Cin)

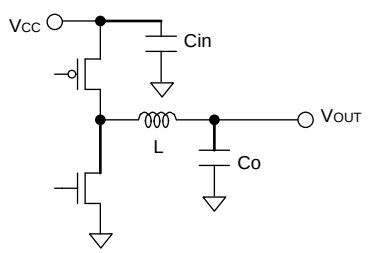


Figure 29. Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (6):

$$I_{RMS} = I_{OUT}\times \frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A] \cdots (6)$$

< Worst case > $I_{RMS(max)}$

When VCC is twice the Vout, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=3.3V, and I_{OUTmax}=0.8A,

$$I_{RMS} = 0.8\times \frac{\sqrt{3.3(5-3.3)}}{5} = 0.38[A_{RMS}]$$

A low ESR 10µF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

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4. Determination of RITH, CITH that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

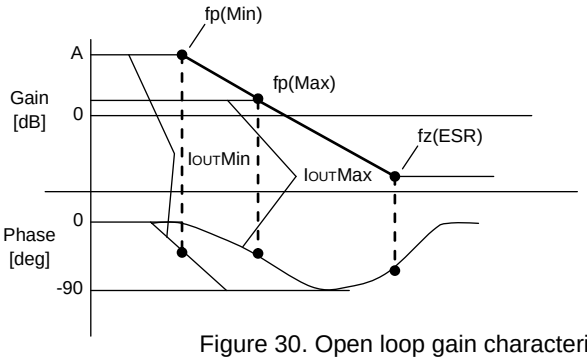


Figure 30. Open loop gain characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O} [Hz]$$

$$fz_{(ESR)} = \frac{1}{2\pi \times ESR \times C_O} [Hz]$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min)} = \frac{1}{2\pi \times R_{OMax} \times C_O} [Hz] \leftarrow \text{with lighter load}$$

$$fp_{(Max)} = \frac{1}{2\pi \times R_{OMin} \times C_O} [Hz] \leftarrow \text{with heavier load}$$

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$fz_{(Amp)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} [Hz]$$

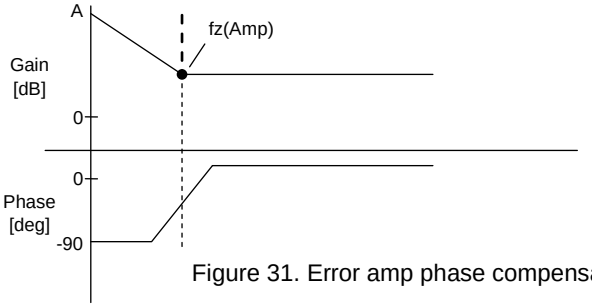


Figure 31. Error amp phase compensation characteristics

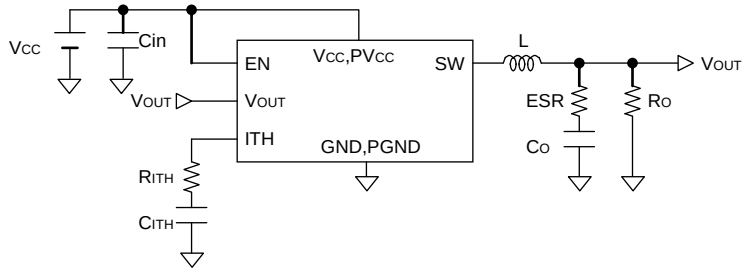


Figure 32. Typical application

Stable feedback loop may be achieved by canceling the pole fp (Min) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz_{(Amp)} = fp_{(Min)}$$

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax} \times C_O}$$

5. Determination of output voltage

The output voltage VOUT is determined by the equation (7):

$V_{OUT} = (R2/R1+1) \times V_{ADJ}$ ・・・(7) V_{ADJ}: Voltage at ADJ terminal (0.8V Typ)

With R1 and R2 adjusted, the output voltage may be determined as required.

{ Adjustable output voltage range : 1.0V to 2.5V }

Use 1 kΩ to 100 kΩ resistor for R1. If a resistor of the resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

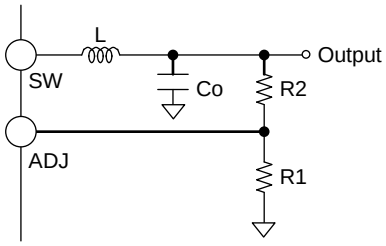


Figure 33. Determination of output voltage

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Switching Regulator Efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_D\alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:
1) ON resistance dissipation of inductor and FET : PD(I^2R)
2) Gate charge/discharge dissipation : PD(Gate)
3) Switching dissipation : PD(SW)
4) ESR dissipation of capacitor : PD(ESR)
5) Operating current dissipation of IC : PD(IC)

1)PD(I^2R)=I_{OUT}^2×(R_{COIL}+R_{ON}) (R_{COIL}[Ω] : DC resistance of inductor, R_{ON}[Ω] : ON resistance of FETI_{OUT}[A] : Output current.)
2)PD(Gate)=Cgs×f×V^2 (Cgs[F] : Gate capacitance of FET,f[Hz] : Switching frequency,V[V] : Gate driving voltage of FET)

3)PD(SW)= $\frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$ (C_{RSS}[F] : Reverse transfer capacitance of FET、I_{DRIVE}[A] : Peak current of gate.)

4)PD(ESR)=I_{RMS}^2×ESR (I_{RMS}[A] : Ripple current of capacitor,ESR[Ω] : Equivalent series resistance.)
5)PD(IC)=Vin×I_{CC} (I_{CC}[A] : Circuit current.)

Power Dissipation

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

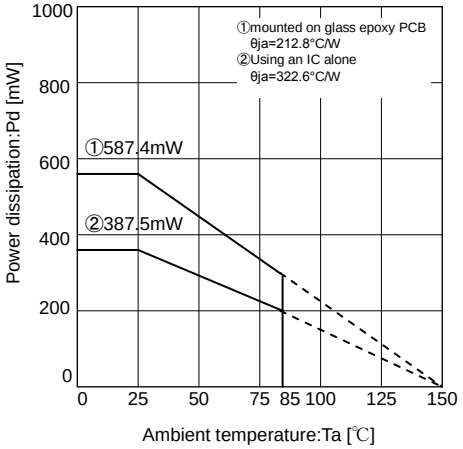


Figure 34. Thermal derating curve (MSOP8)

$P=I_{OUT}^2 \times (R_{COIL}+R_{ON})$
$R_{ON}=D \times R_{ONP}+(1-D) \times R_{ONN}$

D : ON duty (=V_{OUT}/V_{CC})
R_{COIL} : DC resistance of coil
R_{ONP} : ON resistance of P-channel MOS FET
R_{ONN} : ON resistance of N-channel MOS FET
I_{OUT} : Output current

If V_{CC}=5V, V_{OUT}=3.3V, R_{COIL}=0.15Ω, R_{ONP}=0.35Ω, R_{ONN}=0.25Ω,I_{OUT}=0.8A, for example,

$D=V_{OUT}/V_{CC}=3.3/5=0.66$
$R_{ON}=0.66 \times 0.35+(1-0.66) \times 0.25$
$=0.231+0.085$
$=0.316[\Omega]$

$P=0.8^2 \times (0.15+0.316)$
$\fallingdotseq 298[mV]$

As R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON duty becomes greater. With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

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I/O equivalence circuit

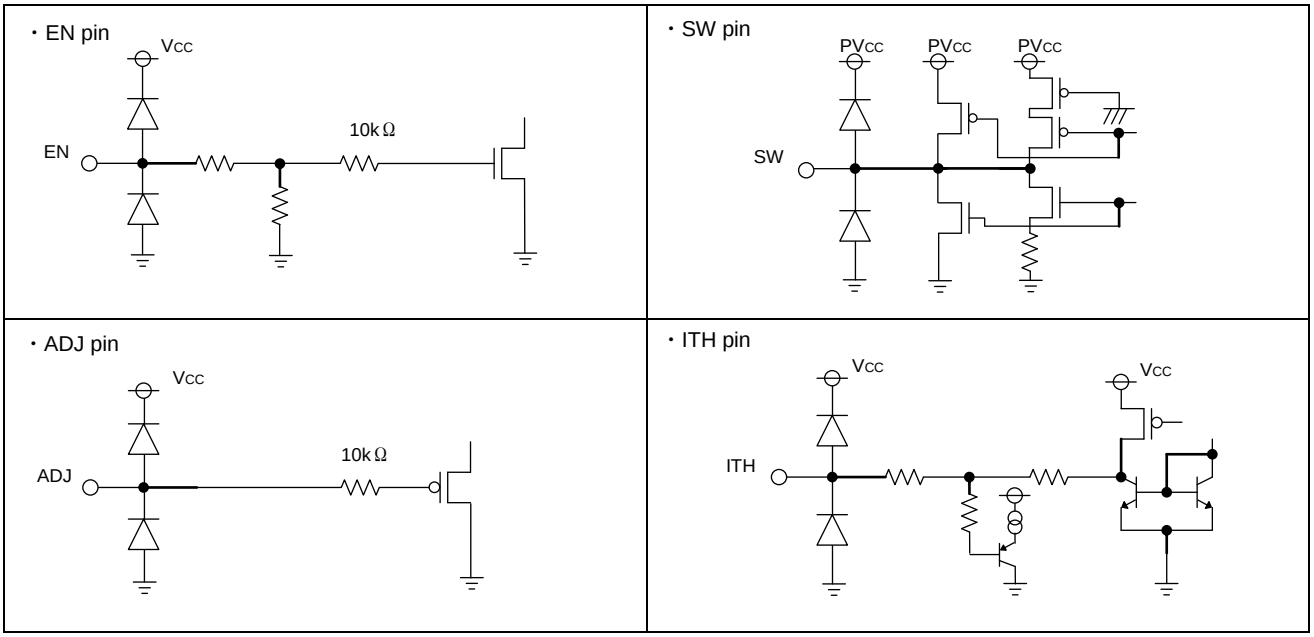


Figure 35. I/O equivalence circuit

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

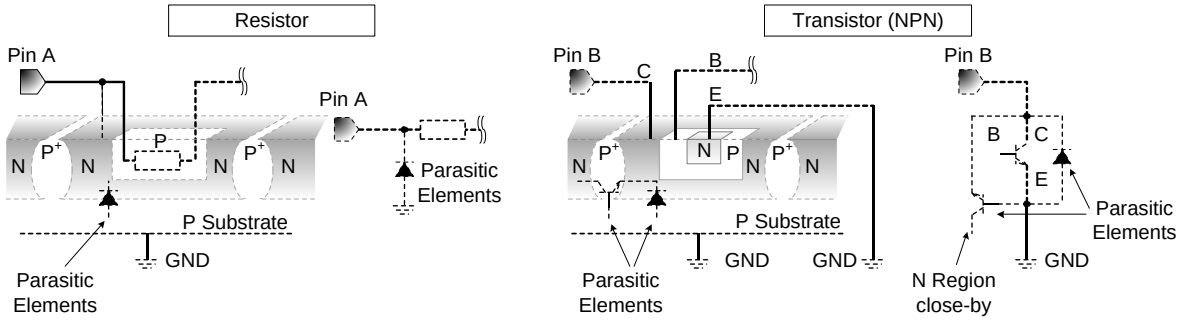


Figure 36. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

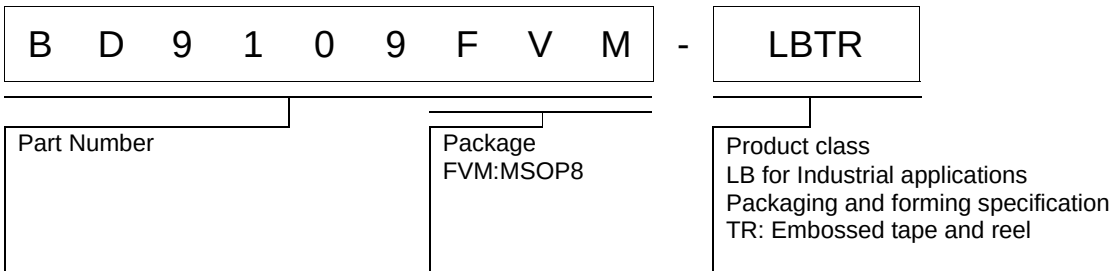
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

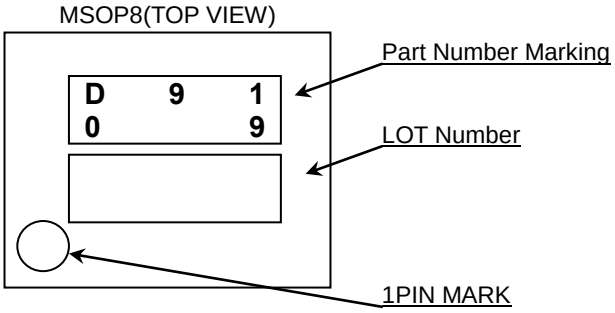
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information



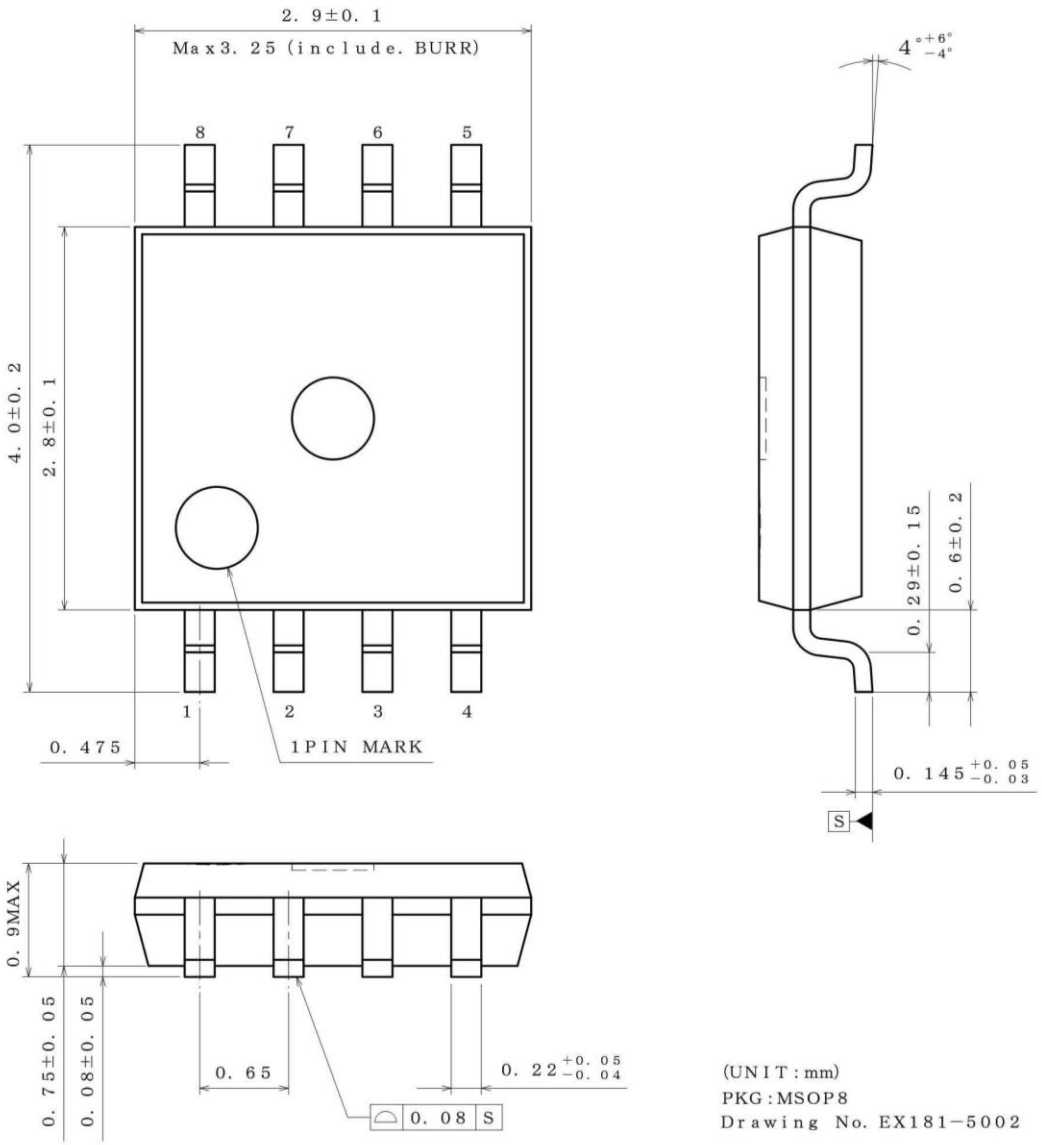
Marking Diagrams



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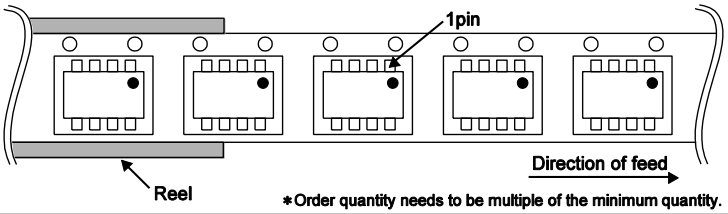
Physical Dimension, Tape and Reel Information

Package Name	MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
10.Sep.2013	001	New Release
21.Feb.2014	002	Delete sentence “and log life cycle” in General Description and Futures.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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