2.7V to 14V Synchronous Buck-Boost Controller

BD8303MUV

General Description

BD8303MUV is ROHM's high efficiency step-up/step-down switching regulator IC. It produces output of 3.3V / 5V from 1 cell of lithium battery, 4 batteries, or 2 cells of Li batteries with just one inductor.

This IC uses an original step-up/step-down drive system and provides a higher efficient power supply than conventional SEPIC-system or H-bridge system switching regulators.

Features

- Highly-Efficient Step-Up/Step-Down DC/DC Converter Implemented with Just One Inductor
- Supports High-Current Applications with External N-Channel FET
- Incorporates a Soft-Start Function
- Incorporates a Timer-Latch System with Short Circuit Protection Function

Applications

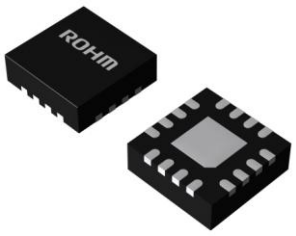
General Portable Equipment

- DVC
- Single-Lens Reflex Cameras
- Portable DVDs
- Mobile PCs

Key Specifications

- Input Voltage Range: +2.7V to +14V
- Reference Volatage Accuracy : 1.25%
- Standby Current: 0μA(Typ)
- Operating Temperature Range: -25°C to +85°C

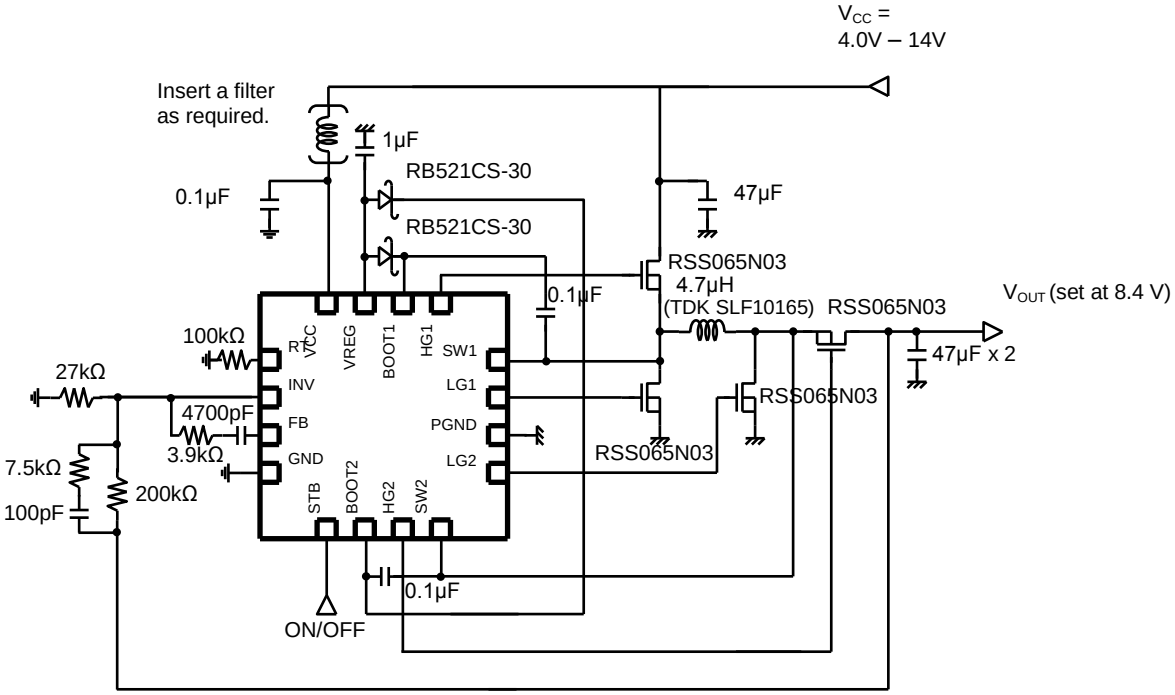
Package W(Typ) x D(Typ) x H(Max)



VQFN016V3030
3.00mm x 3.00mm x 1.00mm

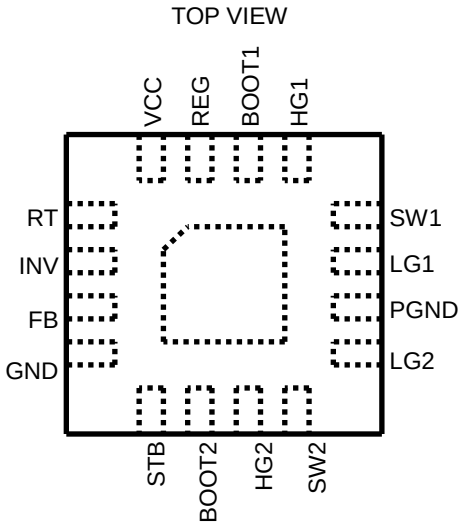
Typical Application Circuit

V_{CC}=4.0~14V, V_{OUT}=8.4V, I_{OUT}=100mA ~ 1500mA



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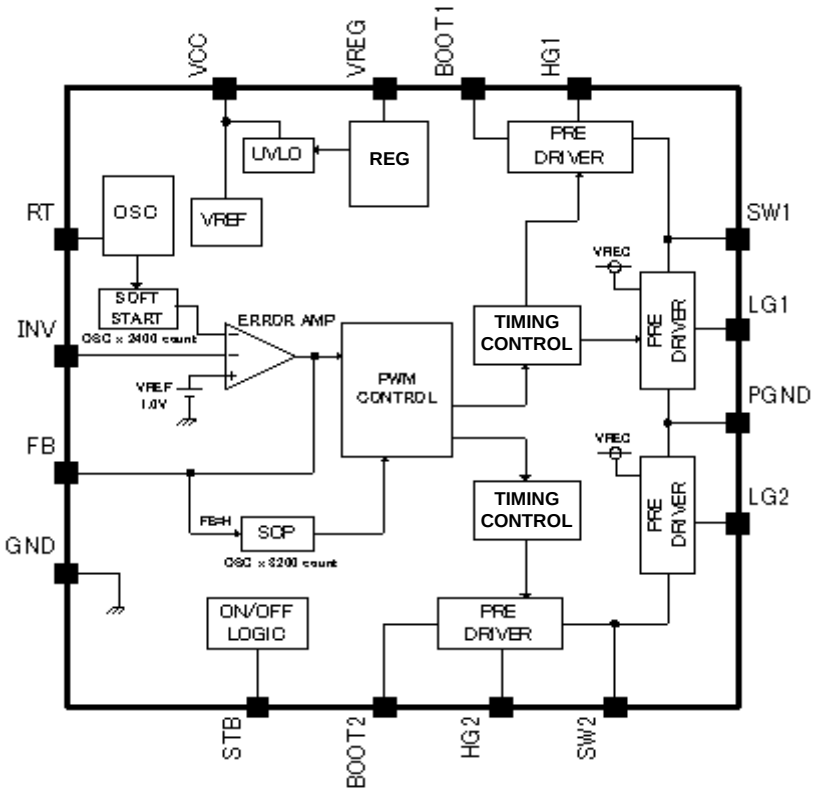
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	RT	Oscillation frequency set terminal
2	INV	Error AMP input terminal
3	FB	Error AMP output terminal
4	GND	Ground terminal
5	STB	ON/OFF terminal
6	BOOT2	Output side high-side driver input terminal
7	HG2	Output side high-side FET gate drive terminal
8	SW2	Output side coil connecting terminal
9	LG2	Output side low-side FET gate drive terminal
10	PGND	Driver part ground terminal
11	LG1	Input side low-side FET gate drive terminal
12	SW1	Input side coil connecting terminal
13	HG1	Input side high-side FET gate drive terminal
14	BOOT1	Input side high-side driver input terminal
15	REG	5V Internal regulator output terminal
16	VCC	Power input terminal

Block Diagram



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Description of Blocks

1. VREF
   This block generates ERROR AMP reference voltage. The reference voltage is set to 1.0V.

2. VREG
   This is a voltage regulator block which outputs 5.0V and is used as power supply for IC internal circuit and BOOT pin supply. Follows power supply voltage when 5.0V or below while the output voltage drops at the same time.
   An external 1.0µF capacitor is recommended to prevent oscillation.

3. UVLO
   This block prevents the malfunction of the internal circuitry during start-up or when the supply drops below a certain voltage. When VREG is below 2.4V, the HG1, HG2, LG1 and LG2 pin is low, this block turns OFF all FET and DC/DC converter outputs and resets the timer latch of the internal SCP circuit and soft-start circuit

4. SCP
   This block is the Short Circuit Protection that uses a Timer Latch System. It has an internal counter that is in synch with OSC. When the INV pin is set to 1.0V or lower voltage, the internal counter will count about 8200 pulses after which the latch circuit will activate Turning OFF the DC/DC converter output (13.6msec when R_{RT} = 51kΩ). Restarting the STB pin or the supply voltage will reset the latch circuit.

5. OSC
   The OSC block generates the internal frequency of the IC. The frequency can be varied depending on the value of the external resistance of the RT pin (Pin 1).When R_{RT} = 51kΩ, the operation frequency is set to 600kHz.

6. ERROR AMP
   The ERROR AMP block detects output signals and PWM control signals and compares them with an internal reference voltage set at 1.0V.

7. PWM COMP
   The PWM COMP block is a Voltage-to-Pulse Width converter that controls the output voltage depending on the input voltage. This block controls the pulse width by comparing the internal SLOPE waveform with the ERROR AMP output voltage. The output signal of the PWM COMP block is then fed to the driver. Max Duty and Min Duty are set at the primary side and the secondary side of the inductor respectively, which are as follows:

Primary side (SW1)	HG1 Max Duty	:	About 90%,
	HG1 Min Duty	:	0 %
Secondary side (SW2)	LG2 Max Duty	:	About 90%,
	LG2 Min Duty	:	About 10%,

8. SOFT START
   This block prevents in-rush current during start-up by bringing the output voltage of the DCDC converter into a soft-start. The Soft-Start block is in synch with the internal OSC block. This block enables the output voltage of the DCDC converter to reach the set voltage after about 2400 pulses (4msec when R_{RT} = 51kΩ).

9. N-Channel DRIVER
   This block consists of a CMOS inverter circuit that drives the built-in N-Channel FET. It provides dead time for preventing feed through during switching of HG1 = L to LG1 = H to HG2 = L to LG2 = H and LG1 = L to HG1 = H, LG2 = L to HG2 = H. The dead time is set at about 100nsec for each individual SWs

10. ON/OFF LOGIC
    This block enables and disables the IC depending on the voltage applied at STB pin (Pin 5). The IC Turns ON when STB voltage is 2.5 V or higher and it Turns OFF when STB is open or when 0V is applied. The STB pin has a pull-down resistor of approximately 400kΩ.

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Maximum Applied Power Voltage	V_{CC}	15	V
	V_{REG}	7	V
	Between V_{BOOT1} , V_{BOOT2} and V_{SW1}, V_{SW2}	7	V
	Between V_{BOOT1} , V_{BOOT2} and GND	20	V
	V_{SW1} and V_{SW2}	15	V
Power Dissipation	Pd	0.62 (Note 1)	W
Operating Temperature Range	Topr	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) When installed on a 70.0 mm x 70.0 mm x 1.6 mm glass epoxy board. The rating is reduced by 4.96 mW/°C at Ta = 25°C or more.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Standard Value			Unit
		Min	Typ	Max	
Power Supply Voltage Range	V_{CC}	2.7	—	14	V
Output Voltage Range	V_{OUT}	1.8	—	12	V
Oscillation Frequency Range	f_{OSC}	0.2	0.6	1.0	MHz

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Electrical Characteristics (Unless otherwise specified, Ta = 25°C, V_{CC} = 7.4V)

Parameter		Symbol	Target Value			Unit	Conditions
			Minimum	Typical	Maximum		
UVLO							
Detection Threshold Voltage		V_{UV}	-	2.4	2.6	V	VREG monitor
Hysteresis Range		ΔV_{UVHY}	50	100	200	mV	
Oscillator							
Oscillation Frequency		f_{OSC}	480	600	720	kHz	R_{RT}=51kΩ
Regulator							
Output Voltage		V_{REG}	4.7	5.1	5.5	V	
Error AMP							
INV Threshold Voltage		V_{INV}	0.9875	1.00	1.0125	V	
Input Bias Current		I_{INV}	-50	0	+50	nA	V_{CC}=12.0V, V_{INV}=6.0V
Soft-Start Time		t_{SS}	2.4	4.0	5.6	msec	R_{RT}=51kΩ
Output Source Current		I_{EO}	10	20	30	μA	V_{INV}=0.8V , V_{FB}=1.5V
Output Sink Current		I_{EI}	0.6	1.3	3	mA	V_{INV}=1.2V , V_{FB}=1.5V
PWM Comparator							
SW1 Max Duty		D_{MAX1}	85	90	95	%	HG1 ON
SW2 Max Duty		D_{MAX2}	85	90	95	%	LG2 ON
SW2 Min Duty		D_{MIN2}	5	10	15	%	LG2 OFF
Output							
HG1, 2 High side ON-Resistance		R_{ONHP}	-	4	8	Ω	
HG1, 2 Low side ON-Resistance		R_{ONHN}	-	4	8	Ω	
LG1, 2 High side ON-Resistance		R_{ONLP}	-	4	8	Ω	
LG1, 2 Low side ON-Resistance		R_{ONLN}	-	4	8	Ω	
HG1-LG1 Dead Time		t_{DEAD1}	50	100	200	nsec	
HG2-LG2 Dead Time		t_{DEAD2}	50	100	200	nsec	
STB							
STB pin Control Voltage	Operation	V_{STBH}	2.5	-	V_{CC}	V	
	No-Operation	V_{STBL}	-0.3	-	+0.3	V	
STB Pin Pull-Down Resistance		R_{STB}	250	400	700	kΩ	
Circuit Current							
Standby Current	VCC Pin	I_{STB}	-	-	1	μA	
VCC Circuit Current		I_{CC1}	-	650	1000	μA	V_{INV}=1.2V
BOOT1 and BOOT2 Circuit Current		I_{CC2}	-	120	240	μA	V_{INV}=1.2V

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Typical Performance Curves
(Unless otherwise specified, Ta = 25°C, V_{CC} = 7.4V)

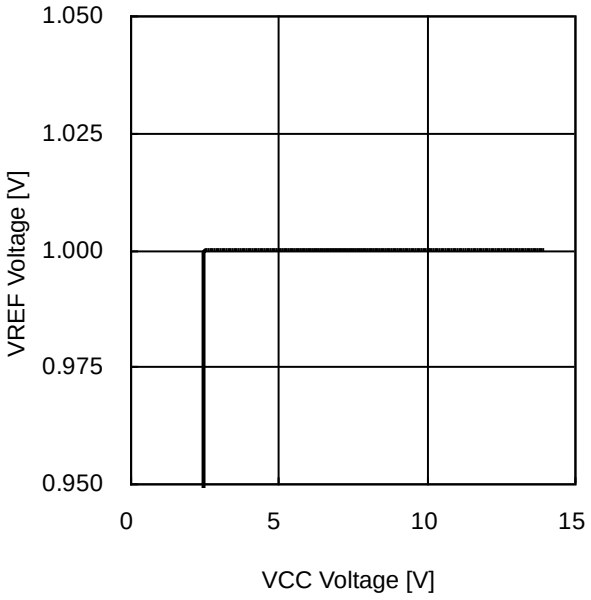


Figure 1. VREF Voltage vs VCC Voltage

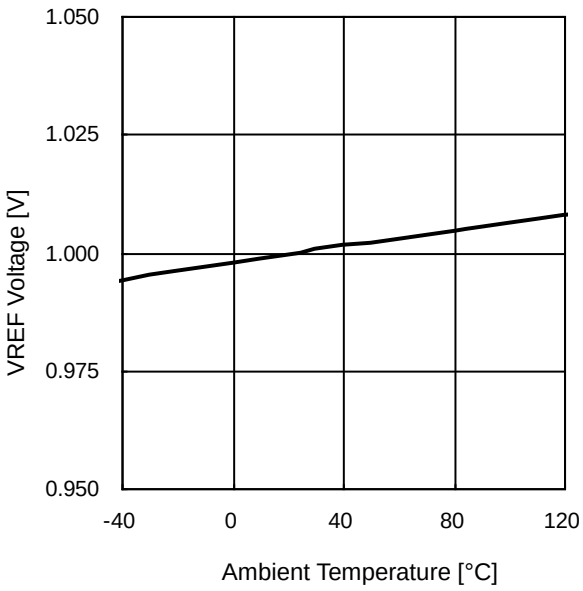


Figure 2. VREF Voltage vs Ambient Temperature

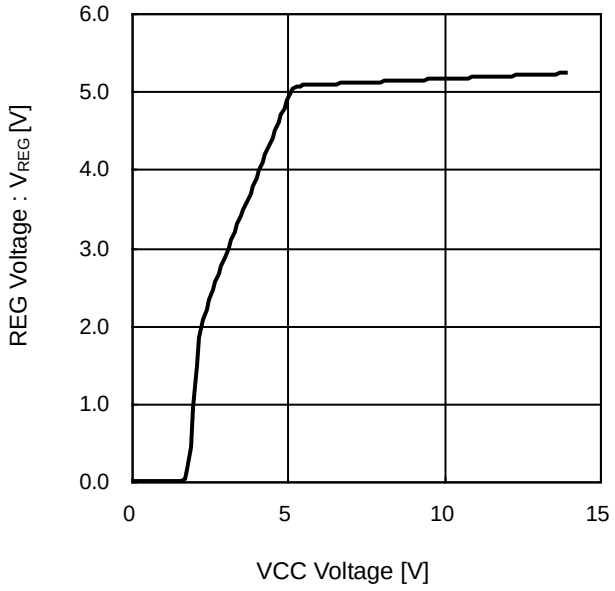


Figure 3. REG Voltage vs VCC Voltage

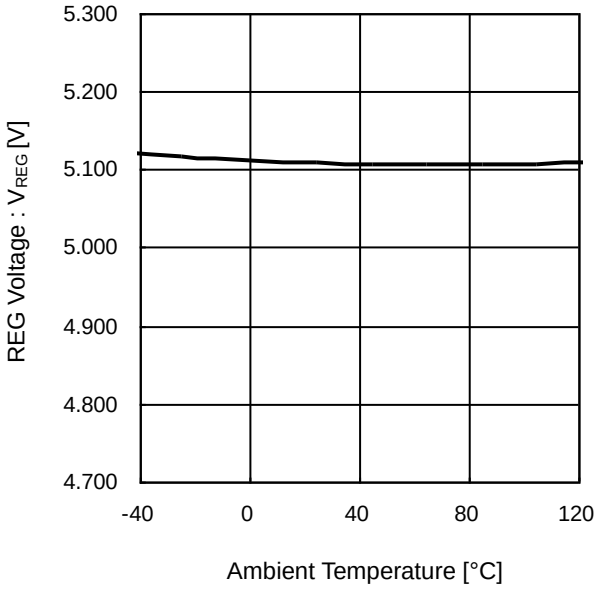


Figure 4. REG Voltage vs Ambient Temperature

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Typical Performance Curves - continued

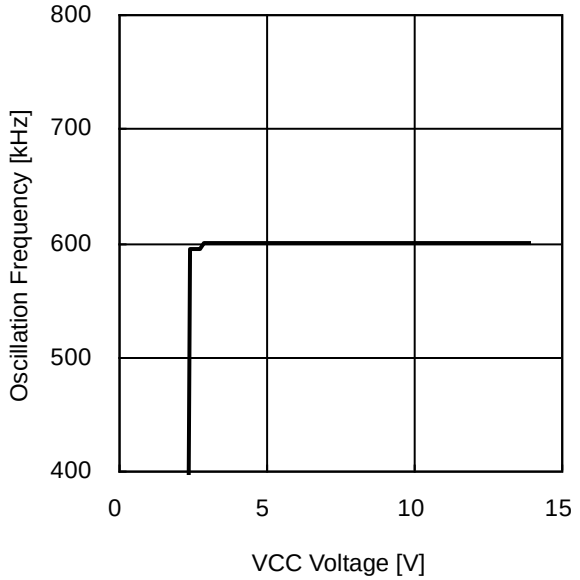


Figure 5. Oscillation Frequency vs V_{CC} Voltage

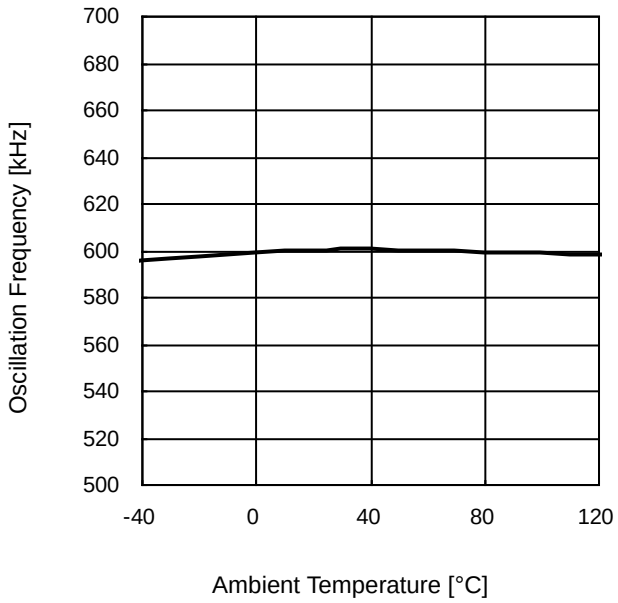


Figure 6. Oscillation Frequency vs Ambient Temperature

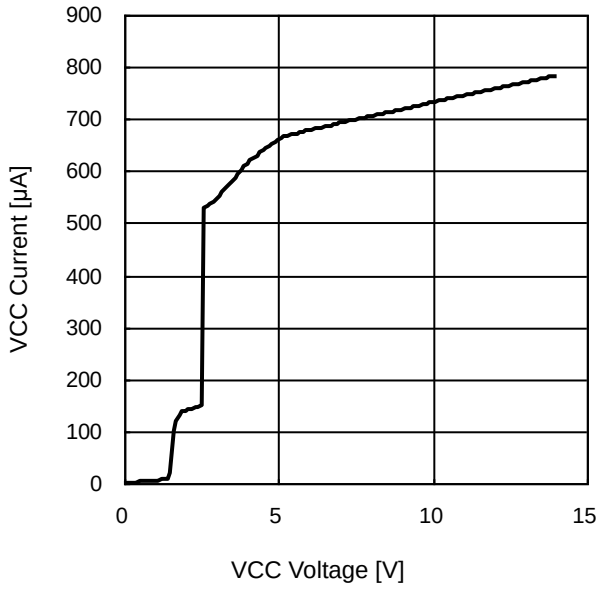


Figure 7. VCC Current vs VCC Voltage

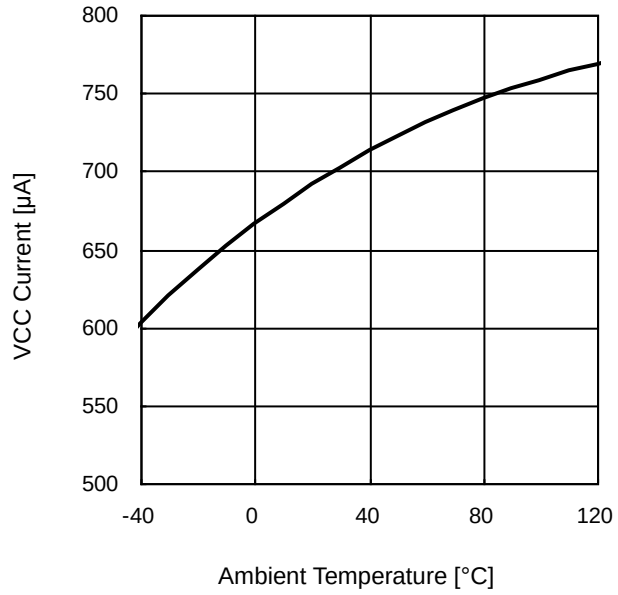


Figure 8. VCC Current vs Ambient Temperature

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Typical Performance Curves - continued

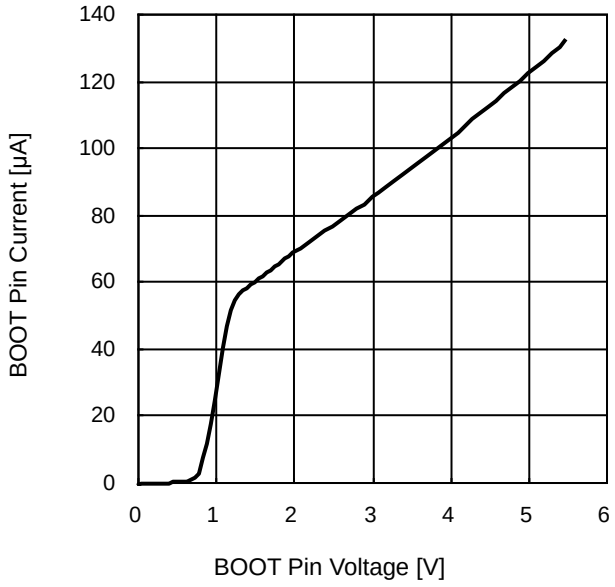


Figure 9. BOOT Pin Current vs BOOT Pin Voltage

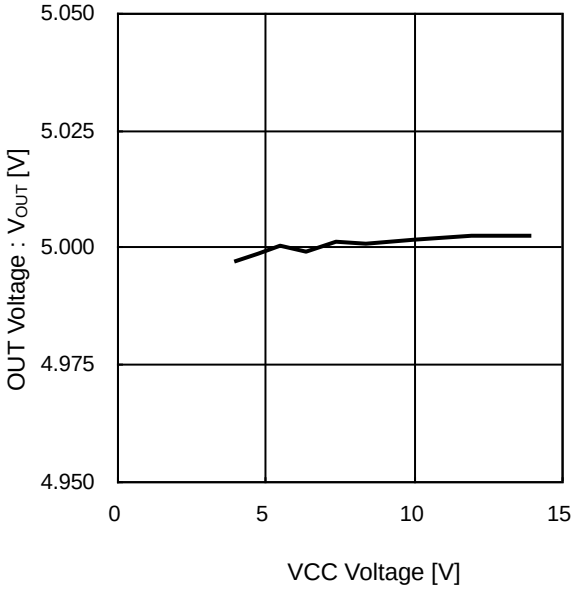


Figure 10. OUT Voltage vs VCC Voltage
(Line Regulation)

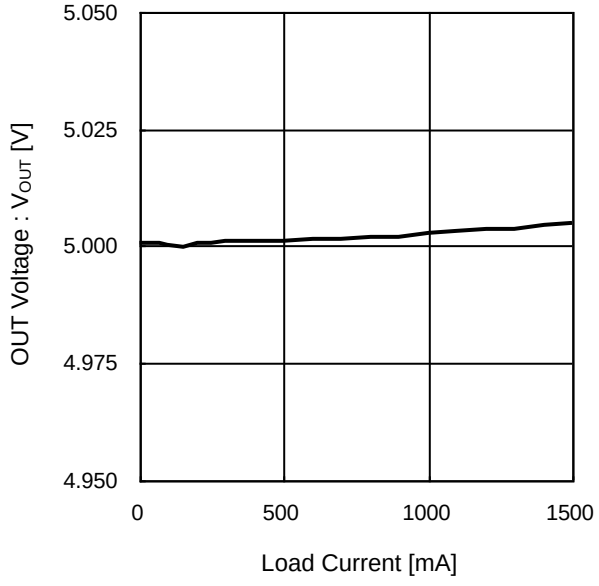


Figure 11. OUT Voltage vs Load Current
(Load Regulation)

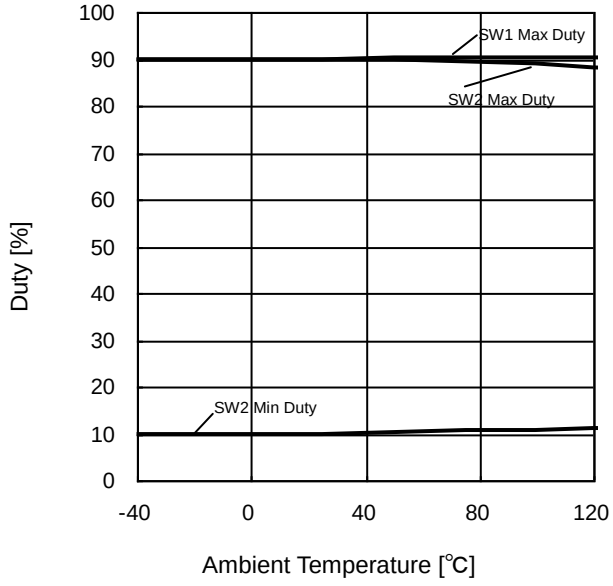


Figure 12.
MAX Duty / MIN Duty vs Ambient Temperature

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Typical Performance Curves - continued

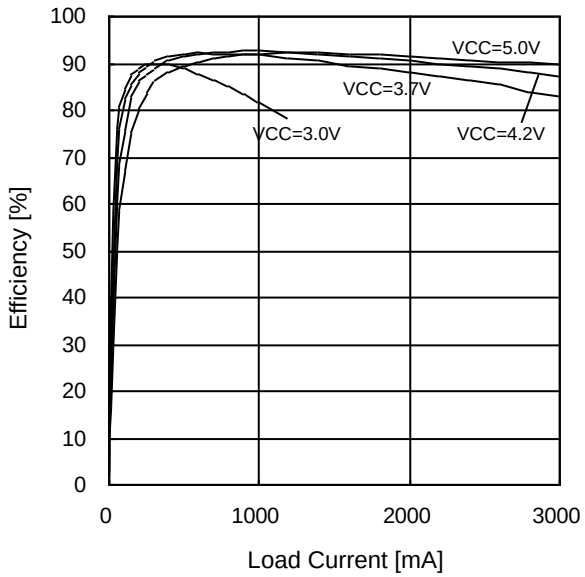


Figure 13. Efficiency vs Load Current
(Example of Application Circuit [1]
(V_{OUT} = 3.3V))

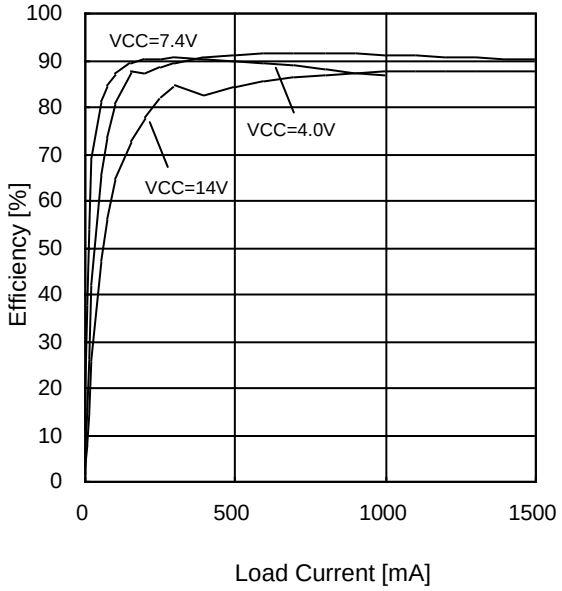


Figure 14. Efficiency vs Load Current
(Example of Application Circuit [2]
(V_{OUT} = 5.0V))

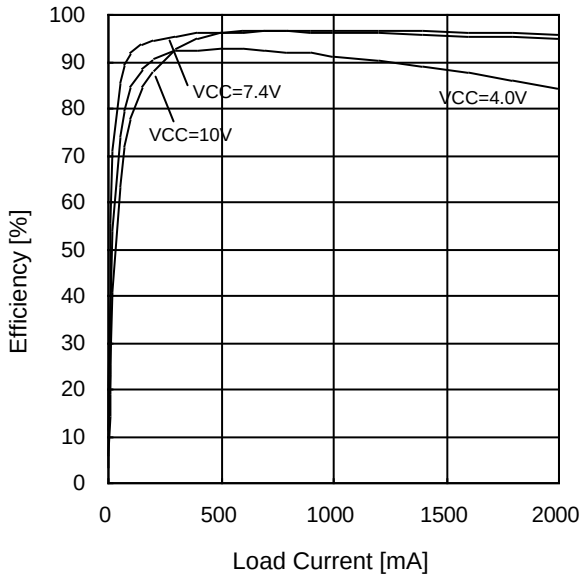


Figure 15. Efficiency vs Load Current
(Example of Application Circuit [3]
(V_{OUT} = 8.4V)

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Typical Waveforms

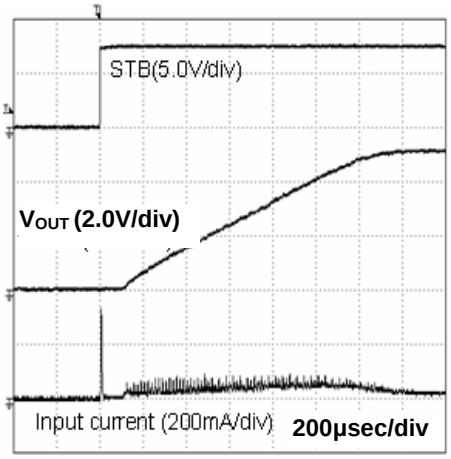


Figure 16. Starting Waveform
Example of Application Circuit [2]
(L=10µH, C_{OUT} = 47µH, f_{OSC} = 750 kHz, unloaded)

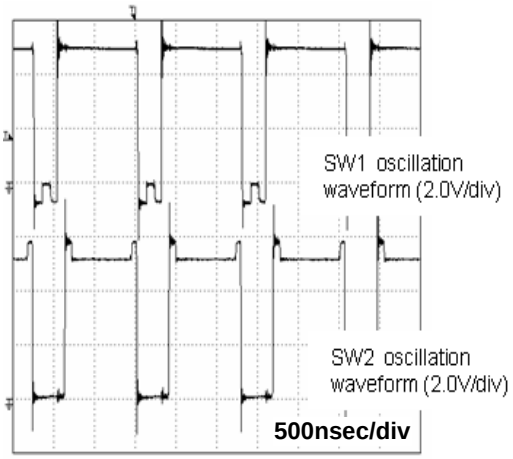


Figure 17. Oscillation Waveform
(V_{CC} = 5.0V, V_{OUT} = 5.0V, I_{LOAD} = 1000mA)

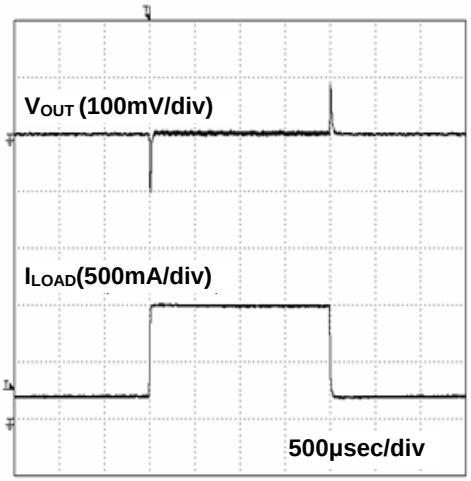


Figure 18. Load Variation Waveform
Example of Application Circuit [2]
(V_{CC} = 7.4V, V_{OUT} = 5.0V,
I_{LOAD} = 200mA ↔1000mA :40 mA/µsec)

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Application Information

1. Package Heat Reduction Curve

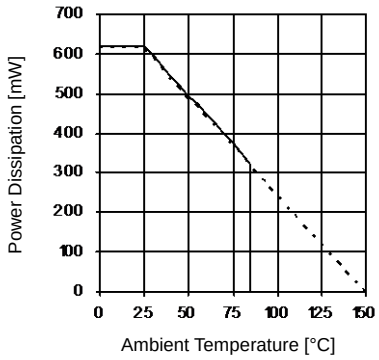


Figure 19. Power Dissipation vs Ambient Temperature
Heat Reduction Curve (IC alone)
when used at Ta = 25°C or more, it is reduced by 4.96 mW/°C.

2. Example of Application Circuit

(1) Application Circuit [1]: Input: 2.7V to 5.5V, Output: 3.3V / 100mA to 2000mA

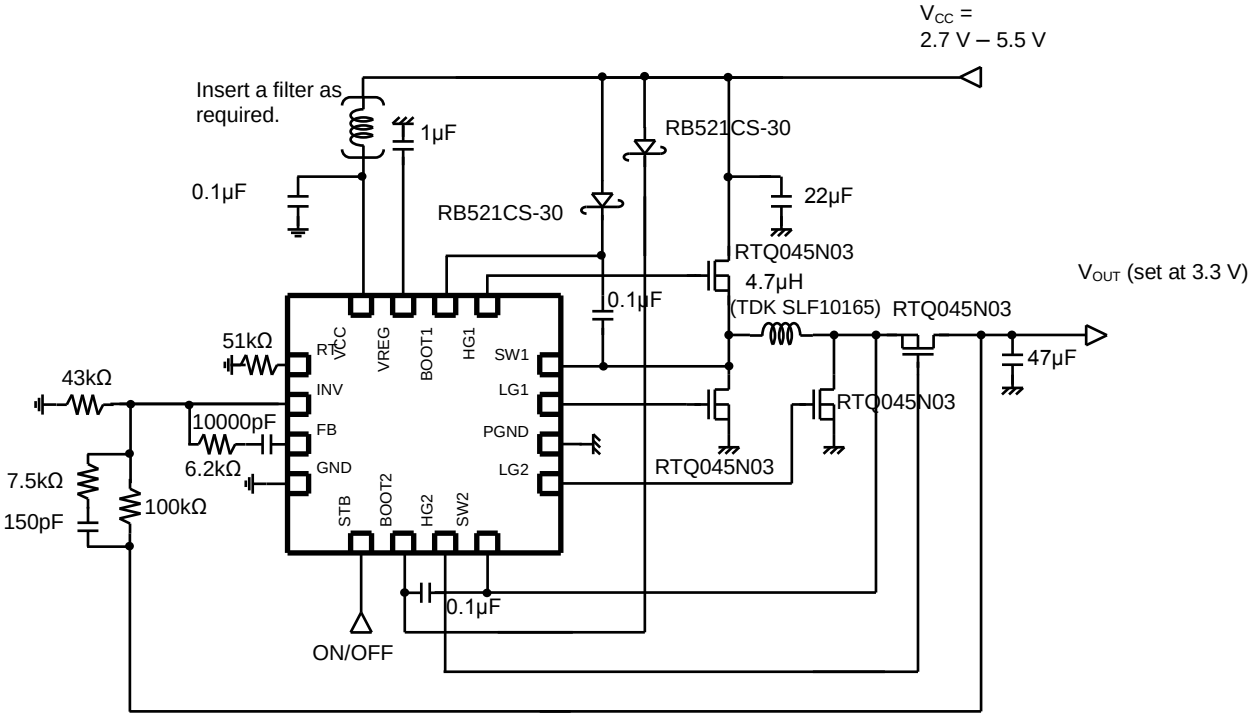


Figure 20. Example of Application Circuit [1]

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(2) Application Circuit [2]: Input: 2.7V to 14 V, Output : 5.0V / 100 mA to 1500 mA

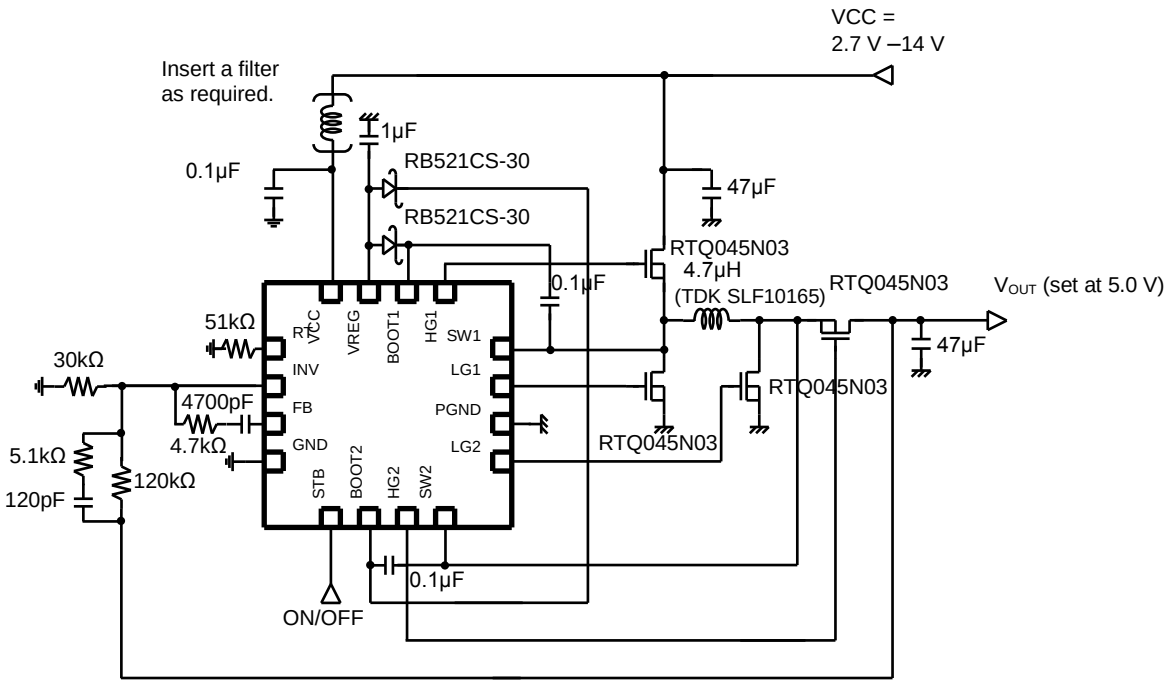


Figure 21. Example of Application Circuit [2]

(3) Application Circuit [3]: Input : 4.0V to 14V, Output : 8.4V / 100mA to 1500mA

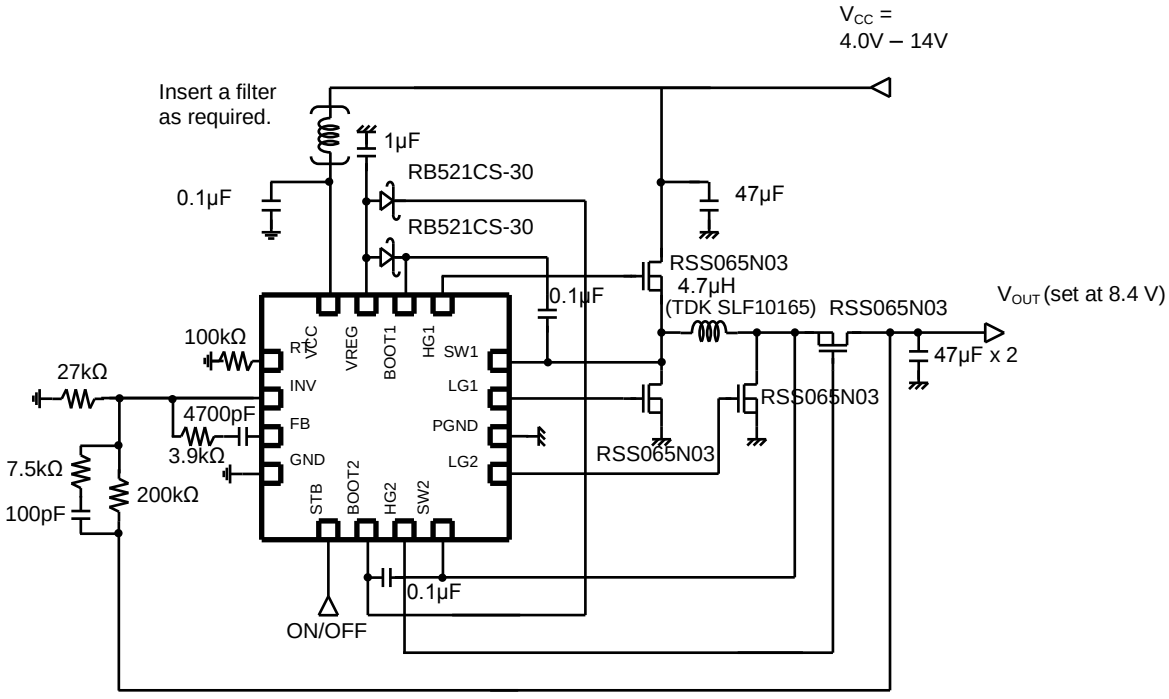


Figure 22. Example of Application Circuit [3]

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(4) Application Circuit [4]: Input : 2.7V to 14V, Output : 12V / 100mA to 1500mA

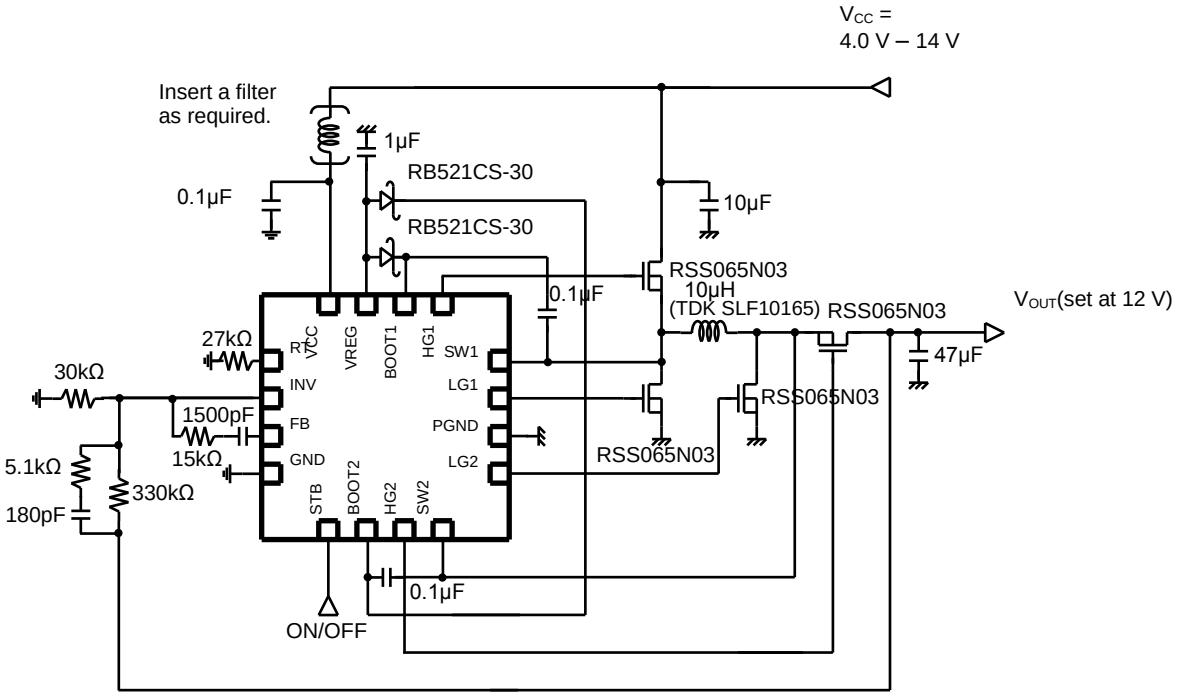


Figure 23. Example of Application Circuit (4)

3. Selection of Parts for Applications

(1) Output Inductor

A shielded inductor that satisfies the current rating (current value, I_{PEAK} as shown in Figure 24 Ripple Current) and has a low DCR (direct current resistance component) is recommended. Inductor values greatly affect the output ripple current. Ripple current can be reduced as the coil (L) value becomes larger and the switching frequency becomes higher as shown in the equations below

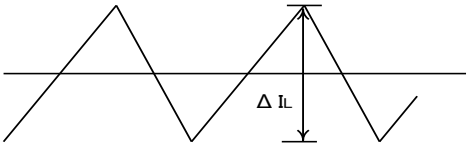


Figure 24. Ripple Current

$$I_{PEAK} = I_{OUT} \times (V_{OUT} / V_{IN}) / \eta + \frac{\Delta I_L}{2} \quad [A] \qquad (1)$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \quad [A] \quad ; \text{ (in step-down mode)} \qquad (2)$$

$$\Delta I_L = \frac{|(V_{IN} - V_{OUT})|}{L} \times \frac{V_{OUT} \times 2 \times 0.8}{(V_{IN} + V_{OUT})} \times \frac{1}{f} \quad [A] \quad ; \text{ (in step-up/down mode)} \qquad (3)$$

$$\Delta I_L = \frac{(V_{OUT} - V_{IN})}{L} \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f} \quad [A] \quad ; \text{ (in step-up mode)} \qquad (4)$$

where:
η is the efficiency
ΔI_L is the output ripple current
f is the switching frequency

As a guide, output ripple current should be set at about 20% to 50% of the maximum output current. Current flow that exceeds the coil rating brings the coil into magnetic saturation which may lead to lower efficiency or output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil.

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(2) Output Capacitor
A ceramic capacitor with low ESR is recommended at the output to reduce ripple. There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration. Output ripple voltage when ceramic capacitor is used is obtained by the following equation.

$$V_{PP} = \Delta I_L \times \frac{1}{2\pi \times f \times C_O} + \Delta I_L \times R_{ESR} \quad [V] \tag{5}$$

Setting must be performed so that output ripple is within the allowable ripple voltage.

(3) External FET
An external FET which satisfies the following items and has small C_{iss} (input capacitance), Q_g (total gate charge quantity) and ON-Resistance should be selected. There must be an adequate margin between the turn OFF time of MOS and the dead time to prevent through-current.

Drain-source voltage rating: Output voltage + Body Diode (V_F) of MOS or higher
Gate-source voltage rating: 7.0 V or higher
Drain-source current rating: I_{PEAK} of Output inductor paragraph or higher

(4) BOOT-SW Capacitor
The capacitor between BOOT and SW should be designed so that the gate drive voltage will not be below V_{GS} necessary for the FET to use, taking circuit current input to the BOOT pin into consideration. There must be an adequate margin between the maximum rating and gate drive voltage.

Gate Drive Voltage

$$= (V_{REG}\ voltage) - (V_F\ of\ Di) - (Voltage\ drop\ by\ BOOT\ pin\ consumption) \quad [V] \tag{6}$$

Voltage Drop by BOOT Pin Consumption

$$= \left(I_{BOOT} \times \left(1 / f_{OSC} \right) + Qg\ of\ external\ FET \right) / C_{BOOT} \quad [V] \tag{7}$$

(5) REG-BOOT Diode
A Schottky diode which has less forward voltage drop (V_F) and satisfies the following items:

Average rectified current: There must be an adequate margin against the current consumed by MOSFET switching.
DC inverse voltage: Input voltage or higher

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(6) Setting of Oscillation Frequency

Oscillation frequency can be set using a resistance value connected to the RT pin (Pin 1). Oscillation frequency is set at 600 kHz when R_{RT} = 51kΩ, and frequency is inversely proportional to RT value (See Figure 25 for the relationship between RT and frequency) as a result, Soft-start time changes along with oscillation frequency (See Figure 26 for the relationship between RT and soft-start time)

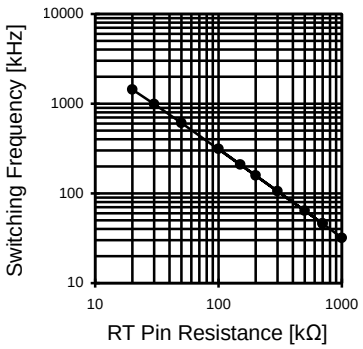


Figure 25. Switching Frequency vs RT Pin Resistance

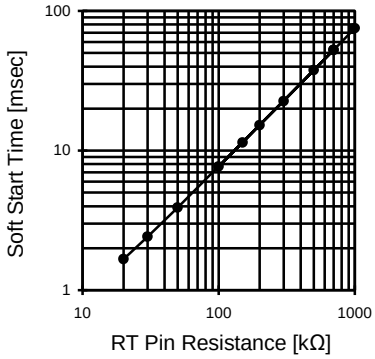
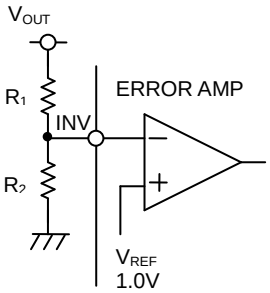


Figure 26. Soft-Start Time vs RT Pin Resistance

(Note) Note that the above example of frequency setting is just a design target value, and may differ from the actual equipment.

(7) Output Voltage Setting

The internal reference voltage of the ERROR AMP is 1.0V. Output voltage should be obtained by referring to Equation (8) of Figure 27.



$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 1.0 \qquad [V] \qquad (8)$$

Figure 27. Setting of Feedback Resistance

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(8) Determination of External Phase Compensation

Condition for stable application

The condition for feedback system stability under negative feedback is as follows:

Phase delay is 135 °or less when gain is 1 (0 dB) (Phase margin is 45° or higher). Since DC/DC converter application is sampled according to the switching frequency, the G_{BW} of the whole system (frequency at which gain is 0 dB) must be set to be equal to or lower than 1/5 of the switching frequency.

(a) Phase delay must be 135°or lower when gain is 1 (0dB) (Phase margin is 45° or higher).

(b) The G_{BW} at that time (frequency when gain is 0 dB) must be equal to or lower than 1/5 of the switching frequency.

For this reason, switching frequency must be increased to improve responsiveness.

One of the points to secure stability by phase compensation is to cancel secondary phase delay (-180°) generated by LC resonance by the secondary phase lead (i.e. put two phase leads).

Since Gain-BW is determined by the phase compensation capacitor attached to the error amplifier, when it is necessary to reduce Gain-BW, the capacitor should be made larger.

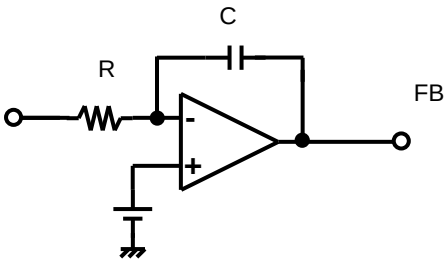
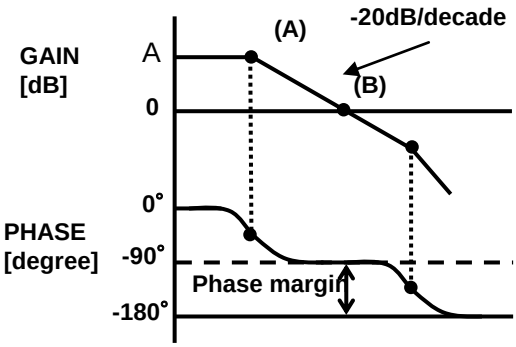


Figure 28. General Integrator

Error AMP is a low-pass filter because phase compensation such as (1) and (2) is performed. For DC/DC converter application, R is a parallel feedback resistance.



$$Point(A) \quad fp = \frac{1}{2\pi RCA} \quad [Hz] \qquad (9)$$

$$Point(B) \quad f_{GBW} = \frac{1}{2\pi RC} \quad [Hz] \qquad (10)$$

Figure 29. Frequency Property of Integrator

Phase compensation when output capacitor with low ESR such as ceramic capacitor is used is as follows:

When output capacitor with low ESR (several tens of mΩ) is used for output, secondary phase lead (two phase leads) must be put to cancel secondary phase lead caused by LC. One of the examples of phase compensation methods is as follows:

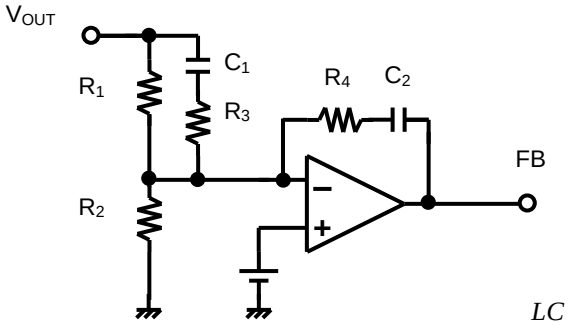


Figure 30. Example of Setting of Phase Compensation

$$Phaselead\ fz1 = \frac{1}{2\pi R_1 C_1} \quad [Hz] \qquad (11)$$

$$Phaselead\ fz2 = \frac{1}{2\pi R_4 C_2} \quad [Hz] \qquad (12)$$

$$Phasedelay\ fp1 = \frac{1}{2\pi R_3 C_1} \quad [Hz] \qquad (13)$$

$$LC\ resonance\ frequency = \frac{1}{2\pi\sqrt{(LCout)}} \quad [Hz] \qquad (14)$$

Cout : Output Capacitor

For setting of phase-lead frequency, both of them should be put near LC resonance frequency.

When G_{BW} frequency becomes too high due to the secondary phase lead, it may get stabilized by putting the primary phase delay in a frequency slightly higher than the LC resonance frequency to compensate it.

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4. Example of Board Layout

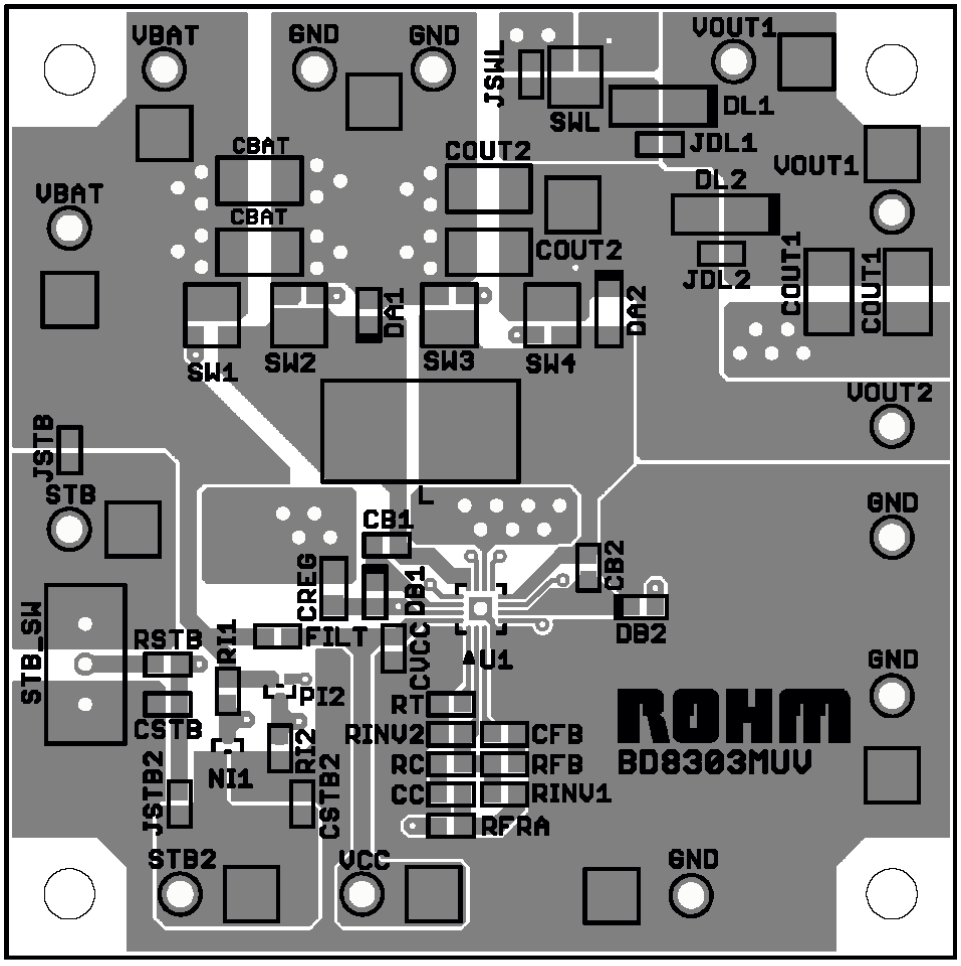
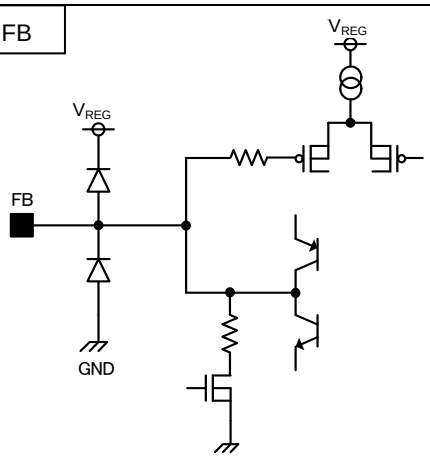


Figure 31. Example of Board Layout

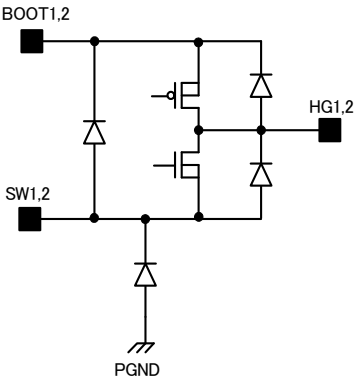
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I/O Equivalent Circuits

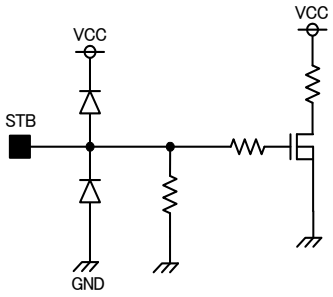
FB



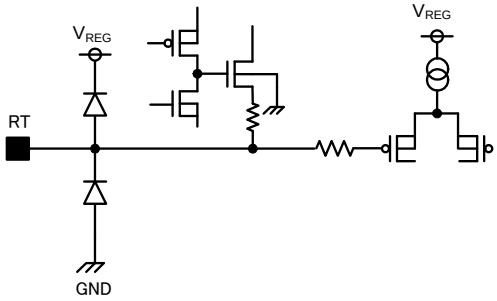
BOOT1
BOOT2
HG1, HG2
SW1, SW2



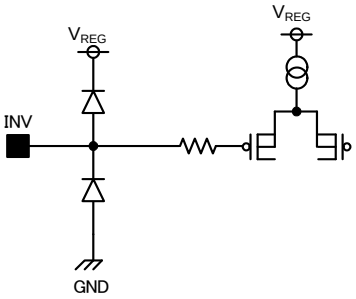
STB



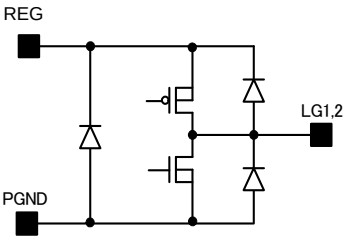
RT



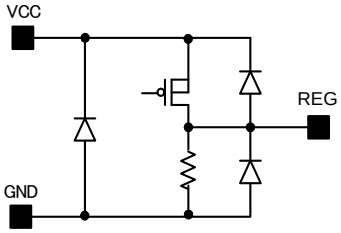
INV



LG1, LG2
PGND



VCC, REG
GND



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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

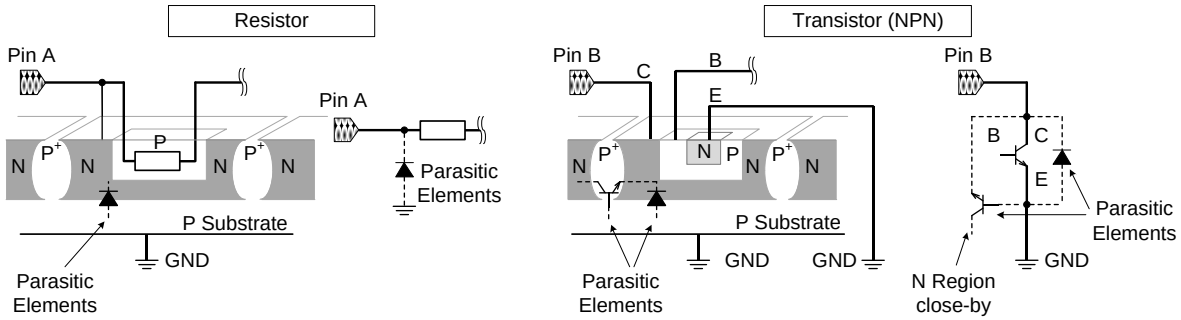


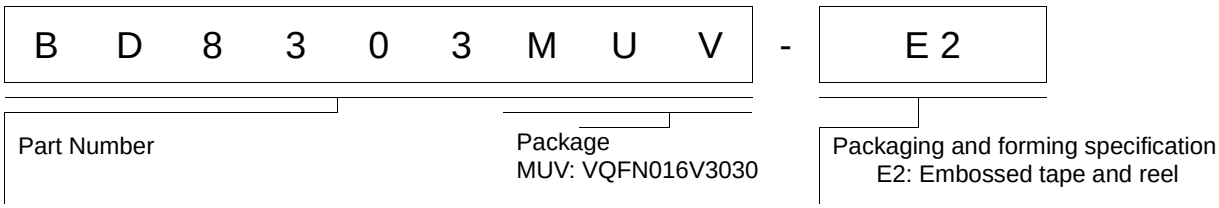
Figure 32. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

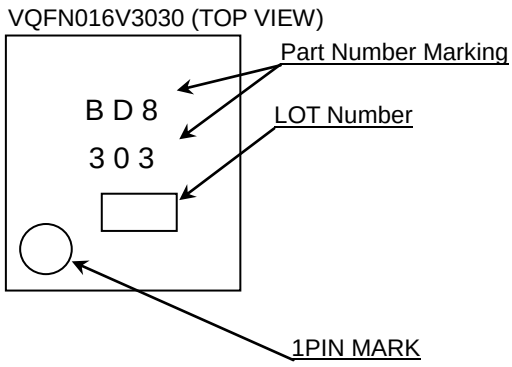
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Ordering Information



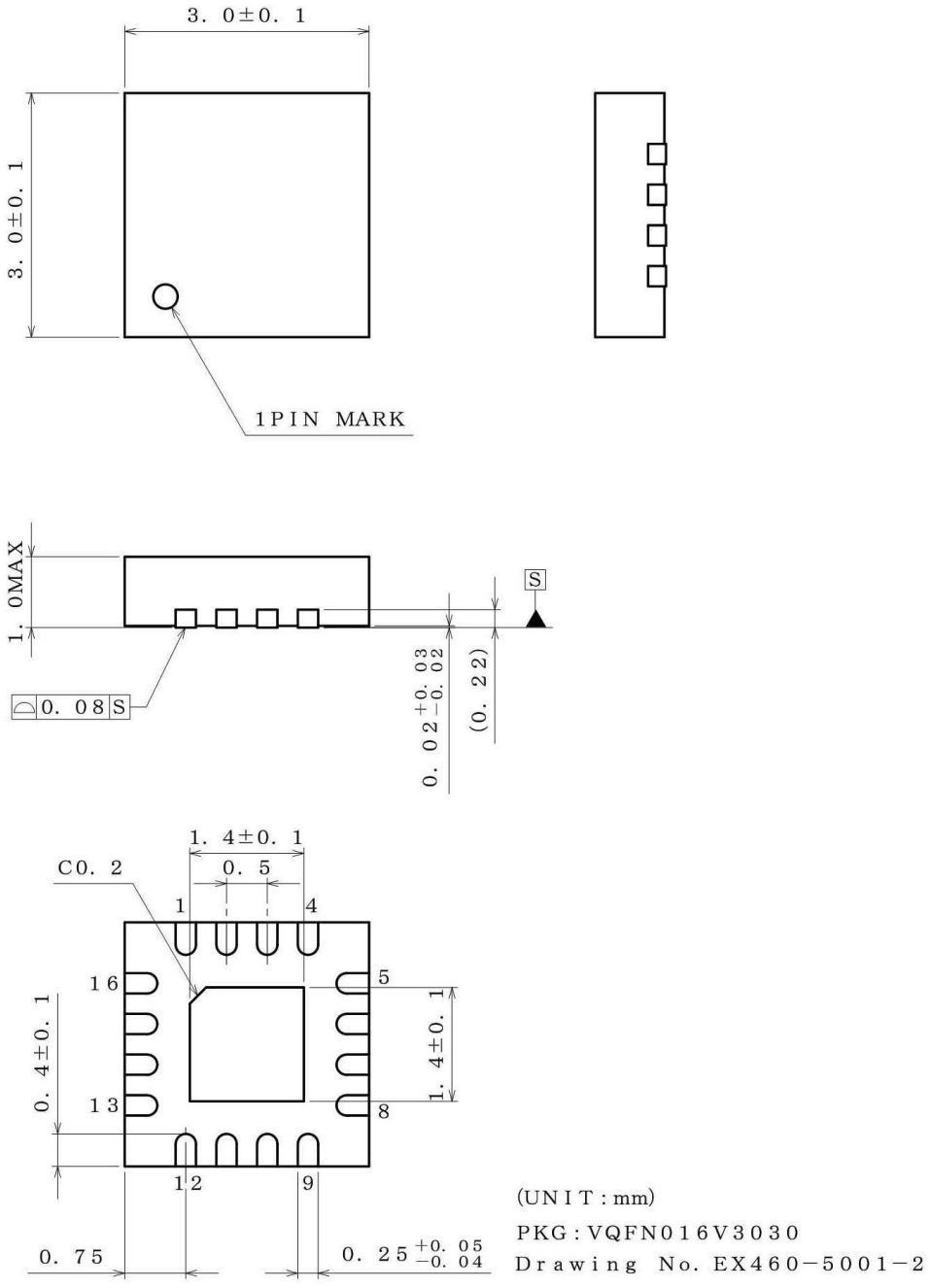
Marking Diagram



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Physical Dimension, Tape and Reel Information

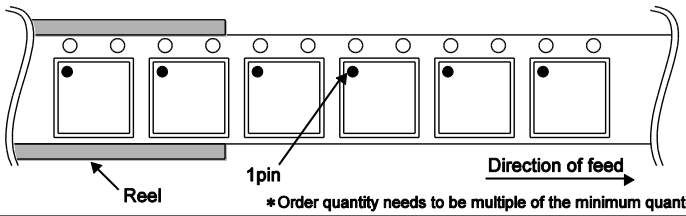
Package Name	VQFN016V3030



(UNIT:mm)
PKG:VQFN016V3030
Drawing No. EX460-5001-2

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
26.Nov.2014	001	New Release
16.Feb.2015	002	Correction of the writing.

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Part Number	BD8303MUV
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Minimum Package Quantity	3000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes