H-bridge Drivers for Brush Motors

18V max. H-bridge Drivers

BD622☐ Series

No.10007EDT02

●Overview

These H-bridge drivers are full bridge drivers for brush motor applications. Each IC can operate at a wide range of power supply voltages (from 3V to 36V), supporting output currents of up to 2A. MOS transistors in the output stage allow for PWM signal control, while the integrated VREF voltage control function of previous models offers direct replacement of deprecated motor driver ICs. These highly efficient H-bridge driver ICs facilitate low-power consumption design.

●Features

1) Built-in, selectable one channel or two channels configuration
2) Low standby current
3) Supports PWM control signal input (20kHz to 100kHz)
4) VREF voltage setting pin enables PWM duty control
5) Cross-conduction prevention circuit
6) Four protection circuits provided: OCP, OVP, TSD and UVLO

●Applications

VCR; CD/DVD players; audio-visual equipment; optical disc drives; PC peripherals; car audios; car navigation systems; OA equipments

●Line up matrix

Rating voltage	Channels	Maximum output current		
		0.5A	1.0A	2.0A
7V	1ch	BD6210 HFP / F	BD6211 HFP / F	BD6212 HFP / FP
	2ch	BD6215 FP	BD6216 FP / FM	BD6217 FM
18V	1ch	BD6220 HFP / F	BD6221 HFP / F	BD6222 HFP / FP
	2ch	BD6225 FP	BD6226 FP / FM	
36V	1ch	BD6230 HFP / F	BD6231 HFP / F	BD6232 HFP / FP
	2ch	BD6235 FP	BD6236 FP / FM	BD6237 FM

*Packages; F:SOP8, HFP:HRP7, FP:HSOP25, FM:HSOP-M28

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●**Absolute maximum ratings** (Ta=25°C, All voltages are with respect to ground)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	18	V
Output current	I_{OMAX}	0.5 *1 / 1.0 *2 / 2.0 *3	A
All other input pins	V_{IN}	-0.3 ~ VCC	V
Operating temperature	T_{OPR}	-40 ~ +85	°C
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	Pd	0.687 *4 / 1.4 *5 / 1.45 *6 / 2.2 *7	W
Junction temperature	T_{jmax}	150	°C

*1 BD6220 / BD6225. Do not, exceed Pd or ASO.
*2 BD6221 / BD6226. Do not, exceed Pd or ASO.
*3 BD6222. Do not, exceed Pd or ASO.
*4 SOP8 package. Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 5.5mW/°C above 25°C.
*5 HRP7 package. Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 11.2mW/°C above 25°C.
*6 HSOP25 package. Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 11.6mW/°C above 25°C.
*7 HSOP-M28 package. Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 17.6mW/°C above 25°C.

●**Operating conditions** (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	6 ~ 15	V
VREF voltage	VREF	3 ~ 15	V

●**Electrical characteristics** (Unless otherwise specified, Ta=25°C and VCC=VREF=12V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Min.	Min.		
Supply current (1ch)	I_{CC}	0.8	1.3	2.5	mA	Forward / Reverse / Brake
Supply current (2ch)	I_{CC}	1.3	2.0	3.5	mA	Forward / Reverse / Brake
Stand-by current	I_{STBY}	-	0	10	μA	Stand-by
Input high voltage	V_{IH}	2.0	-	-	V	
Input low voltage	V_{IL}	-	-	0.8	V	
Input bias current	I_{IH}	30	50	100	μA	V_{IN}=5.0V
Output ON resistance *1	R_{ON}	1.0	1.5	2.5	Ω	I_O=0.25A, vertically total
Output ON resistance *2	R_{ON}	1.0	1.5	2.5	Ω	I_O=0.5A, vertically total
Output ON resistance *3	R_{ON}	0.5	1.0	1.5	Ω	I_O=1.0A, vertically total
VREF bias current	I_{VREF}	-10	0	10	μA	VREF=VCC
Carrier frequency	F_{PWM}	20	25	35	kHz	VREF=9V
Input frequency range	F_{MAX}	20	-	100	kHz	FIN / RIN

*1 BD6220 / BD6225
*2 BD6221 / BD6226
*3 BD6222

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●Electrical characteristic curves (Reference data)

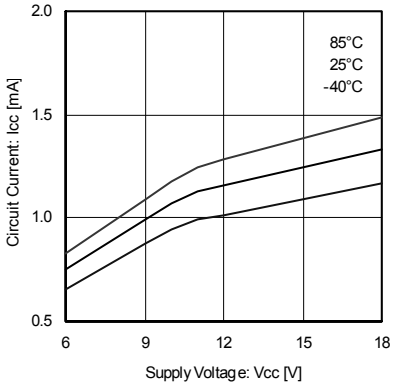


Fig.1 Supply current (1ch)

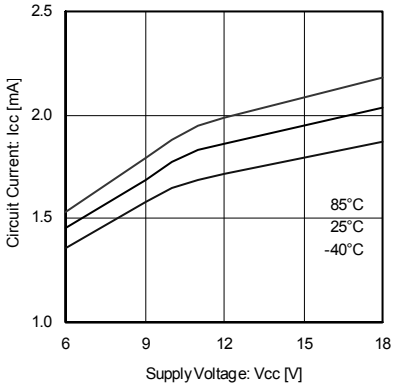


Fig.2 Supply current (2ch)

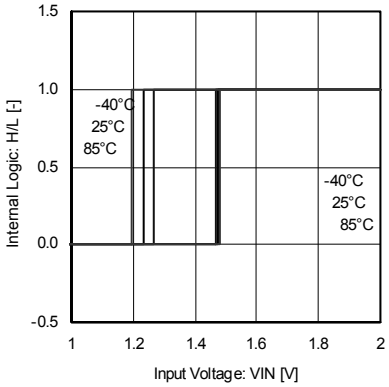


Fig.3 Input threshold voltage

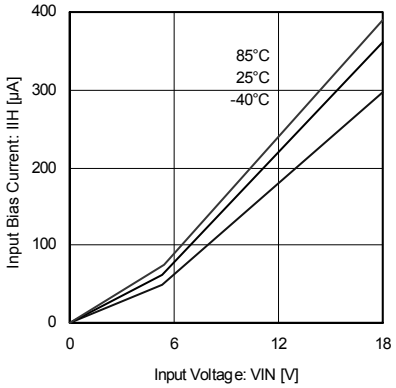


Fig.4 Input bias current

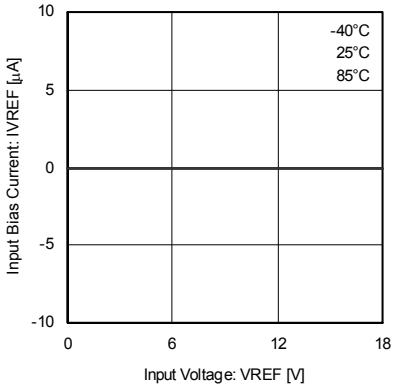


Fig.5 VREF input bias current

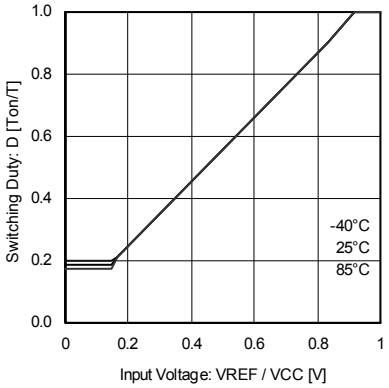


Fig.6 VREF - DUTY (VCC=12V)

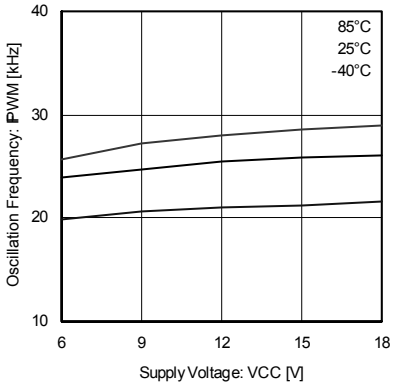


Fig.7 VCC - Carrier frequency

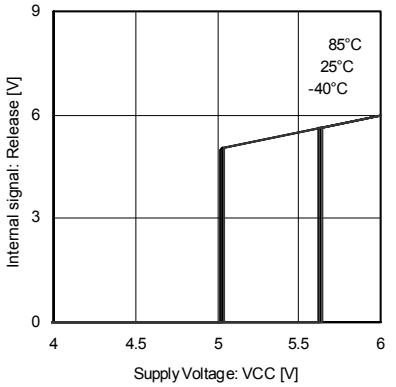


Fig.8 Under voltage lock out

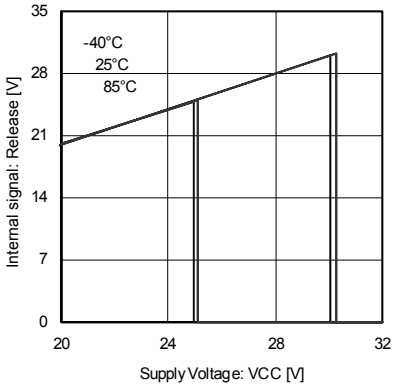


Fig.9 Over voltage protection

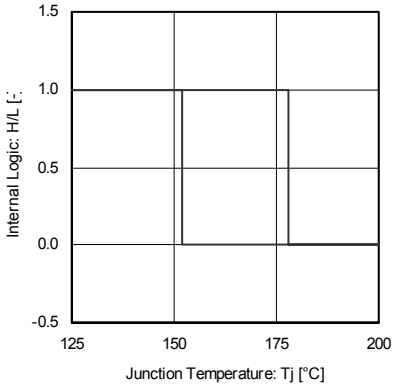


Fig.10 Thermal shutdown

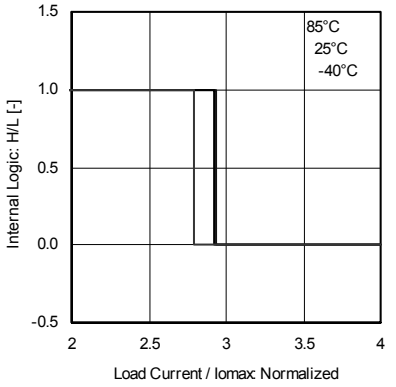


Fig.11 Over current protection (H side)

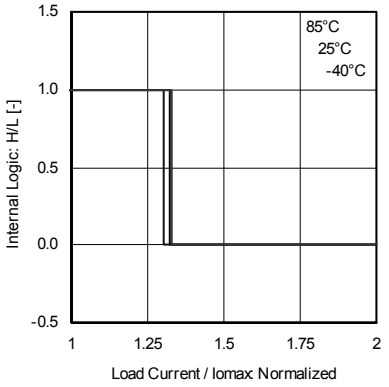


Fig.12 Over current protection (L side)

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●**Electrical characteristic curves (Reference data)** - Continued

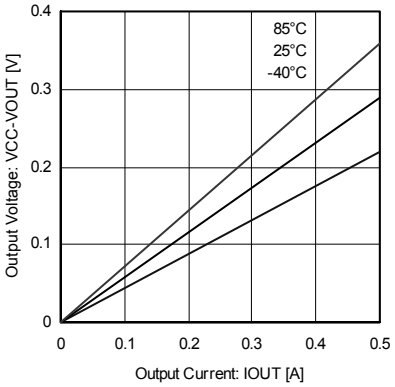


Fig.13 Output high voltage (0.5A class)

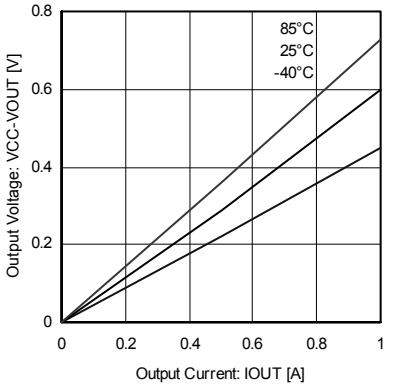


Fig.14 Output high voltage (1A class)

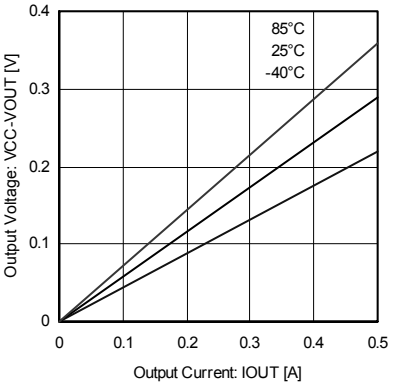


Fig.15 Output high voltage (2A class)

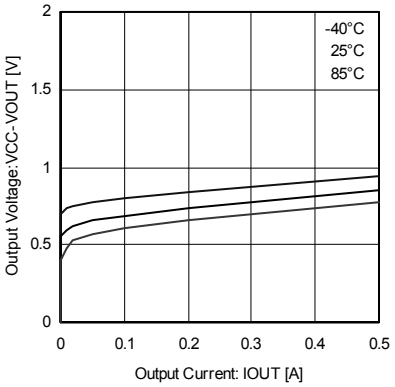


Fig.16 High side body diode (0.5A class)

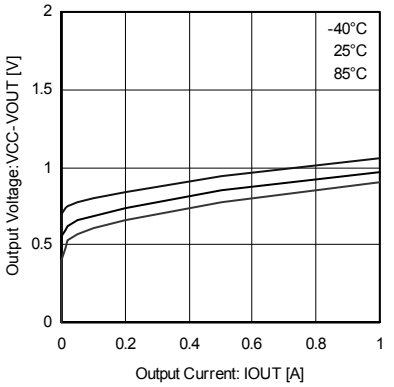


Fig.17 High side body diode (1A class)

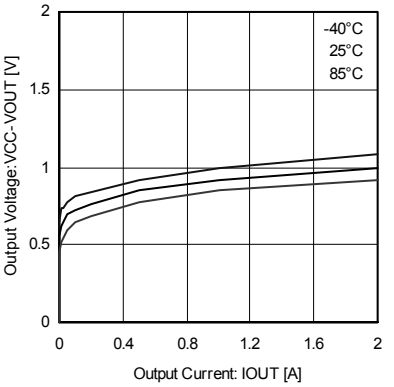


Fig.18 High side body diode (2A class)

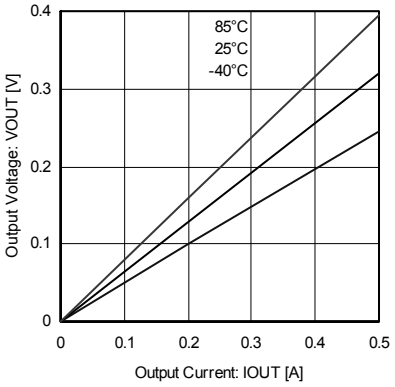


Fig.19 Output low voltage (0.5A class)

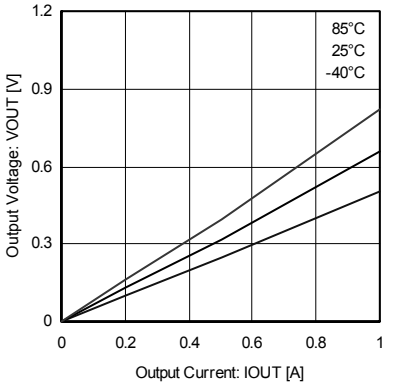


Fig.20 Output low voltage (1A class)

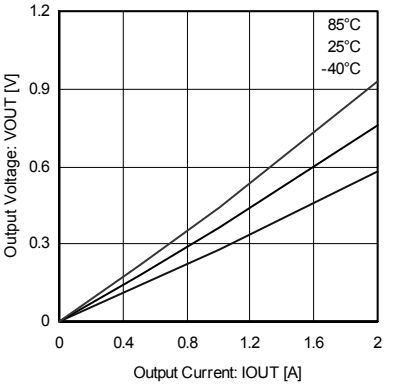


Fig.21 Output low voltage (2A class)

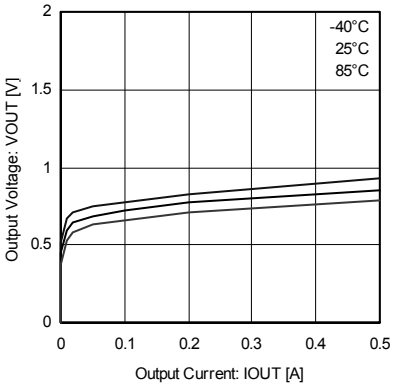


Fig.22 Low side body diode (0.5A class)

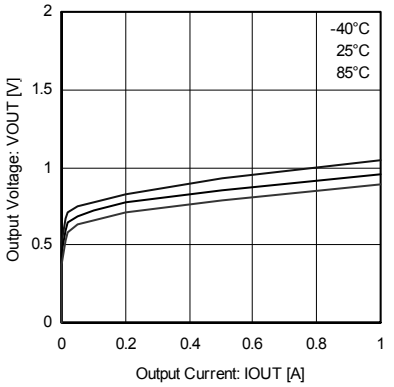


Fig.23 Low side body diode (1A class)

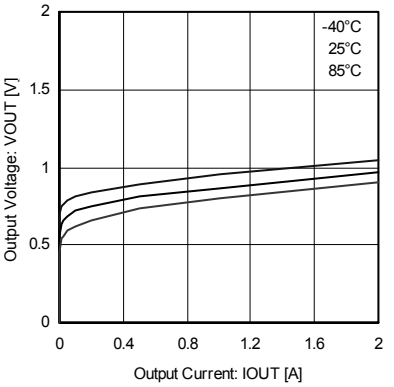


Fig.24 Low side body diode (2A class)

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●Block diagram and pin configuration

BD6220F / BD6221F

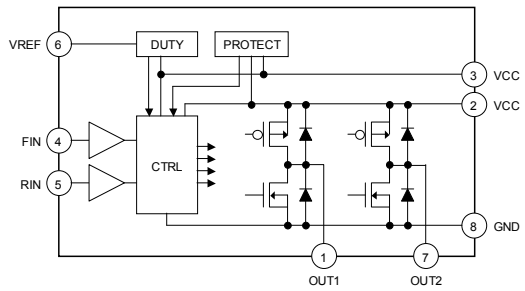


Fig.25 BD6220F / BD6221F

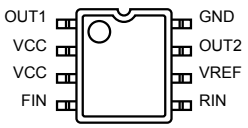


Fig.26 SOP8

Table 1 BD6220F/BD6221F

Pin	Name	Function
1	OUT1	Driver output
2	VCC	Power supply
3	VCC	Power supply
4	FIN	Control input (forward)
5	RIN	Control input (reverse)
6	VREF	Duty setting pin
7	OUT2	Driver output
8	GND	Ground

Note: Use all VCC pin by the same voltage.

BD6220HFP / BD6221HFP / BD6222HFP

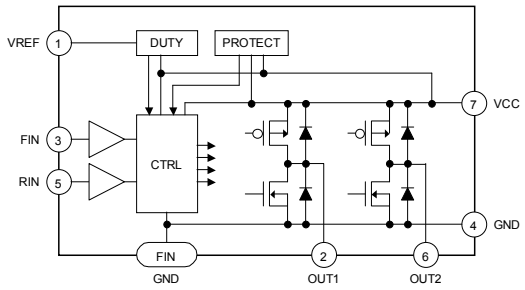


Fig.27 BD6220HFP / BD6221HFP / BD6222HFP

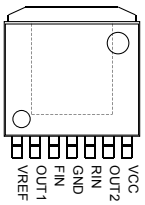


Fig.28 HRP7

Table 2 BD6220HFP/BD6221HFP/BD6222HFP

Pin	Name	Function
1	VREF	Duty setting pin
2	OUT1	Driver output
3	FIN	Control input (forward)
4	GND	Ground
5	RIN	Control input (reverse)
6	OUT2	Driver output
7	VCC	Power supply
FIN	GND	Ground

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●**Block diagram and pin configuration** - Continued

BD6222FP

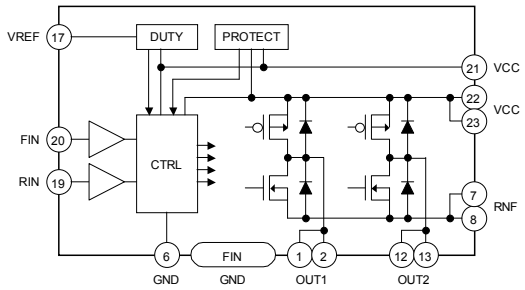


Fig.29 BD6222FP

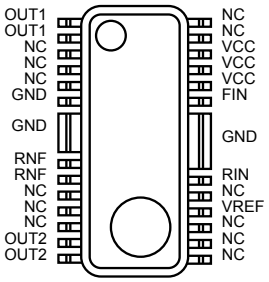


Fig.30 HSOP25

Table 3 BD6222FP

Pin	Name	Function
1,2	OUT1	Driver output
6	GND	Small signal ground
7,8	RNF	Power stage ground
12,13	OUT2	Driver output
17	VREF	Duty setting pin
19	RIN	Control input (reverse)
20	FIN	Control input (forward)
21	VCC	Power supply
22,23	VCC	Power supply
FIN	GND	Ground

Note: All pins not described above are NC pins.
Use all VCC pin by the same voltage.

BD6225FP / BD6226FP

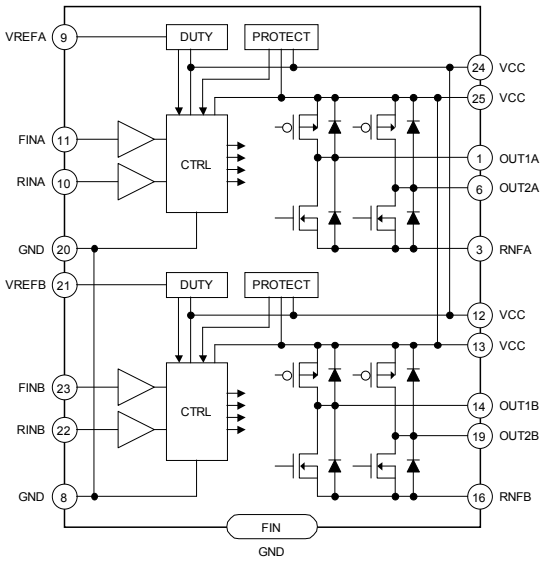


Fig.31 BD6225FP / BD6226FP

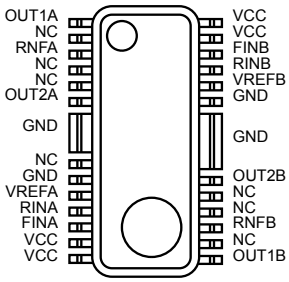


Fig.32 HSOP25

Table 4 BD6225FP / BD6226FP

Pin	Name	Function
1	OUT1A	Driver output
3	RNFA	Power stage ground
6	OUT2A	Driver output
8	GND	Small signal ground
9	VREFA	Duty setting pin
10	RINA	Control input (reverse)
11	FINA	Control input (forward)
12	VCC	Power supply
13	VCC	Power supply
14	OUT1B	Driver output
16	RNFB	Power stage ground
19	OUT2B	Driver output
20	GND	Small signal ground
21	VREFB	Duty setting pin
22	RINB	Control input (reverse)
23	FINB	Control input (forward)
24	VCC	Power supply
25	VCC	Power supply
FIN	GND	Ground

Note: All pins not described above are NC pins.
Use all VCC pin by the same voltage.

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●**Block diagram and pin configuration** - Continued

BD6226FM

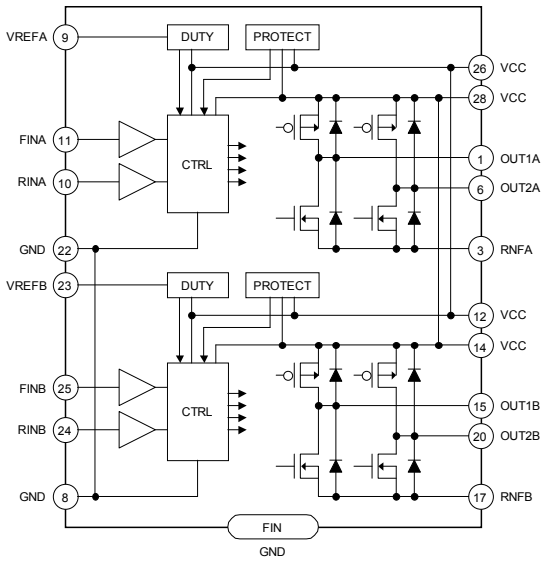


Fig.33 BD6226FM

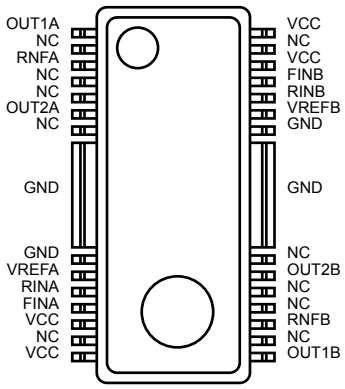


Fig.34 HSOP-M28

Table 5 BD6226FM

Pin	Name	Function
1	OUT1A	Driver output
3	RNFA	Power stage ground
6	OUT2A	Driver output
8	GND	Small signal ground
9	VREFA	Duty setting pin
10	RINA	Control input (reverse)
11	FINA	Control input (forward)
12	VCC	Power supply
14	VCC	Power supply
15	OUT1B	Driver output
17	RNFB	Power stage ground
20	OUT2B	Driver output
22	GND	Small signal ground
23	VREFB	Duty setting pin
24	RINB	Control input (reverse)
25	FINB	Control input (forward)
26	VCC	Power supply
28	VCC	Power supply
FIN	GND	Ground

Note: All pins not described above are NC pins.
Use all VCC pin by the same voltage.

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●Functional descriptions

1) Operation modes

Table 6 Logic table

	FIN	RIN	VREF	OUT1	OUT2	Operation
a	L	L	X	Hi-Z*	Hi-Z*	Stand-by (idling)
b	H	L	VCC	H	L	Forward (OUT1 > OUT2)
c	L	H	VCC	L	H	Reverse (OUT1 < OUT2)
d	H	H	X	L	L	Brake (stop)
e	PWM	L	VCC	H	$\overline{PWM}$	Forward (PWM control mode A)
f	L	PWM	VCC	$\overline{PWM}$	H	Reverse (PWM control mode A)
g	H	PWM	VCC	$\overline{PWM}$	L	Forward (PWM control mode B)
h	PWM	H	VCC	L	$\overline{PWM}$	Reverse (PWM control mode B)
i	H	L	Option	H	$\overline{PWM}$	Forward (VREF control)
j	L	H	Option	$\overline{PWM}$	H	Reverse (VREF control)

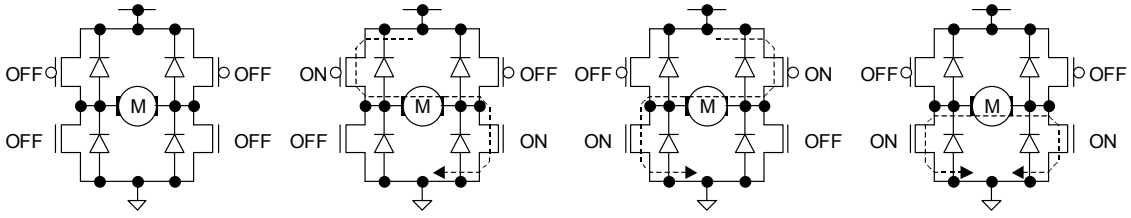
* Hi-Z is the off state of all output transistors. Please note that this is the state of the connected diodes, which differs from that of the mechanical relay.
X : Don't care

a) Stand-by mode
Stand-by operates independently of the VREF pin voltage. In stand-by mode, all internal circuits are turned off, including the output power transistors. Motor output goes to high impedance. If the motor is running at the switch to stand-by mode, the system enters an idling state because of the body diodes. However, when the system switches to stand-by from any other mode (except the brake mode), the control logic remains in the high state for at least 50μs before shutting down all circuits.

b) Forward mode
This operating mode is defined as the forward rotation of the motor when the OUT1 pin is high and OUT2 pin is low. When the motor is connected between the OUT1 and OUT2 pins, the current flows from OUT1 to OUT2. For operation in this mode, connect the VREF pin with VCC pin.

c) Reverse mode
This operating mode is defined as the reverse rotation of the motor when the OUT1 pin is low and OUT2 pin is high. When the motor is connected between the OUT1 and OUT2 pins, the current flows from OUT2 to OUT1. For operation in this mode, connect the VREF pin with VCC pin.

d) Brake mode
This operating mode is used to quickly stop the motor (short circuit brake). It differs from the stand-by mode because the internal control circuit is operating in the brake mode. Please switch to the stand-by mode (rather than the brake mode) to save power and reduce consumption.



a) Stand-by mode b) Forward mode c) Reverse mode d) Brake mode

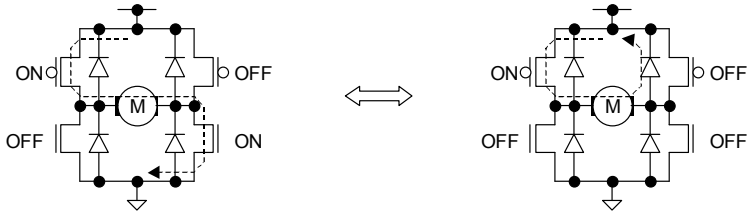
Fig.35 Four basic operations (output stage)

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e) f) PWM control mode A

The rotational speed of the motor can be controlled by the switching duty when the PWM signal is input to the FIN pin or the RIN pin. In this mode, the high side output is fixed and the low side output does the switching, corresponding to the input signal. The switching operates by the output state toggling between "L" and "Hi-Z".

The PWM frequency can be input in the range between 20kHz and 100kHz. Note that control may not be attained by switching on duty at frequencies lower than 20kHz, since the operation functions via the stand-by mode. Also, circuit operation may not respond correctly when the input signal is higher than 100kHz. To operate in this mode, connect the VREF pin with VCC pin. In addition, establish a current path for the recovery current from the motor, by connecting a bypass capacitor (10μF or more is recommended) between VCC and ground.



Control input : H Control input : L

Fig.36 PWM control mode A operation (output stage)

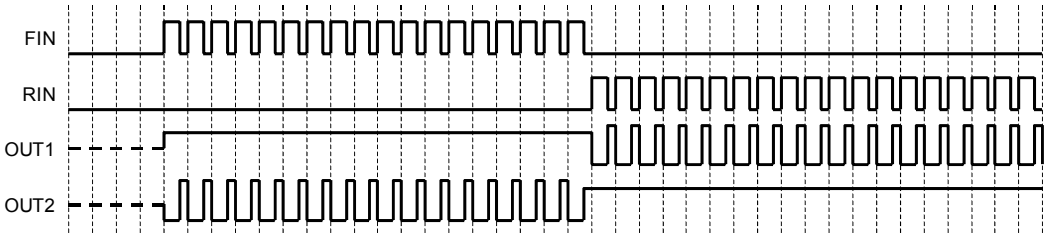
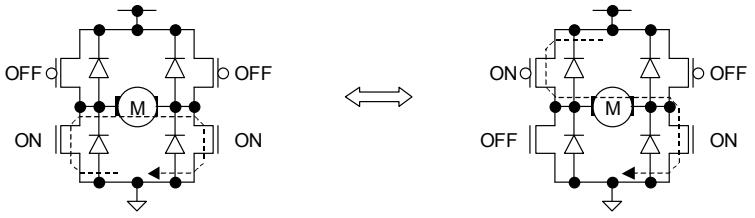


Fig.37 PWM control mode A operation (timing chart)

g) h) PWM control mode B

The rotational speed of the motor can be controlled by the switching duty when the PWM signal is input to the FIN pin or the RIN pin. In this mode, the low side output is fixed and the high side output does the switching, corresponding to the input signal. The switching operates by the output state toggling between "L" and "H".

The PWM frequency can be input in the range between 20kHz and 100kHz. Also, circuit operation may not respond correctly when the input signal is higher than 100kHz. To operate in this mode, connect the VREF pin with VCC pin. In addition, establish a current path for the recovery current from the motor, by connecting a bypass capacitor (10μF or more is recommended) between VCC and ground.



Control input : H Control input : L

Fig.38 PWM control mode B operation (output stage)

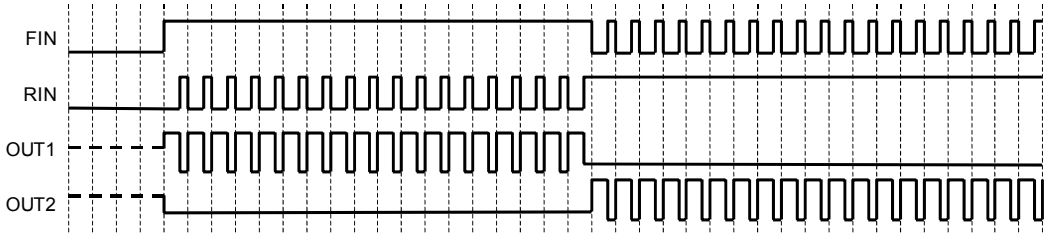


Fig.39 PWM control mode B operation (timing chart)

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i) j) VREF control mode

The built-in VREF-switching on duty conversion circuit provides switching duty corresponding to the voltage of the VREF pin and the VCC voltage. The function offers the same level of control as the high voltage output setting function in previous models. The on duty is shown by the following equation.

DUTY ≈ VREF [V] / VCC [V]

For example, if VCC voltage is 12V and VREF pin voltage is 9V, the switching on duty is about 75 percent. However, please note that the switching on duty might be limited by the range of VREF pin voltage (Refer to the operating conditions, shown on page 2). The PWM carrier frequency in this mode is 25kHz (nominal), and the switching operation is the same as it is the PWM control modes. When operating in this mode, do not input the PWM signal to the FIN and RIN pins. In addition, establish a current path for the recovery current from the motor, by connecting a bypass capacitor (10μF or more is recommended) between VCC and ground.

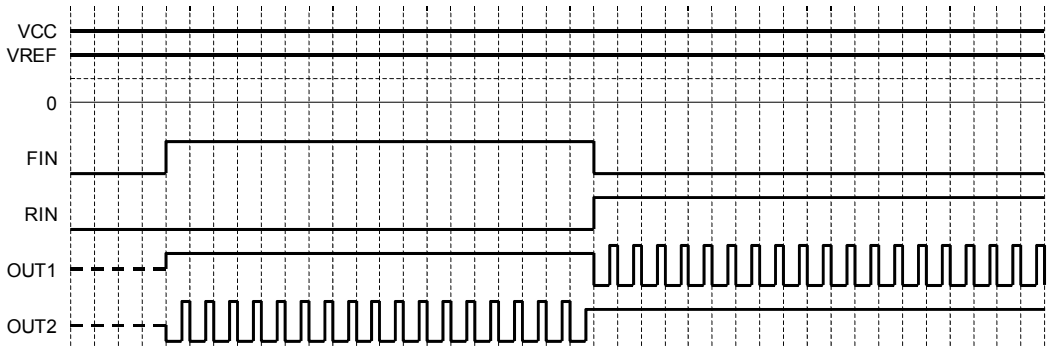


Fig.40 VREF control operation (timing chart)

2) Cross-conduction protection circuit

In the full bridge output stage, when the upper and lower transistors are turned on at the same time, and this condition exists during the period of transition from high to low, or low to high, a rush current flows from the power supply to ground, resulting in a loss. This circuit protects against the rush current by providing a dead time (about 400ns, nominal) at the transition.

3) Output protection circuits

a) Under voltage lock out (UVLO) circuit

To secure the lowest power supply voltage necessary to operate the controller, and to prevent under voltage malfunctions, a UVLO circuit has been built into this driver. When the power supply voltage falls to 5.0V (nominal) or below, the controller forces all driver outputs to high impedance. When the voltage rises to 5.5V (nominal) or above, the UVLO circuit ends the lockout operation and returns the chip to normal operation.

b) Over voltage protection (OVP) circuit

When the power supply voltage exceeds 30V (nominal), the controller forces all driver outputs to high impedance. The OVP circuit is released and its operation ends when the voltage drops back to 25V (nominal) or below. This protection circuit does not work in the stand-by mode. Also, note that this circuit is supplementary, and thus if it is asserted, the absolute maximum rating will have been exceeded. Therefore, do not continue to use the IC after this circuit is activated, and do not operate the IC in an environment where activation of the circuit is assumed.

c) Thermal shutdown (TSD) circuit

The TSD circuit operates when the junction temperature of the driver exceeds the preset temperature (175°C nominal). At this time, the controller forces all driver outputs to high impedance. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature (150°C nominal). Thus, it is a self-returning type circuit.

The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not operate the IC in an environment where activation of the circuit is assumed.

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d) Over current protection (OCP) circuit

To protect this driver IC from ground faults, power supply line faults and load short circuits, the OCP circuit monitors the output current for the circuit's monitoring time (10μs, nominal). When the protection circuit detects an over current, the controller forces all driver outputs to high impedance during the off time (290μs, nominal). The IC returns to normal operation after the off time period has elapsed (self-returning type). At the two channels type, this circuit works independently for each channel.

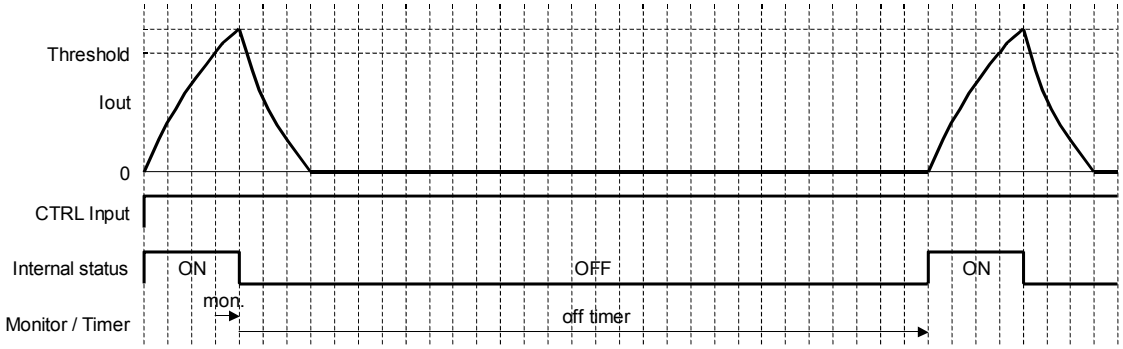


Fig.41 Over current protection (timing chart)

●Interfaces

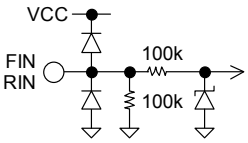


Fig.42 FIN / RIN

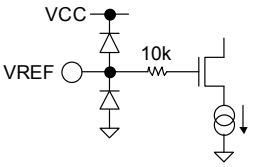


Fig.43 VREF

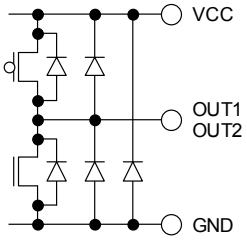


Fig.44 OUT1 / OUT2
(SOP8/HRP7)

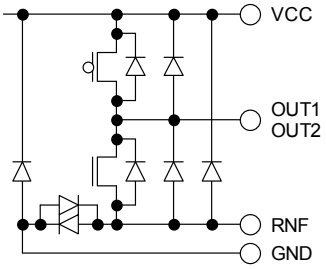


Fig.45 OUT1 / OUT2
(HSOP25/HSOPM28)

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●Notes for use

1) **Absolute maximum ratings**
Devices may be destroyed when supply voltage or operating temperature exceeds the absolute maximum rating. Because the cause of this damage cannot be identified as, for example, a short circuit or an open circuit, it is important to consider circuit protection measures – such as adding fuses – if any value in excess of absolute maximum ratings is to be implemented.

2) **Connecting the power supply connector backward**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply lines, such as adding an external direction diode.

3) **Power supply lines**
Return current generated by the motor's Back-EMF requires countermeasures, such as providing a return current path by inserting capacitors across the power supply and GND (10μF, ceramic capacitor is recommended). In this case, it is important to conclusively confirm that none of the negative effects sometimes seen with electrolytic capacitors – including a capacitance drop at low temperatures - occurs. Also, the connected power supply must have sufficient current absorbing capability. Otherwise, the regenerated current will increase voltage on the power supply line, which may in turn cause problems with the product, including peripheral circuits exceeding the absolute maximum rating. To help protect against damage or degradation, physical safety measures should be taken, such as providing a voltage clamping diode across the power supply and GND.

4) **Electrical potential at GND**
Keep the GND terminal potential to the minimum potential under any operating condition. In addition, check to determine whether there is any terminal that provides voltage below GND, including the voltage during transient phenomena. When both a small signal GND and high current GND are present, single-point grounding (at the set's reference point) is recommended, in order to separate the small signal and high current GND, and to ensure that voltage changes due to the wiring resistance and high current do not affect the voltage at the small signal GND. In the same way, care must be taken to avoid changes in the GND wire pattern in any external connected component.

5) **Thermal design**
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) under actual operating conditions.

6) **Inter-pin shorts and mounting errors**
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error, or if pins are shorted together.

7) **Operation in strong electromagnetic fields**
Using this product in strong electromagnetic fields may cause IC malfunctions. Use extreme caution with electromagnetic fields.

8) **ASO - Area of Safety Operation**
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9) **Built-in thermal shutdown (TSD) circuit**
The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not operate the IC in an environment where activation of the circuit is assumed.

10) **Capacitor between output and GND**
In the event a large capacitor is connected between the output and GND, if VCC and VIN are short-circuited with 0V or GND for any reason, the current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1μF between output and GND.

11) **Testing on application boards**
When testing the IC on an application board, connecting a capacitor to a low impedance pin subjects the IC to stress. Therefore, always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from the test setup during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

12) **Switching noise**
When the operation mode is in PWM control or VREF control, PWM switching noise may effects to the control input pins and cause IC malfunctions. In this case, insert a pulled down resistor (10kΩ is recommended) between each control input pin and ground.

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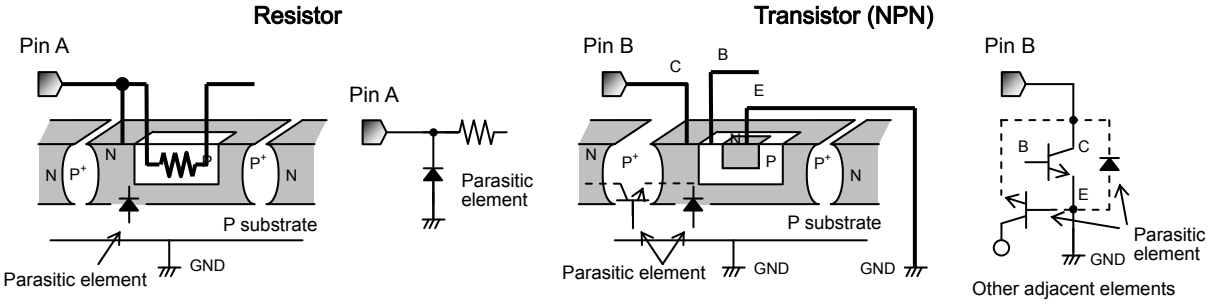
13) Regarding the input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements, in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, do not use methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.



Appendix: Example of monolithic IC structure

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●Ordering part number

B	D	6	2	2	0	F		-	E	2

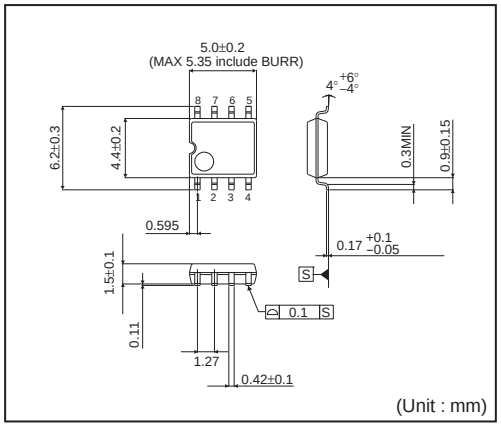
ROHM part number

Type
1X: 7V max.
2X: 18V max.
3X: 36V max.
X0: 1ch/0.5A X5: 2ch/0.5A
X1: 1ch/1A X6: 2ch/1A
X2: 1ch/2A

Package
F: SOP8
FP: HSOP25
FM: HSOP-M28
HFP: HRP7

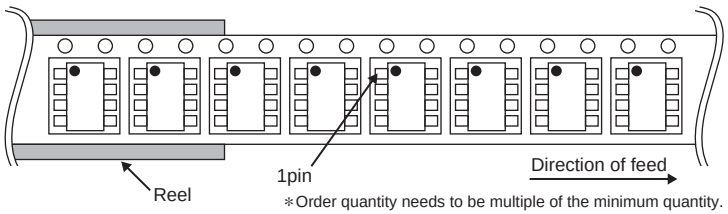
Packaging spec.
E2: Embossed taping (SOP8/HSOP25/HSOP-M28)
TR: Embossed taping (HRP7)

SOP8



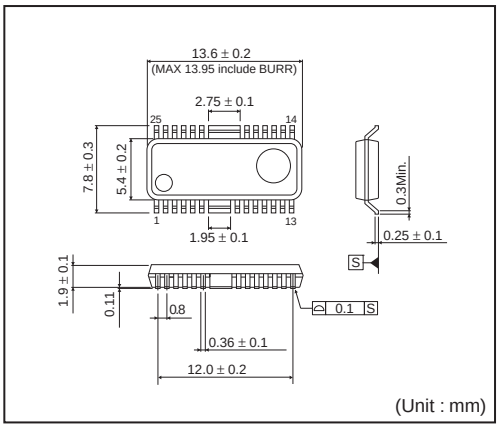
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



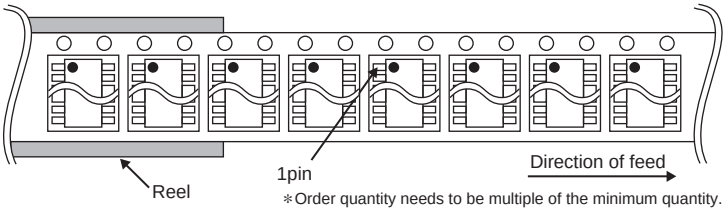
∗Order quantity needs to be multiple of the minimum quantity.

HSOP25



<Tape and Reel information>

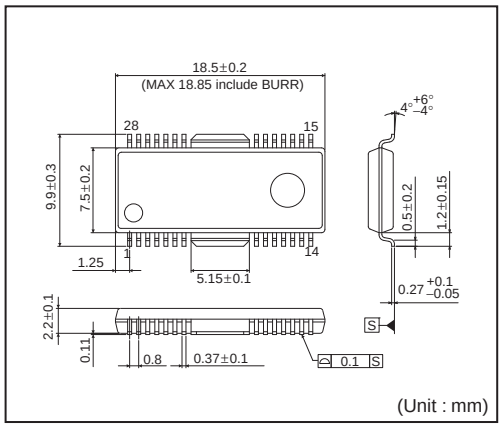
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

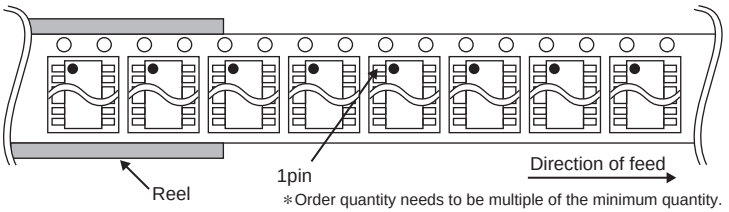
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HSOP-M28



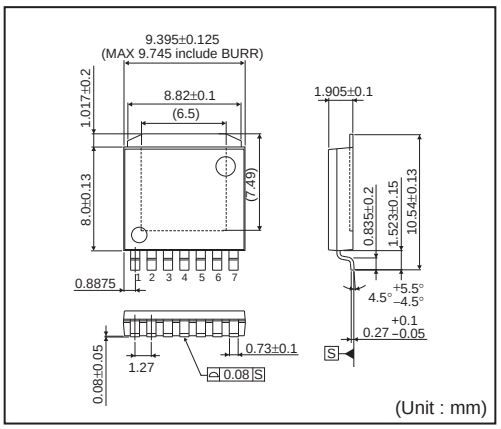
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



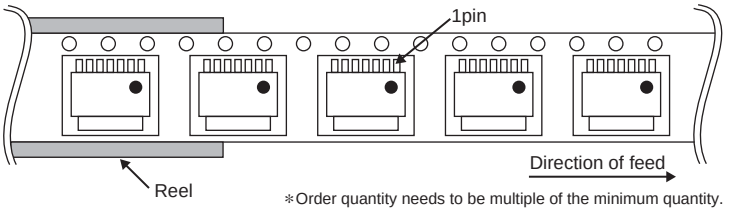
∗Order quantity needs to be multiple of the minimum quantity.

HRP7



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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