Automotive 1.0A Variable Output LDO Regulator

BDxxHC0MEFJ-M

●General Description

BDxxHC0MEFJ-M is a LDO regulator with output current 1.0A. The output accuracy is ±1% of output voltage. With external resistance, it is available to set the output voltage at random (from 1.5V to 7.0V).It has package type: HTSOP-J8. Over current protection (for protecting the IC destruction by output short circuit), circuit current ON/OFF switch (for setting the circuit 0μA at shutdown mode), and thermal shutdown circuit (for protecting IC from heat destruction by over load condition) are all built in. It is usable for ceramic capacitor and enables to improve smaller set and long-life.

●Features

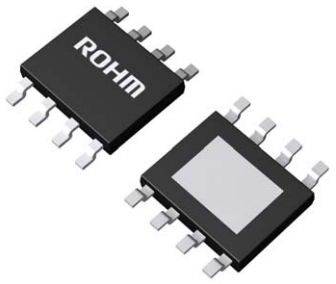
- High accuracy reference voltage circuit
- Built-in Over Current Protection circuit (OCP)
- Built-in Thermal Shut Down circuit (TSD)
- With shut down switch
- AEC-Q100 Qualified

●Key Specifications

- Input power supply voltage range: 4.5V to 8.0V
- Output voltage range(Variable type): 1.5V to 7.0V
- Output voltage(Fixed type): 1.5V/1.8V/2.5V/3.0V/3.3V 5.0V/6.0V/7.0V
- Output current: 1.0A (Max.)
- Shutdown current: 0μA(Typ.)
- Operating temperature range: -40℃ to +105℃

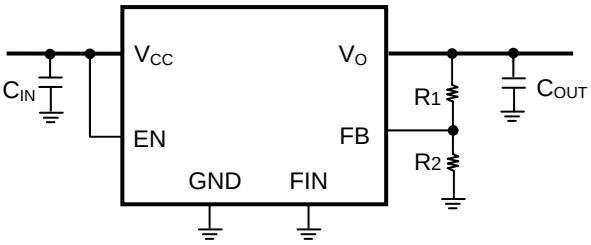
●パッケージ

	(Typ.)	(Typ.)	(Max.)
HTSOP-J8	4.90mm x 6.00mm x 1.00mm		

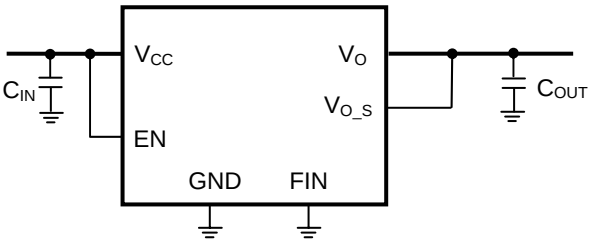


HTSOP-J8

●Typical Application Circuit



C_{IN},C_{OUT} : Ceramic Capacitor



C_{IN},C_{OUT} : Ceramic Capacitor

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

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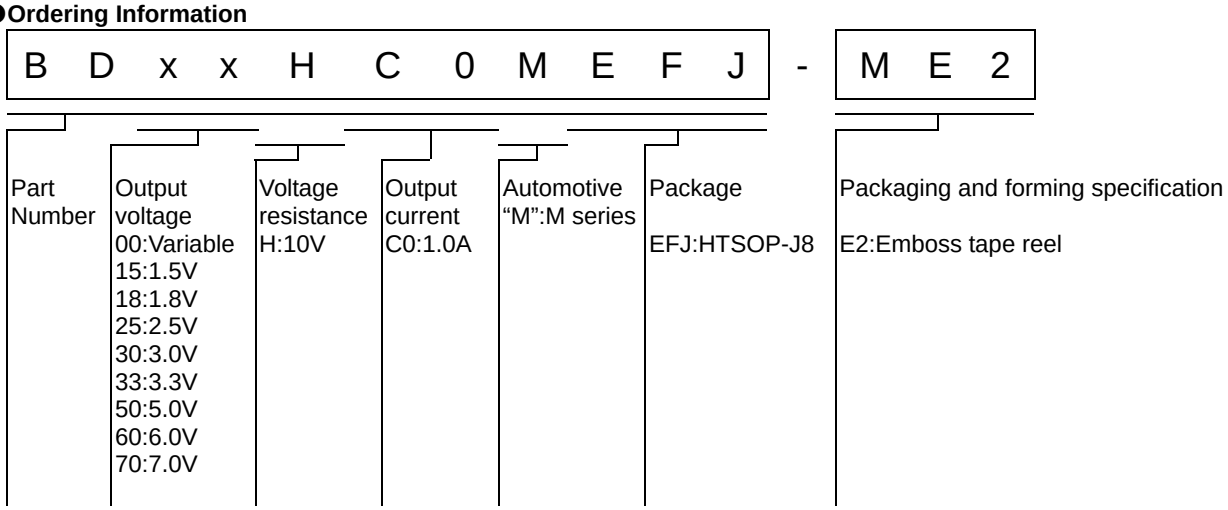
●**Ordering Information**



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●Block Diagram

BD00HC0MEFJ-M

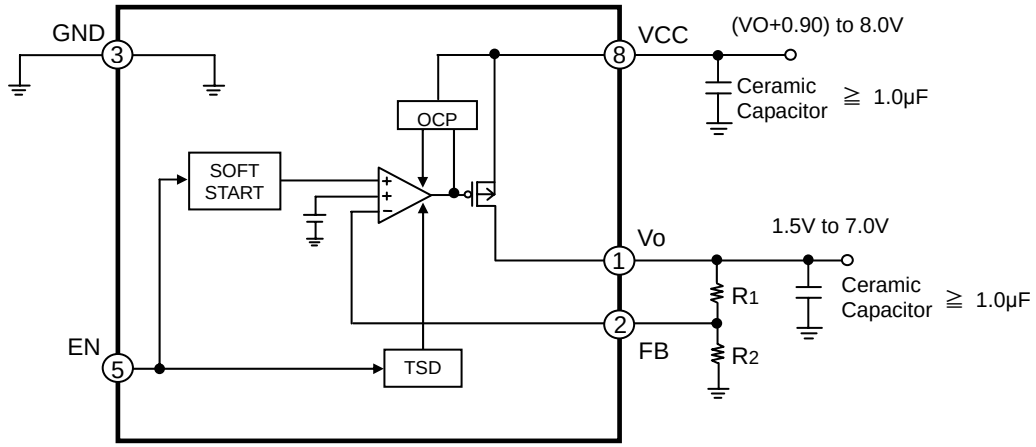


Fig.1 Block Diagram

BDxxHC0MEFJ-M (Fixed type)

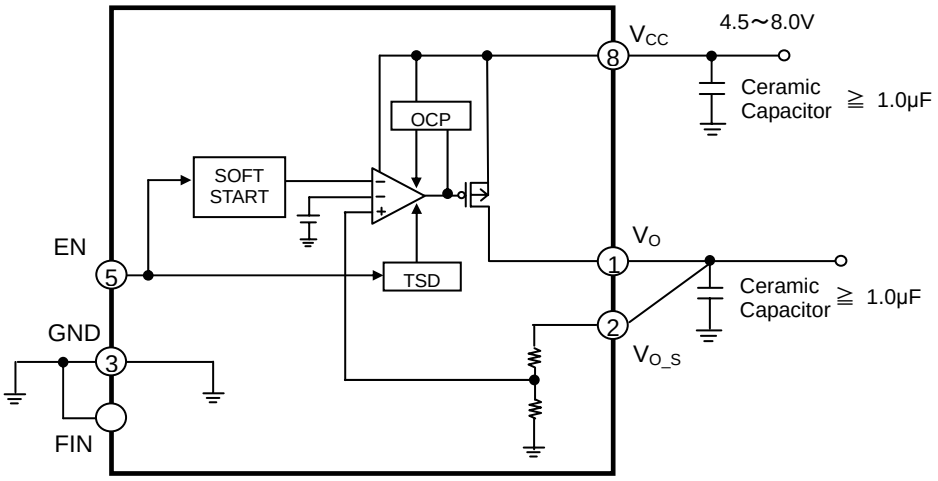
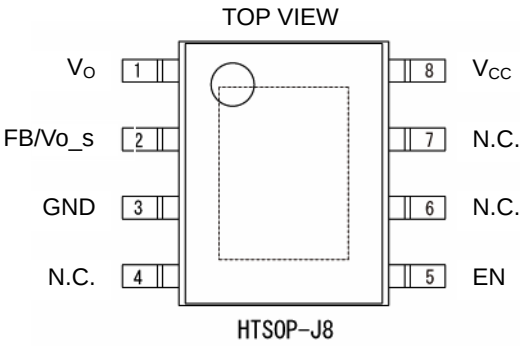


Fig.2 Block Diagram (Fixed type)

●Pin Configuration



●Pin Description

Pin No.	Pin name	Pin Function
1	V_O	Output pin
2	FB/Vo_s	Feedback pin
3	GND	GND pin
4	N.C.	Non Connection (Used to connect GND or OPEN state.)
5	EN	Enable pin
6	N.C.	Non Connection (Used to connect GND or OPEN state.)
7	N.C.	Non Connection (Used to connect GND or OPEN state.)
8	V_{CC}	Input pin
Reverse	FIN	Substrate(Connect to GND)

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●**Absolute Maximum Ratings** (Ta=25℃)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	10.0 *1	V
EN voltage		V_{EN}	10.0	V
Power dissipation	HTSOP-J8	Pd*2	2110 *2	mW
Operating Temperature Range		Topr	-40 to +105	℃
Storage Temperature Range		Tstg	-55 to +150	℃
Junction Temperature		Tjmax	+150	℃

*1 Not to exceed Pd

*2 Reduced by 16.9mW/℃ for each increase in Ta of 1℃ over 25℃. (when mounted on a board 70mm×70mm×1.6mm glass-epoxy board, two layer)

●**Recommended Operating Ratings** (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Input power supply voltage	V_{CC}	4.5	8.0	V
EN voltage	V_{EN}	0.0	8.0	V
Output voltage setting range	V_O	1.5	7.0	V
Output current	I_O	0.0	1.0	A

●**Electrical Characteristics** (Unless otherwise noted, EN=3V, Vcc=6V, R_1=43kΩ, R_2=8.2kΩ)

Parameter	Symbol	Temp	Min.	Typ.	Max.	Unit	Conditions
Circuit current at shutdown mode	I_{SD}	25℃	-	0	5	μA	V_{EN}=0V, OFF mode
		-40~105℃	-	-	5		
Bias current	I_{CC}	25℃	-	600	900	μA	
		-40~105℃	-	-	1200		
Line regulation	Reg.I	25℃	-	25	50	mV	V_{CC} =(Vo+0.9V)→8.0V
		-40~105℃	-	-	50		
Load regulation	Reg I_O	25℃	-	25	75	mV	I_O=0→1.0A
		-40~105℃	-	-	75		
Minimum dropout Voltage	V_{CO}	25℃	-	0.6	0.9	V	V_{CC}=5V, I_O=1.0A
		-40~105℃	-	-	1.2		
Output reference voltage (Variable type)	V_{FB}	25℃	0.792	0.800	0.808	V	I_O=0mA
		-40~105℃	0.776	-	0.824		
Output voltage(Fixed type)	V_O	25℃	V_O×0.99	V_O	V_O×1.01	V	I_O=0mA
		-40~105℃	Vo×0.97	Vo	Vo×1.03		
EN Low voltage	V_{EN}(Low)	25℃	0	-	0.8	V	
		-40~105℃	0	-	0.8		
EN High voltage	V_{EN}(High)	25℃	2.4	-	8.0	V	
		-40~105℃	2.4	-	8.0		
EN Bias current	I_{EN}	25℃	1	3	9	μA	
		-40~105℃	-	-	9		

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●Typical Performance Curves

(Unless otherwise noted, EN=3V, V_{CC}=6V, R_1=43kΩ, R_2=8.2kΩ)

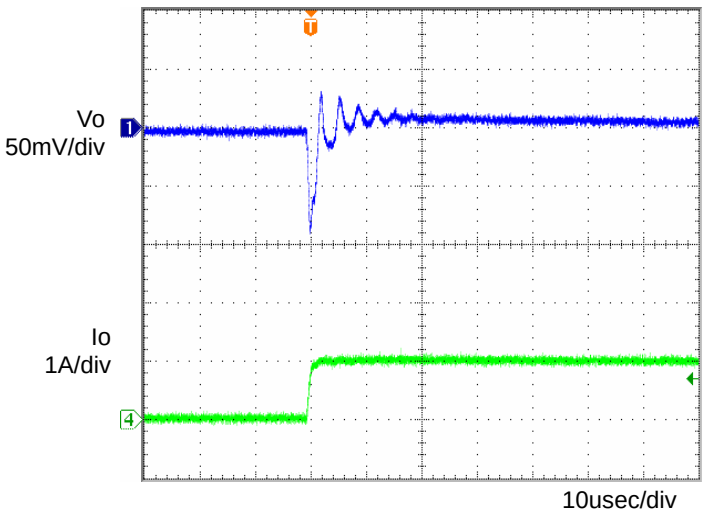

Fig.3
Transient Response
(0→1.0A)
Co=1μF,Ta=-40℃

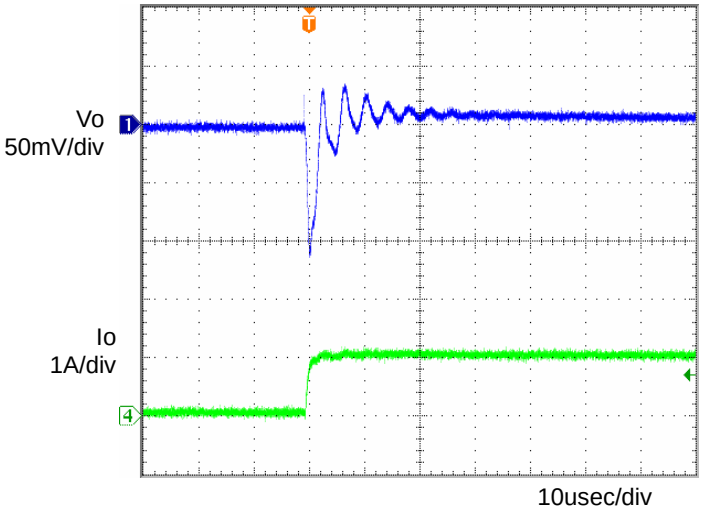

Fig.4
Transient Response
(0→1.0A)
Co=1μF,Ta=25℃

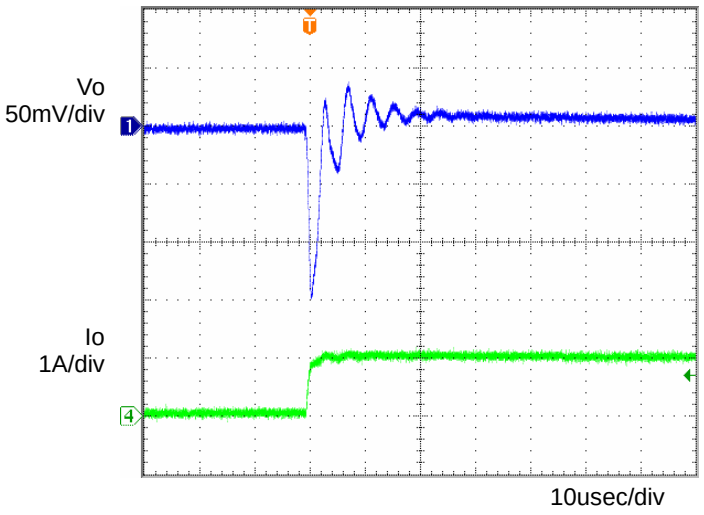

Fig.5
Transient Response
(0→1.0A)
Co=1μF,Ta=105℃

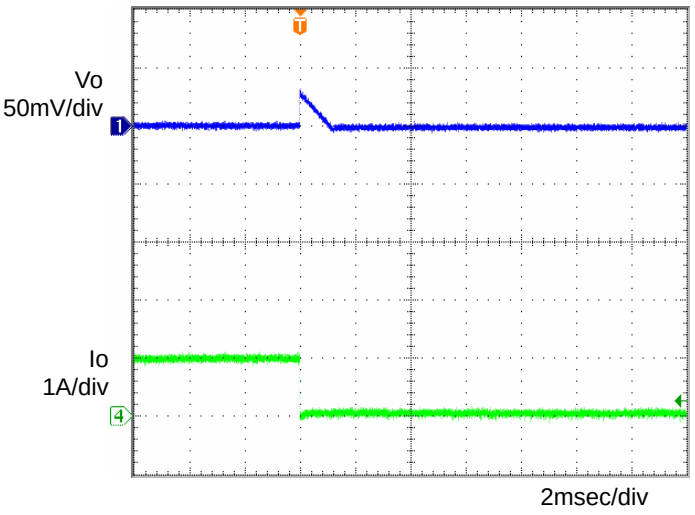

Fig.6
Transient Response
(1.0→0A)
Co=1μF,Ta=-40℃

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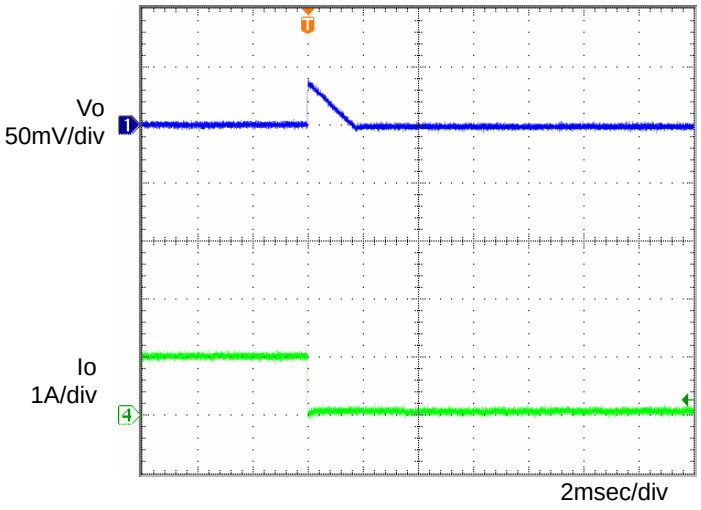

Fig.7
Transient Response
(1.0→0A)
Co=1μF,Ta=25℃

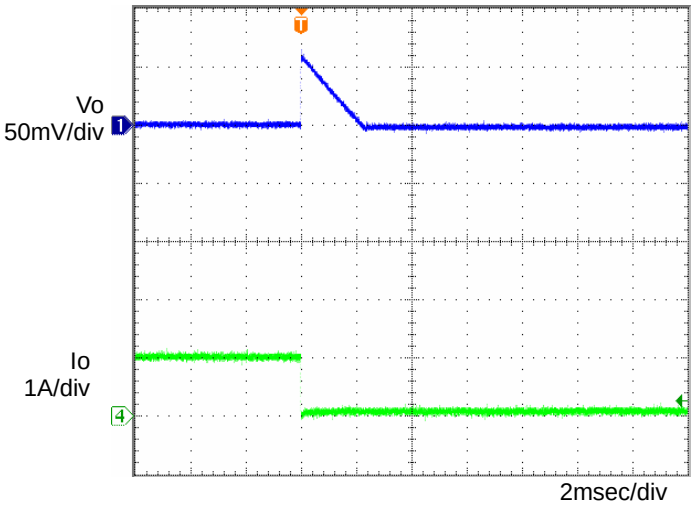

Fig.8
Transient Response
(1.0→0A)
Co=1μF,Ta=105℃

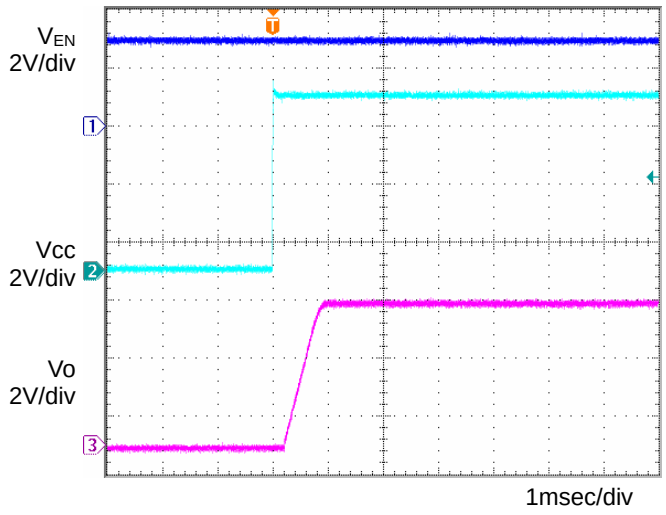

Fig.9
Input sequence 1
Co=1μF,Ta=-40℃

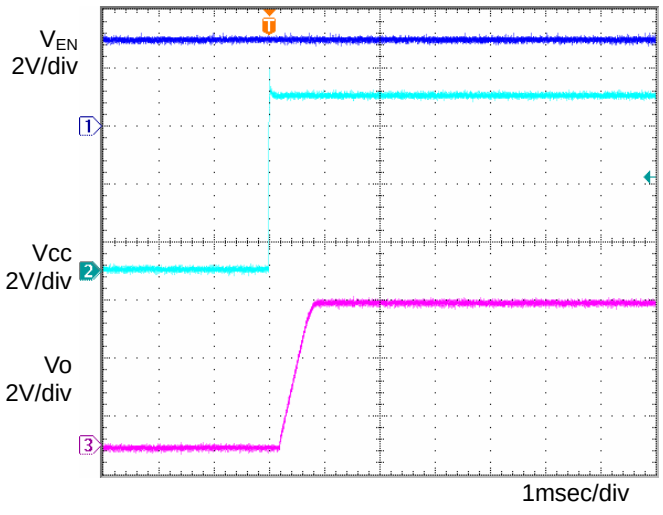

Fig.10
Input sequence 1
Co=1μF,Ta=25℃

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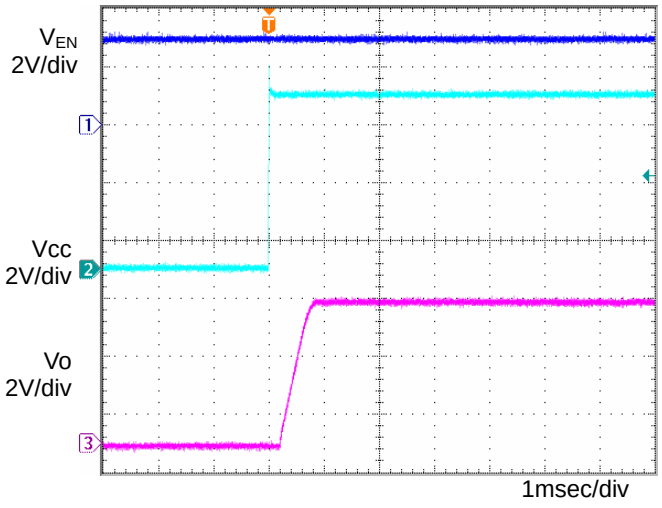

Fig.11
Input sequence 1
Co=1µF,Ta=105℃

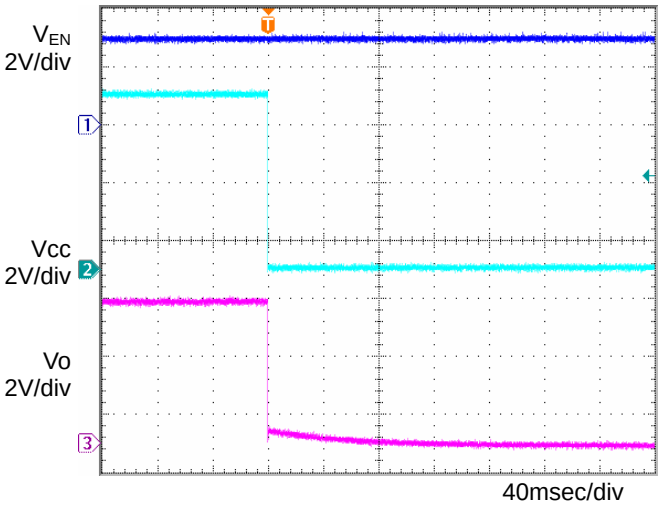

Fig.12
OFF sequence 1
Co=1µF,Ta=-40℃

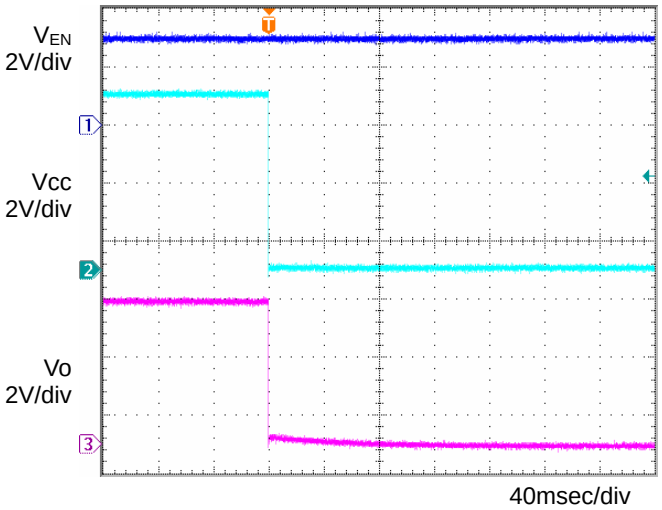

Fig.13
OFF sequence 1
Co=1µF,Ta=25℃

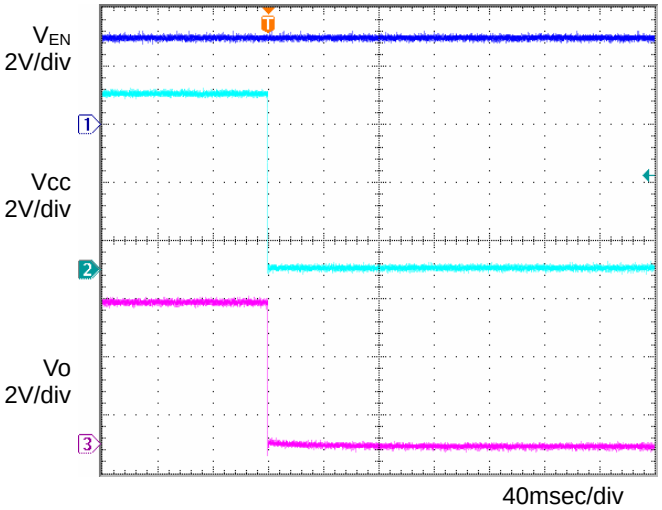

Fig.14
OFF sequence 1
Co=1µF,Ta=105℃

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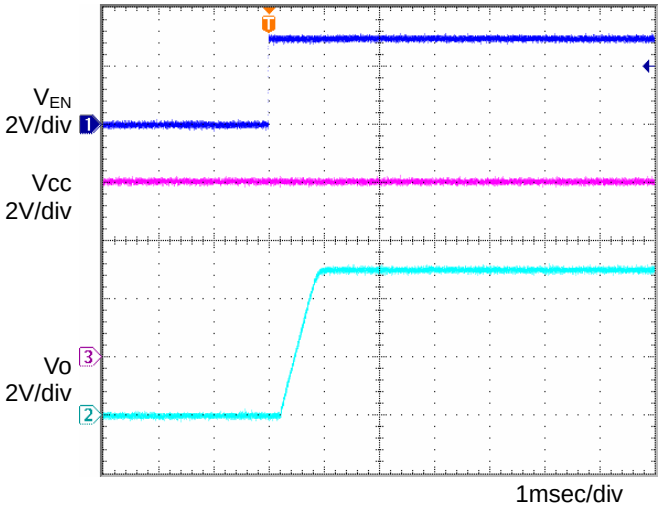

Fig.15
Input sequence 2
Co=1µF,Ta=-40℃

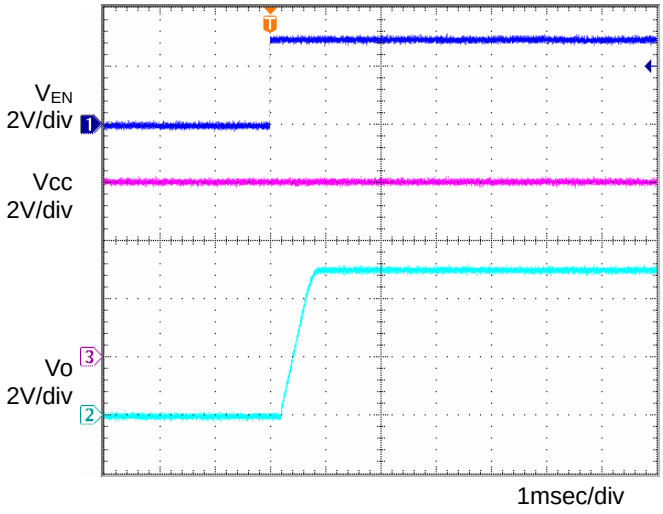

Fig.16
Input sequence 2
Co=1µF,Ta=25℃

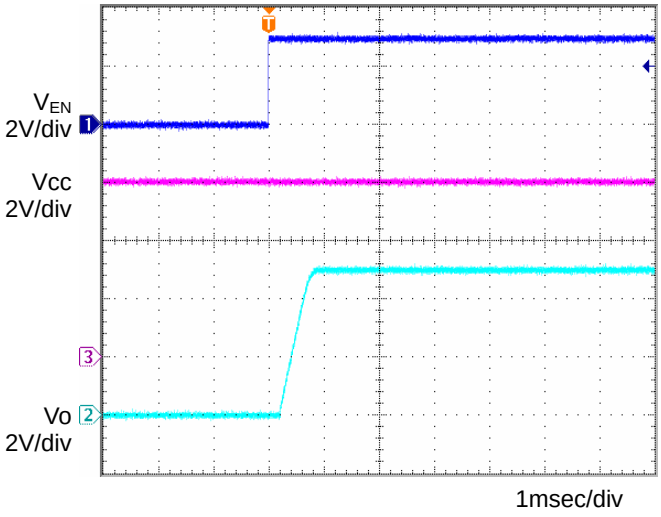

Fig.17
Input sequence 2
Co=1µF,Ta=105℃

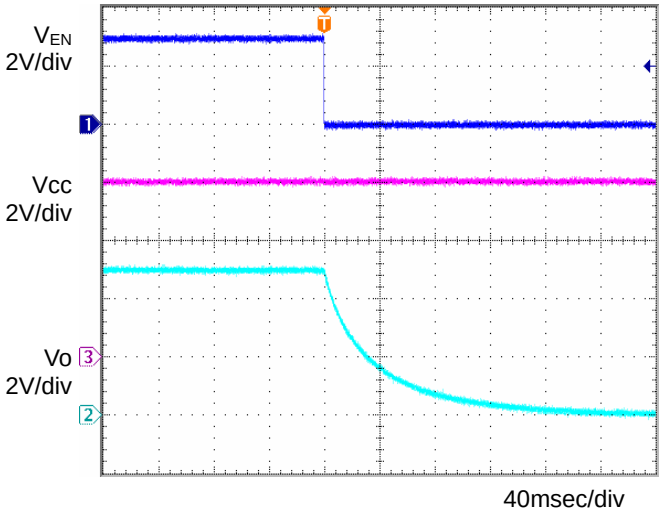

Fig.18
OFF sequence 2
Co=1µF,Ta=-40℃

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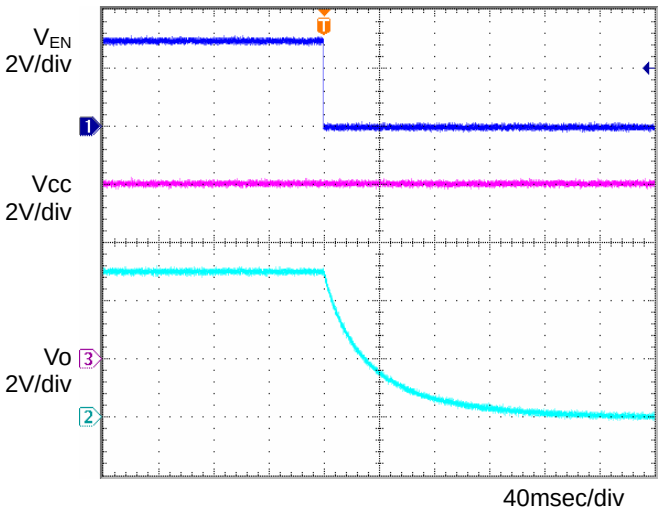

Fig.19
OFF sequence 2
Co=1μF,Ta=25℃

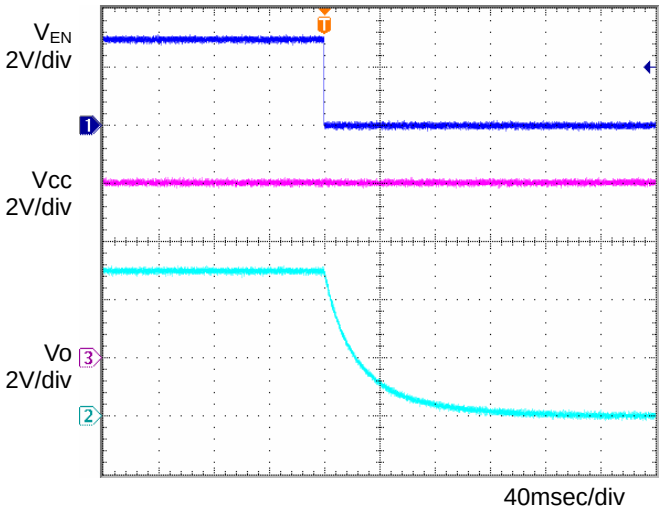

Fig.20
OFF sequence 2
Co=1μF,Ta=105℃

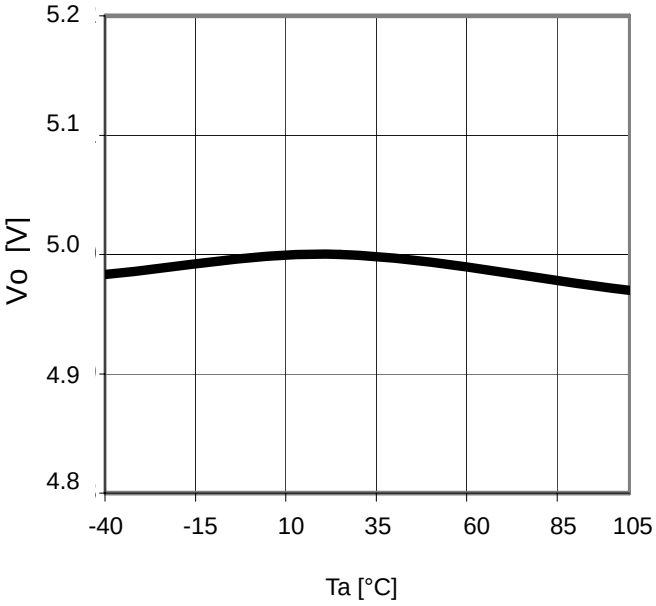

Fig.21
Ta-V_O (I_O=0mA)

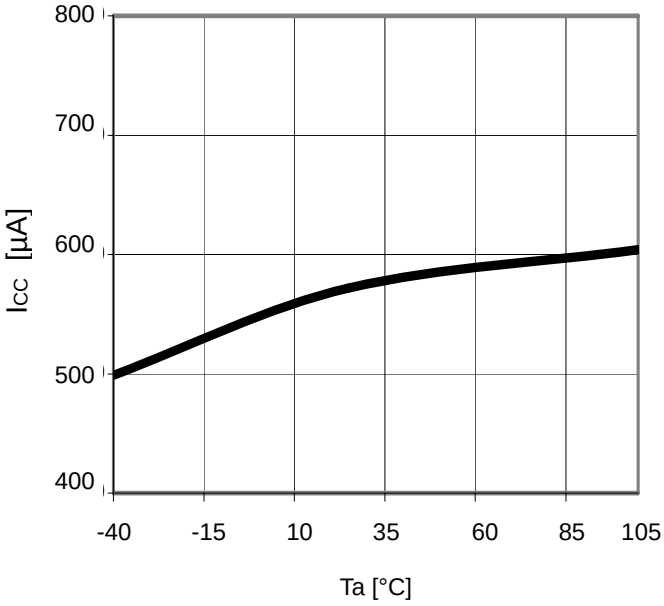

Fig.22
Ta-I_{CC}

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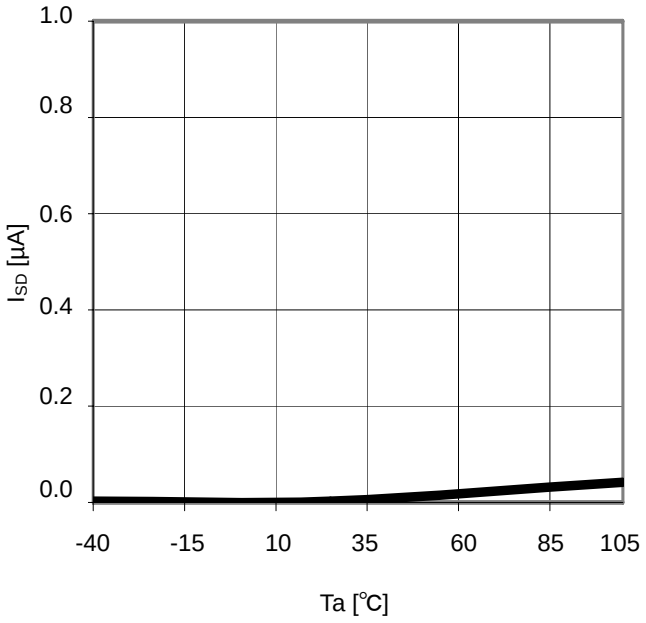

Fig.23
Ta-I_{SD}
(V_{EN}=0V)

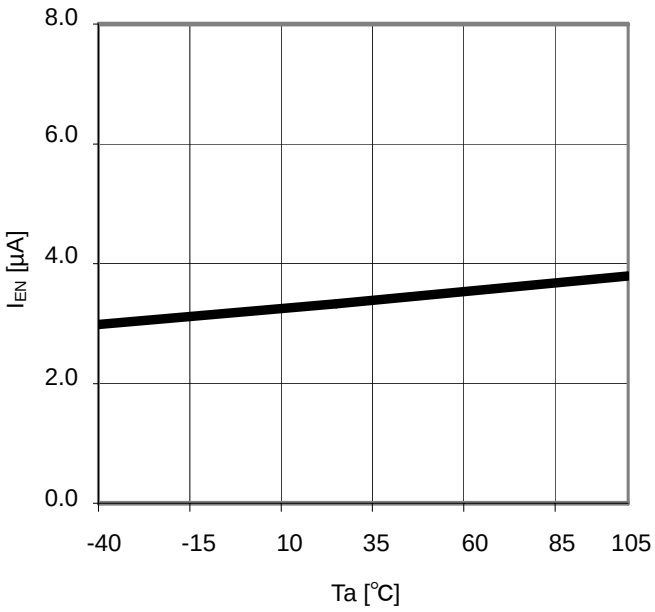

Fig.24
Ta-I_{EN}

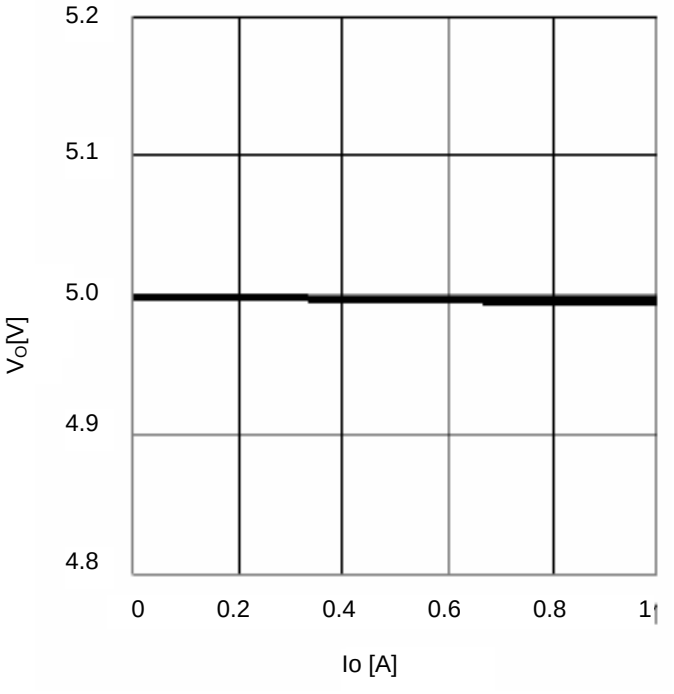

Fig.25
I_O-V_O

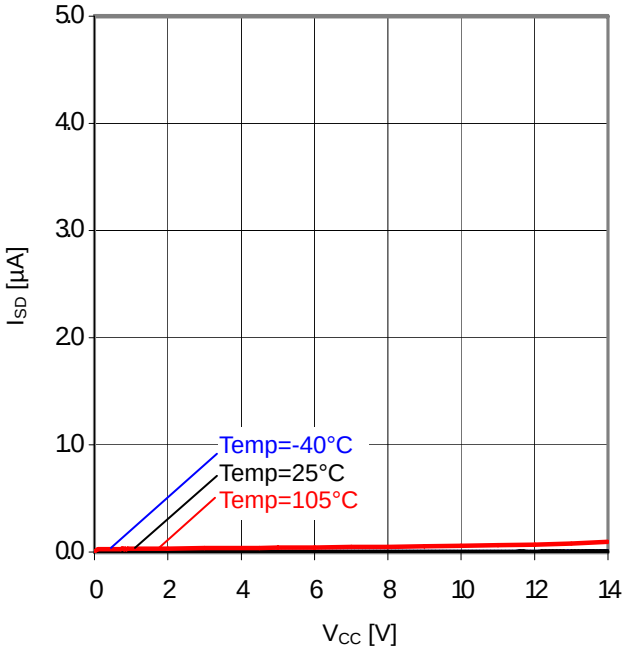

Fig.26
V_{CC}-I_{SD}
(V_{EN}=0V)

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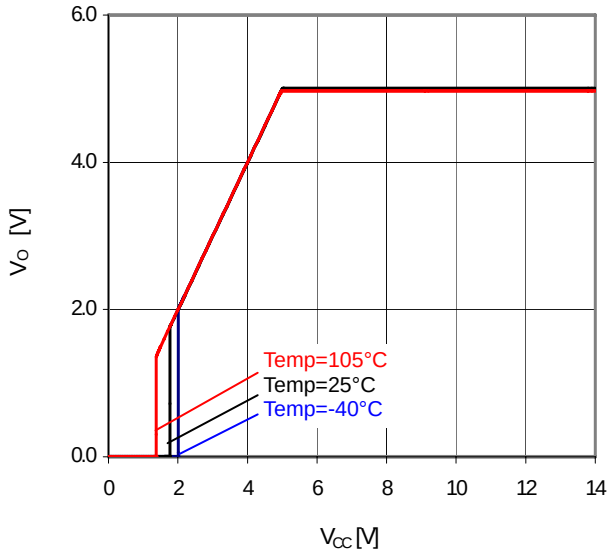

Fig.27
V_{CC}-V_O (I_O=0mA)

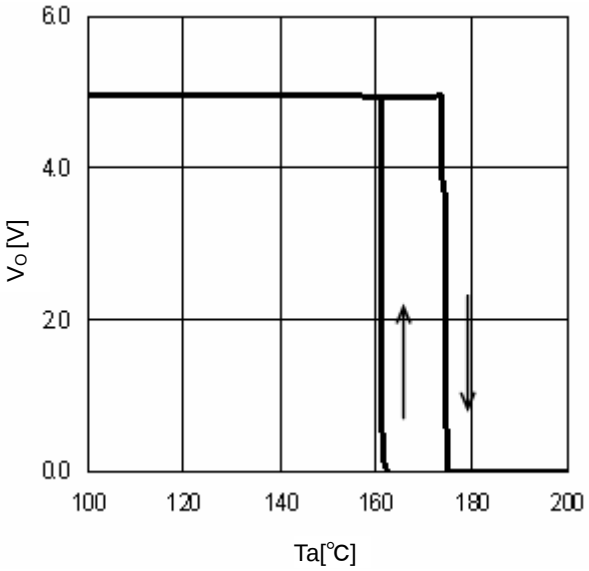

Fig.28
TSD (I_O=0mA)

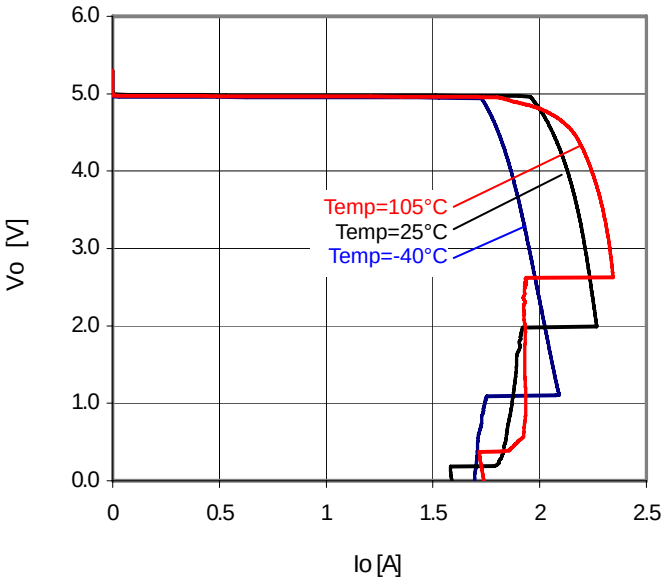

Fig.29
OCP

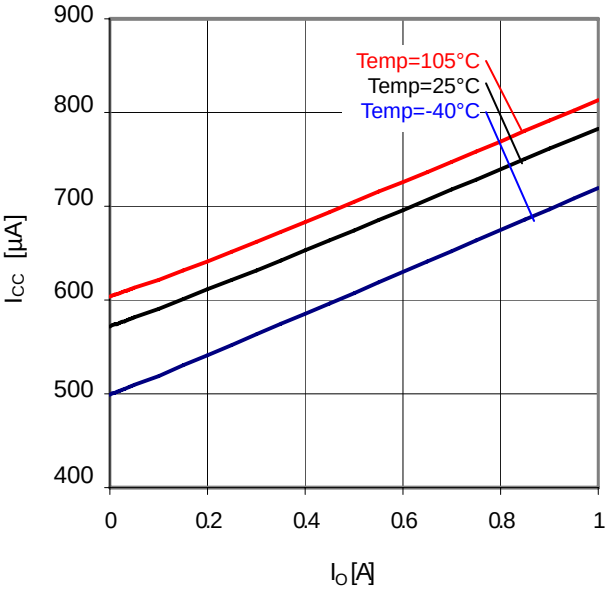

Fig.30
I_O-I_{CC}

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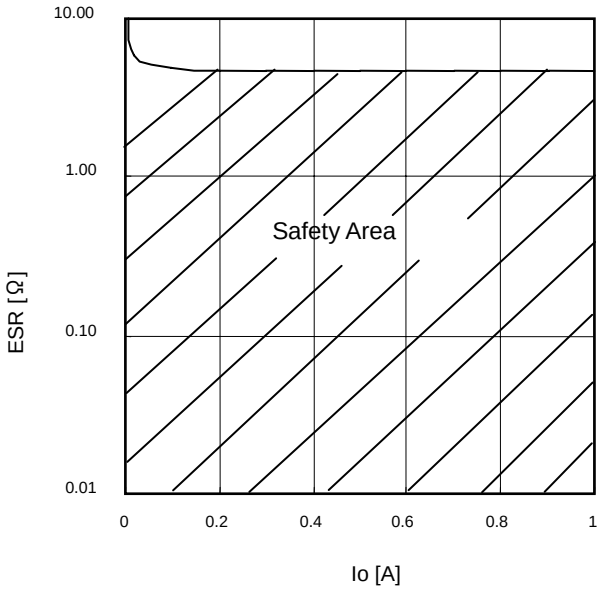

Fig.31
ESR Safety area

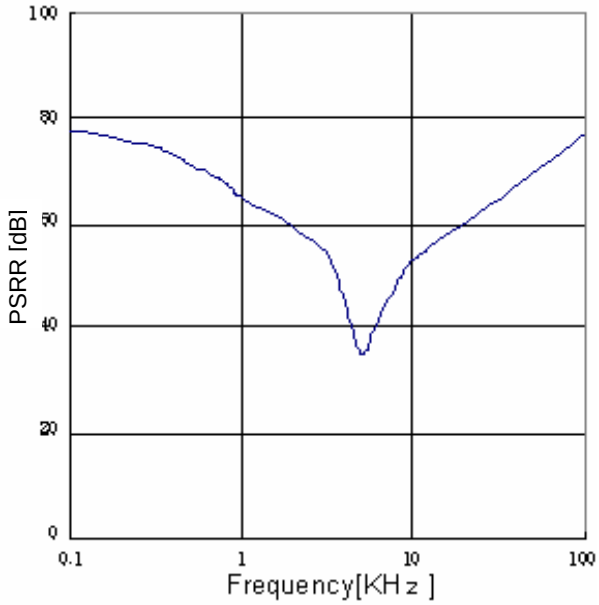

Fig.32
PSRR (I_O=0mA)

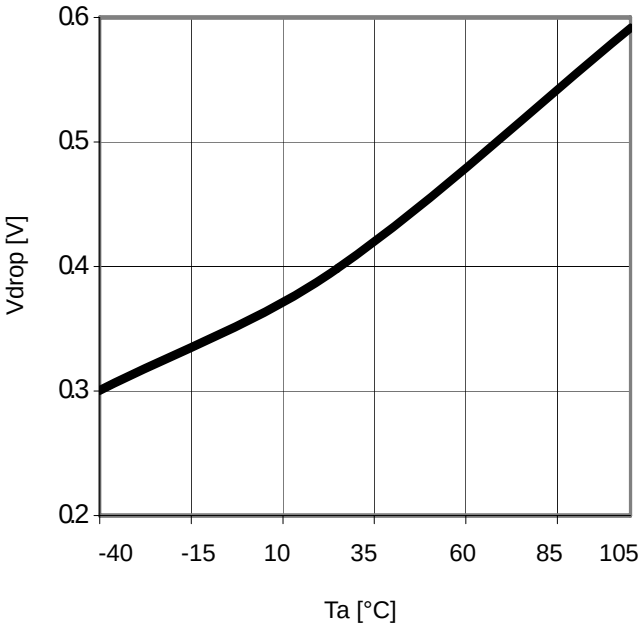

Fig.33
Ta-Vdrop
(V_{CC}=6V, I_O=1A)

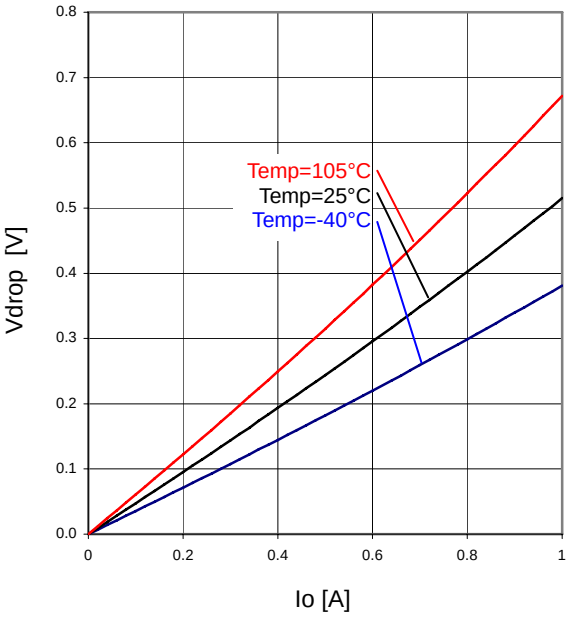

Fig.34
Minimum dropout Voltage 1
（V_{CC}=4.5V）

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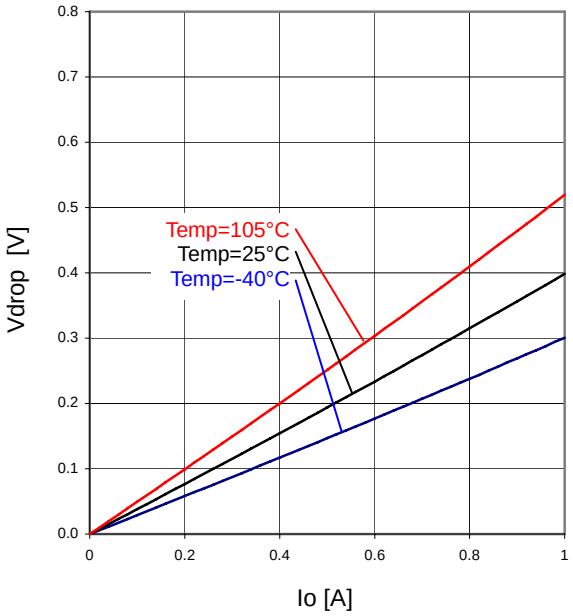

Fig.35
Minimum dropout Voltage 2
(V_{CC}=6.0V)

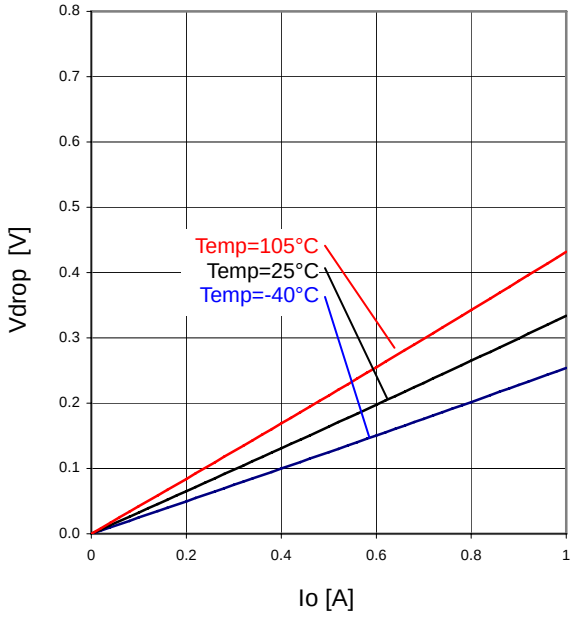

Fig.36
Minimum dropout Voltage 3
(V_{CC}=8.0V)

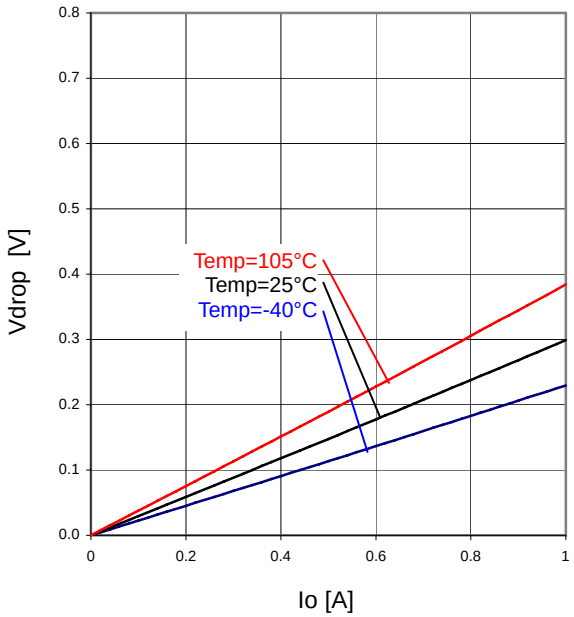

Fig.37
Minimum dropout Voltage 4
(V_{CC}=10.0V)

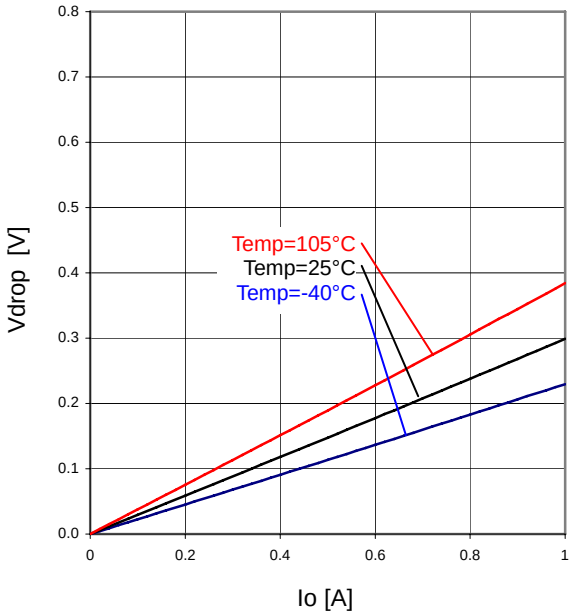

Fig.38
Minimum dropout Voltage 5
(V_{CC}=12.0V)

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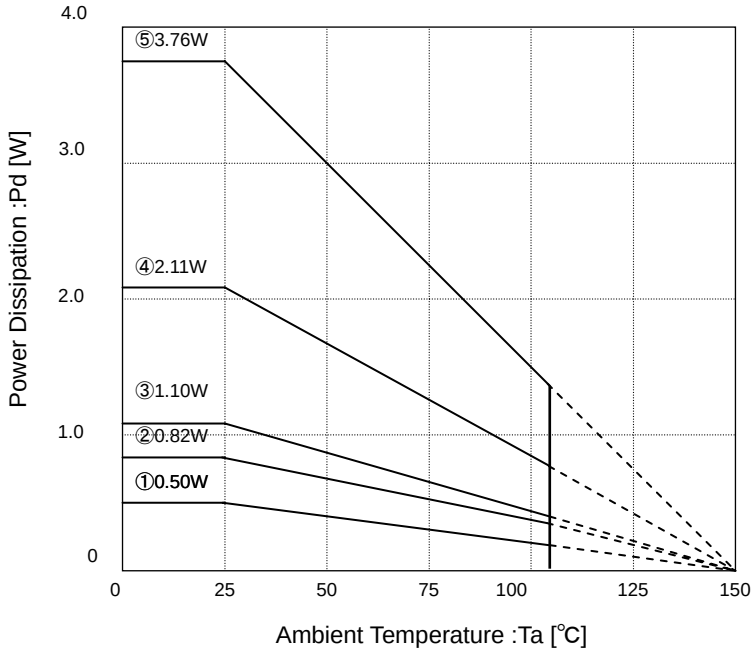
●Power Dissipation

◎HTSOP-J8



Measure condition: mounted on a ROHM board, and IC

Substrate size: 70mm × 70mm × 1.6mm
(Substrate with thermal via)
・ Solder the substrate and package reverse exposure heat radiation part

① IC only
θj-a=249.5℃/W
② 1-layer（copper foil are :0mm×0mm）
θj-a=153.2℃/W
③ 2-layer（copper foil are :15mm×15mm）
θj-a=113.6℃/W
④ 2-layer（copper foil are :70mm×70mm）
θj-a=59.2℃/W
⑤ 4-layer（copper foil are :70mm×70mm）
θj-a=33.3℃/W

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 105℃.
2. Chip junction temperature (Tj) can be no higher than 150℃.

Chip junction temperature can be determined as follows:

Calculation based on ambient temperature (Ta)

$Tj = Ta + \theta j\text{-}a \times W$

＜Reference values＞

θj-a: HTSOP-J8	153.2℃/W	1-layer substrate (copper foil density 0mm×0mm)
	113.6℃/W	2-layer substrate (copper foil density 15mm×15mm)
	59.2℃/W	2-layer substrate (copper foil density 70mm×70mm)
	33.3℃/W	4-layer substrate (copper foil density 70mm×70mm)

Substrate size: 70mm×70mm×1.6mm (substrate with thermal via)

Most of the heat loss that occurs in the BDxxHC0MEFJ-M is generated from the output Pch FET. Power loss is determined by the total V_{CC}-V_O voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the V_{CC} and V_O in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BDxxHC0MEFJ-M make certain to factor conditions such as substrate size into the thermal design.

$$\text{Power consumption[W]} = \left\{ \text{Input voltage } (V_{CC}) - \text{Output voltage } (V_O) \right\} \times I_O(\text{Ave})$$

Example) Where V_{CC}=5.0V, V_O=3.3V, I_O(Ave) = 0.1A,

$$\text{Power consumption[W]} = \left\{ 5.0\text{V} - 3.3\text{V} \right\} \times 0.1\text{A}$$

$$= 0.17\text{W}$$

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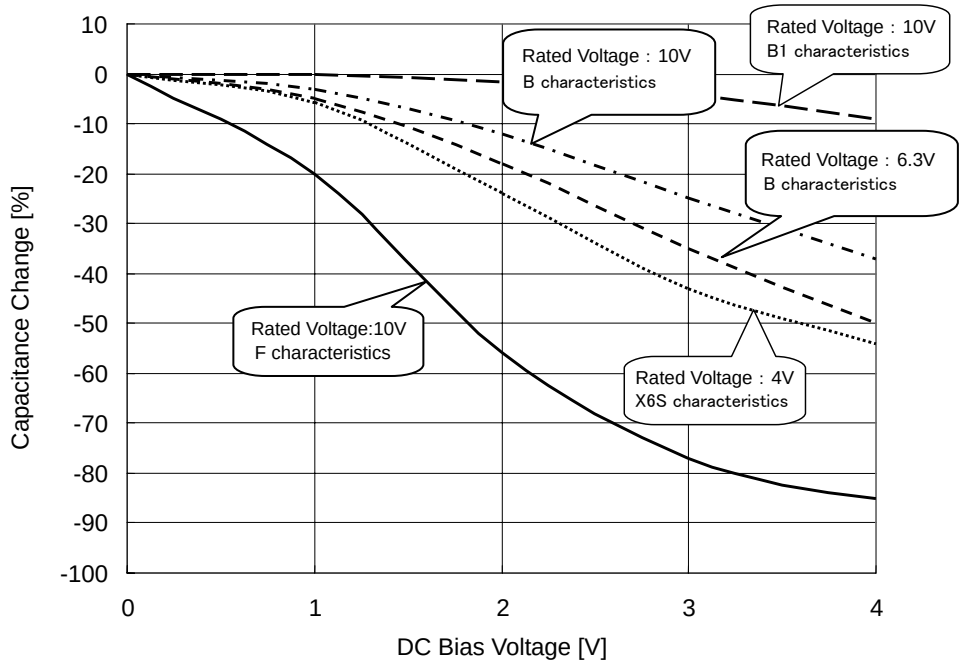
●Input-to-Output Capacitor

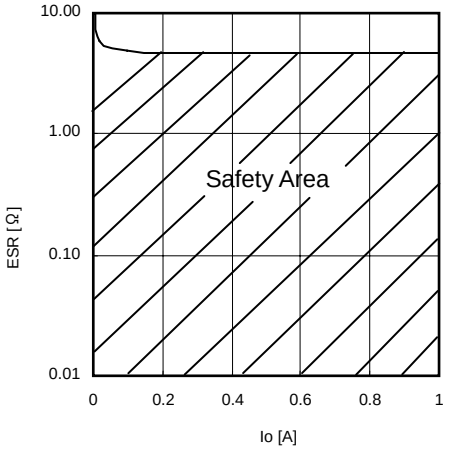
It is recommended that a capacitor is placed nearby pin between Input pin and GND, output pin and GND.
A capacitor, between input pin and GND, is valid when the power supply impedance is high or drawing is long. Also as for a capacitor, between output pin and GND, the greater the capacity, more sustainable the line regulation and it makes improvement of characteristics by load change. However, please check by mounted on a board for the actual application.
Ceramic capacitor usually has difference, thermal characteristics and series bias characteristics, and moreover capacity decreases gradually by using conditions.
For more detail, please be sure to inquire the manufacturer, and select the best ceramic capacitor.



Ceramic capacitor capacity – DC bias characteristics
(Characteristics example)

●Equivalent Series Resistance ESR (ceramic capacitor etc.)

Please attach an anti-oscillation capacitor between V_O and GND. Capacitor usually has ESR(Equivalent Series Resistance), and operates stable in ESR-I_O range, showed right. Generally, ESR of ceramic, tantalum and electronic capacitor etc. is different for each, so please be sure to check a capacitor which is going to use, and use it inside the stable operating region, showed right. Then, please evaluate for the actual application.



ESR – I_O characteristics

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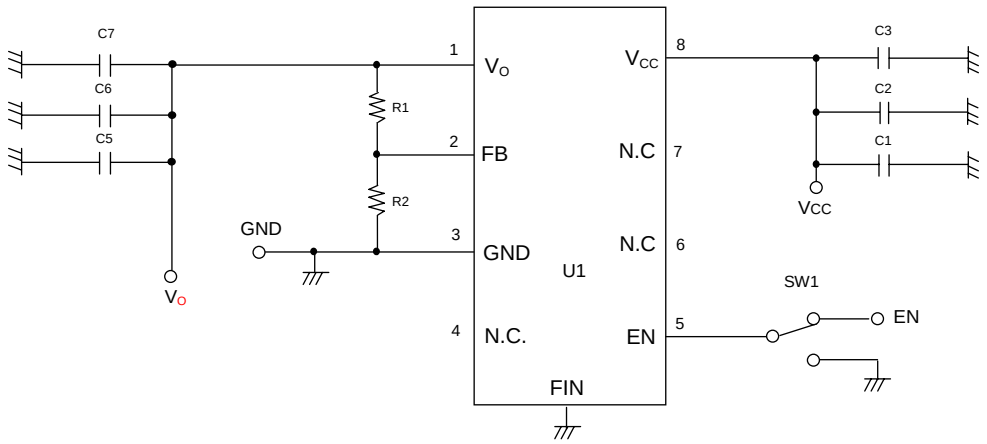
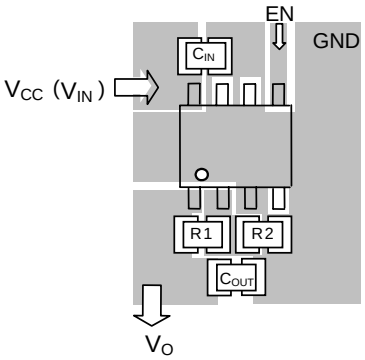
●Evaluation Board Circuit



●Evaluation Board Parts List

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1	43kΩ	MCR01PZPZF4302	ROHM	C4	-	-	-
R2	8.2kΩ	MCR01PZPZF8201	ROHM	C5	1μF	CM105X7R105K16AB	KYOCERA
R3	-	-	-	C6			
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	1μF	CM105B105K16A	KYOCERA	C10	-	-	-
C2	-	-		U1	-	BD00HC0MEFJ-M	ROHM
C3	-	-		U2	-	-	-

●Board Layout



・Input capacitor C_{IN} of V_{CC} (V_{IN}) should be placed very close to V_{CC}(V_{IN}) pin as possible, and used broad wiring pattern. Output capacitor C_{OUT} also should be placed close to IC pin as possible. In case connected to inner layer GND plane, please use several through hole.

・FB pin has comparatively high impedance, and is apt to be effected by noise, so floating capacity should be minimum as possible. Please be careful in wiring drawing

・Please take GND pattern space widely, and design layout to be able to increase radiation efficiency.

・For output voltage setting

Output voltage can be set by FB pin voltage（0.800V typ.）and external resistance R1, R2.

$$V_O = V_{FB} \times \frac{R1+R2}{R2}$$

（The use of resistors with R1+R2=1k to 90kΩ is recommended）

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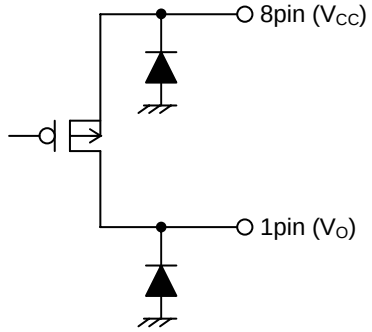
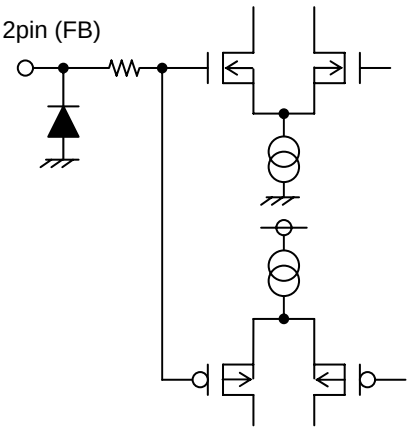
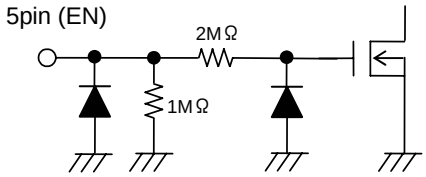
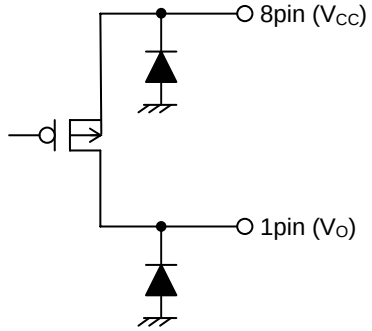
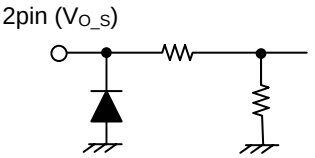
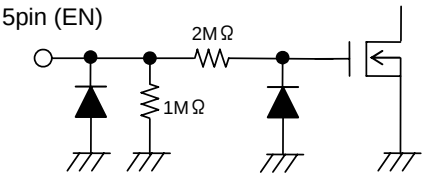
●I/O Equivalent Circuits (Output Voltage Vairable type)

8pin (V_{CC}) / 1pin (V_O)	2pin (FB)	5pin (EN)
		

●I/O Equivalent Circuits (Output Voltage Fixed type)

8pin (V_{CC}) / 1pin (V_O)	2pin (V_{O_S})	5pin (EN)
		

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●Operational Notes

(1). Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2). Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3). Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4). GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

(5). Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6). Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

(7). Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8). ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(9). Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD ON Temperature[℃] (typ.)	Hysteresis Temperature [℃] (typ.)
BDxxHC0MEFJ-M	175	15

(10). Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

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(11). Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated.

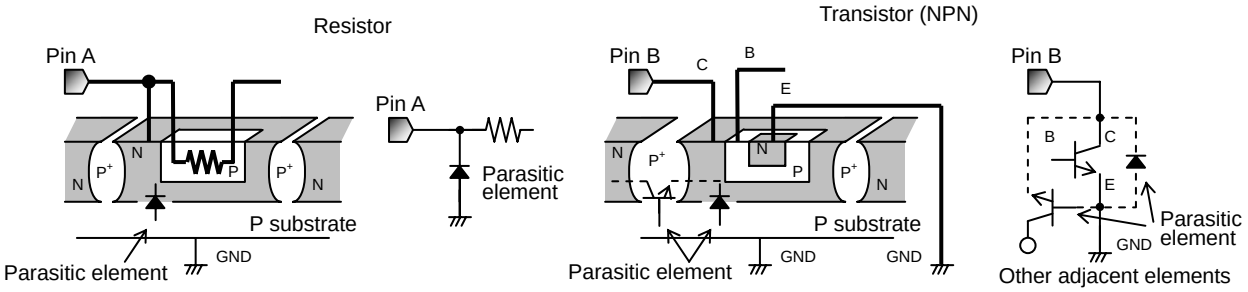
P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC.

The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate) voltage to an input pin, should not be used.



(12). Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

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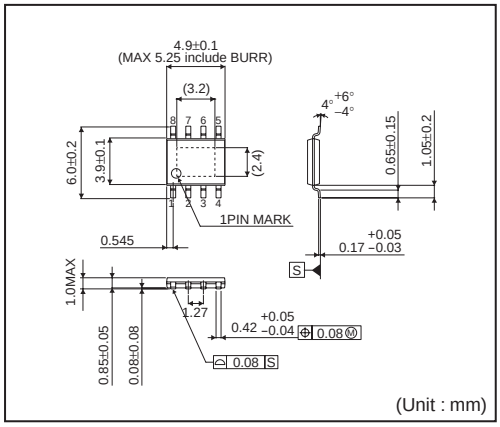
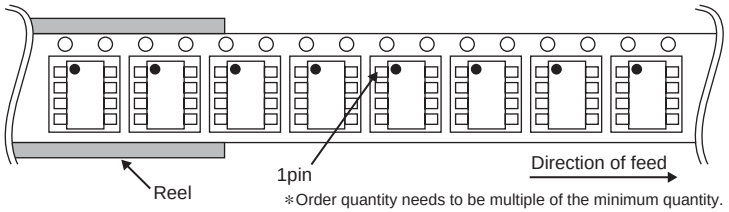
●Physical Dimension Tape and Reel Information

HTSOP-J8



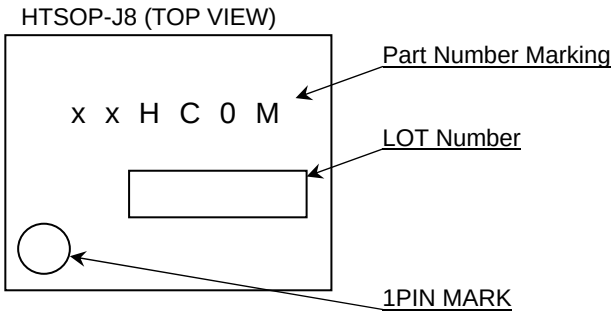
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram



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●**Revision History**

Date	Revision	Changes
31.Aug.2012	001	New Release

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Notice

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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