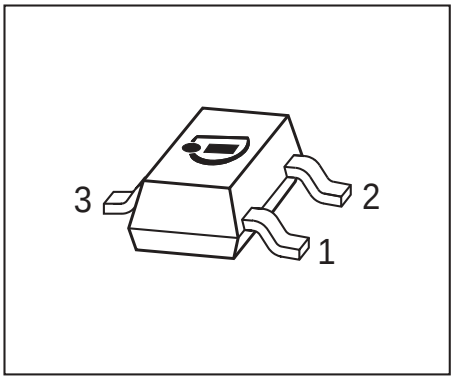
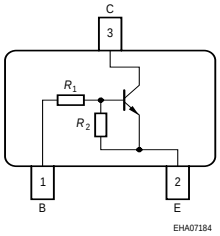
NPN Silicon Digital Transistor



- Built in bias resistor (R_1= 2.2 kΩ, R_2= 10 kΩ)
- Pb-free (RoHS compliant) package[1)]
- Qualified according AEC Q101



Type	Marking	Pin Configuration			Package
BCR505	XWs	1=B	2=E	3=C	SOT23

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	20	
Input reverse voltage	$V_{i(rev)}$	5	
Collector current	I_C	500	mA
Total power dissipation- $T_S \leq 79$ °C	P_{tot}	330	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[2)]	R_{thJS}	≤ 215	K/W

[1]Pb-containing package may be available upon special request
[2]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

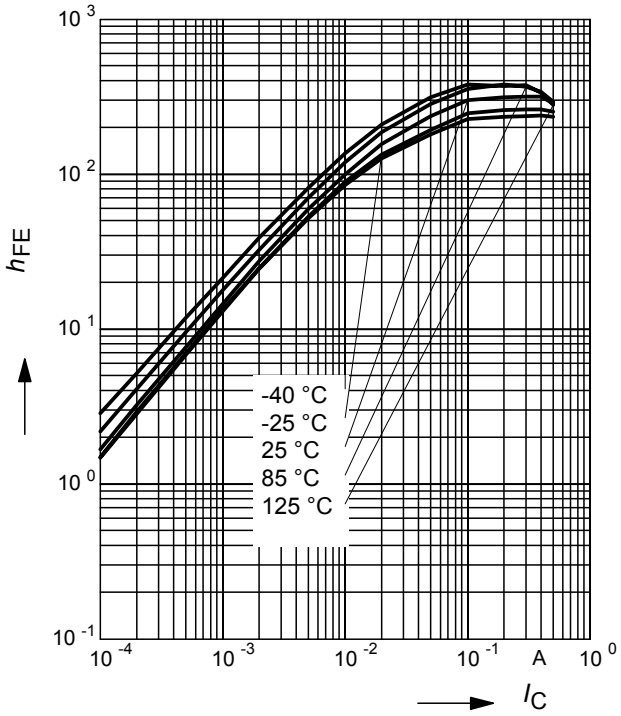
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage I_C = 100 µA, I_B = 0	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current V_{CB} = 50 V, I_E = 0	I_{CBO}	-	-	100	nA
Emitter-base cutoff current V_{EB} = 5 V, I_C = 0	I_{EBO}	-	-	0.65	mA
DC current gain- I_C = 50 mA, V_{CE} = 5 V	h_{FE}	70	-	-	-
Collector-emitter saturation voltage[1)] I_C = 50 mA, I_B = 2.5 mA	V_{CEsat}	-	-	0.3	V
Input off voltage I_C = 100 µA, V_{CE} = 5 V	$V_{i(off)}$	0.4	-	1	
Input on voltage I_C = 10 mA, V_{CE} = 0.3 V	$V_{i(on)}$	0.5	-	1.4	
Input resistor	R_1	1.5	2.2	2.9	kΩ
Resistor ratio	R_1/R_2	0.19	0.22	0.24	-
AC Characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 100 MHz	f_T	-	100	-	MHz

[1]Pulse test: t < 300µs; D < 2%

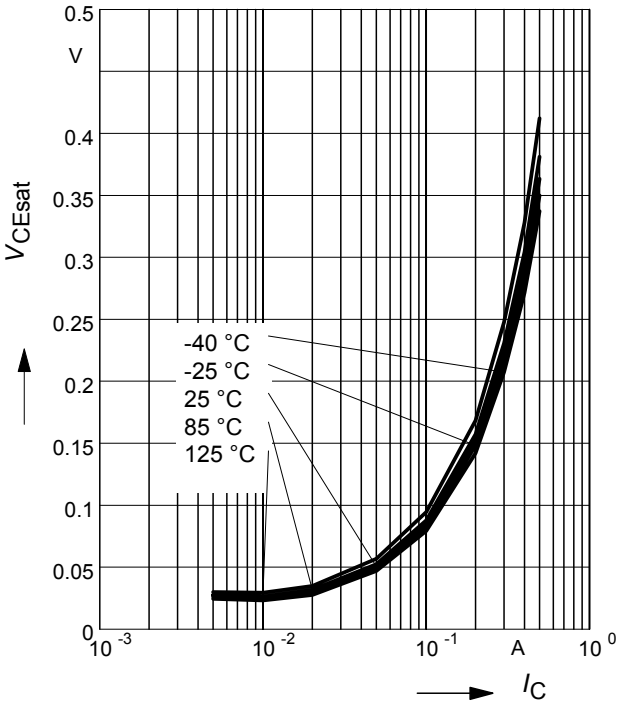
DC current gain h_{FE} = $f(I_C)$

V_{CE} = 5 V (common emitter configuration)



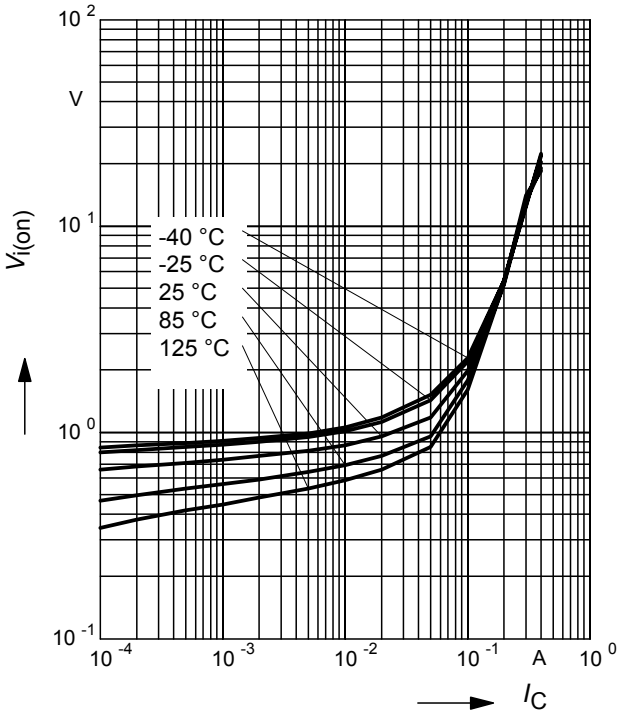
Collector-emitter saturation voltage

V_{CEsat} = $f(I_C)$, I_C/I_B = 20



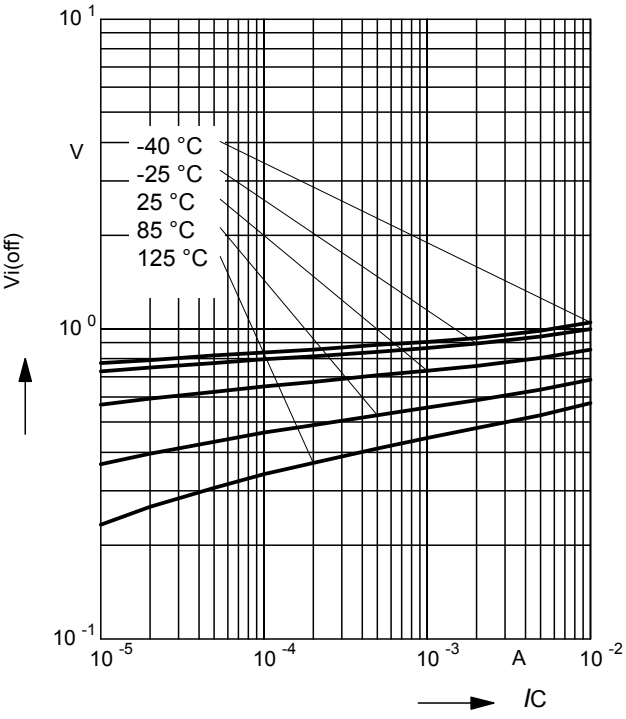
Input on Voltage $V_{i(on)}$ = $f(I_C)$

V_{CE} = 0.3V (common emitter configuration)

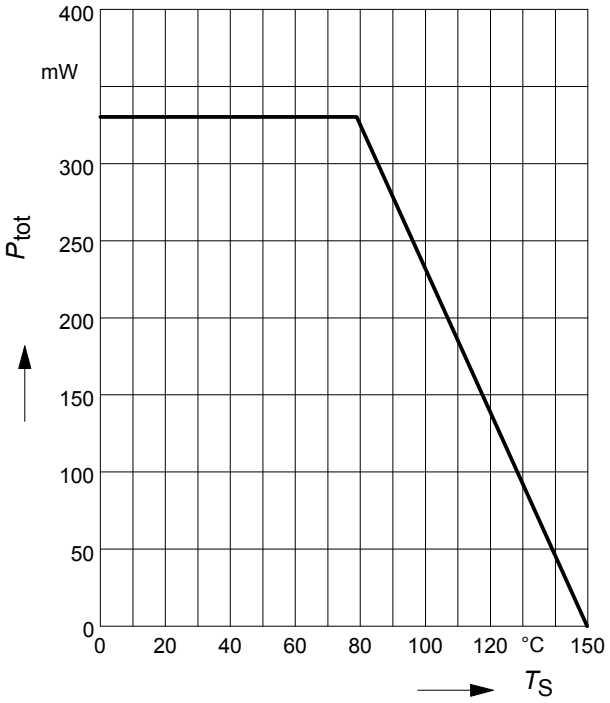


Input off voltage $V_{i(off)}$ = $f(I_C)$

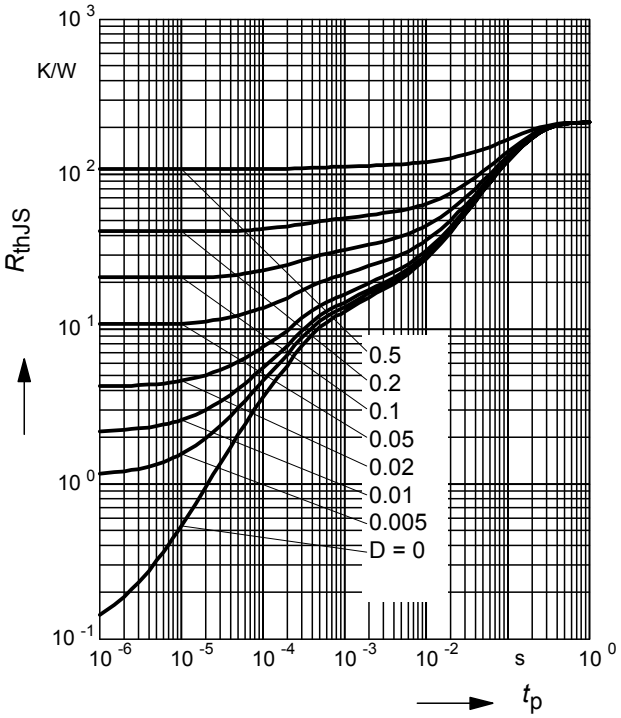
V_{CE} = 5V (common emitter configuration)



Total power dissipation $P_{tot} = f(T_S)$

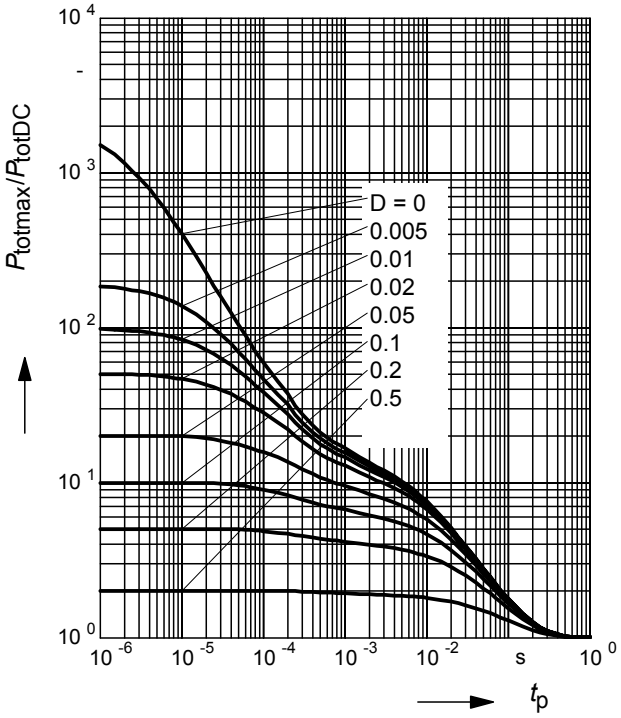


Permissible Pulse Load $R_{thJS} = f(t_p)$

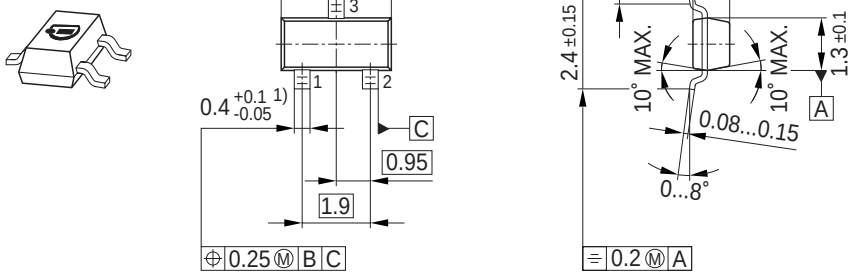


Permissible Pulse Load

$P_{totmax}/P_{totDC} = f(t_p)$

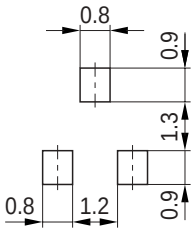


Package Outline

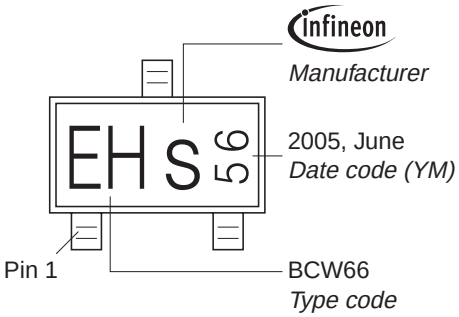


1) Lead width can be 0.6 max. in dambar area

Foot Print

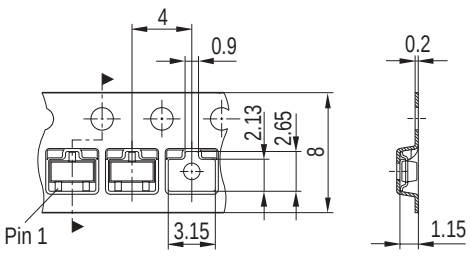


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



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