Features

- ESD Protect for 1 Line with Unidirectional.
- Provide ESD protection for a line to
  IEC 61000-4-2 (ESD) ±30kV (air), ±25kV (contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 5.5A (8/20μs)
- Suitable for, **7V and below,** operating voltage applications
- Ultra Small package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Cellular Handsets and Accessories
- Small Panel Modules
- PDA's
- Portable Devices
- Digital Cameras
- Touch Panels
- Notebooks and Handhelds
- MP3 Players
- Peripherals

Description

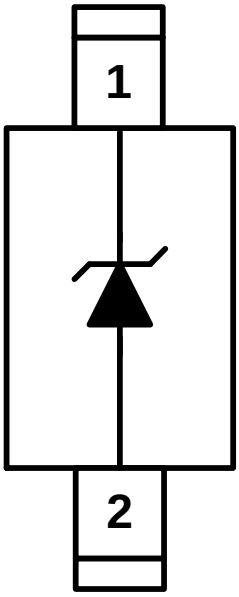
AZ4007-01L is a design which includes a unidirectional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ4007-01L has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4007-01L is a unique design which includes proprietary clamping cell in a single package.

During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4007-01L may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



SOD-323 (Top View)

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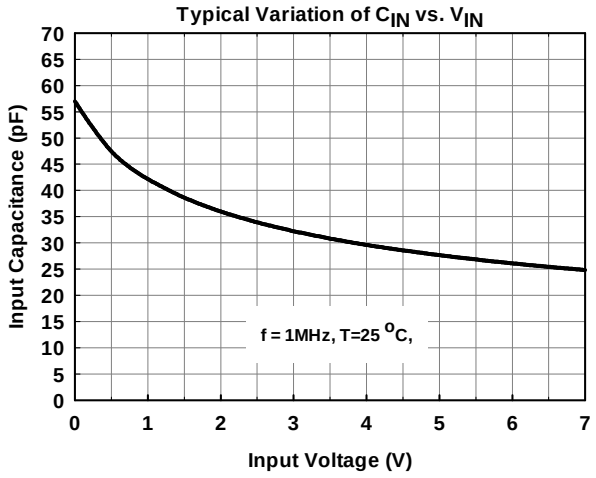
SPECIFICATIONS

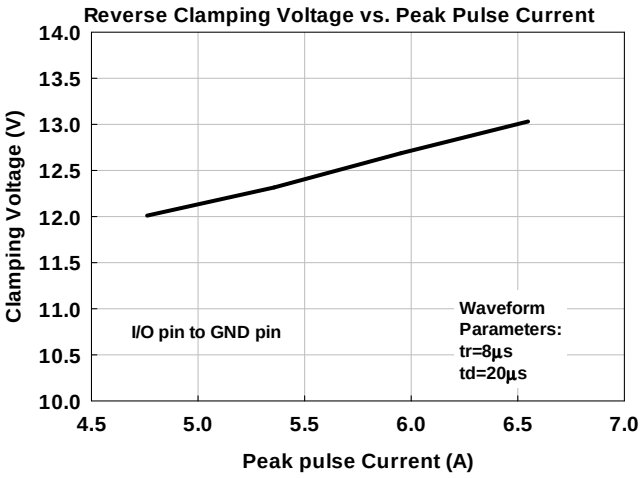
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us)	I_{PP}	5.5	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	8	V
pin-1 to pin-2 ESD per IEC 61000-4-2 (Air) pin-1 to pin-2 ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±25	kV kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	^{o}C
Operating Temperature	T_{OP}	-55 to +125	^{o}C
Storage Temperature	T_{STO}	-55 to +150	^{o}C

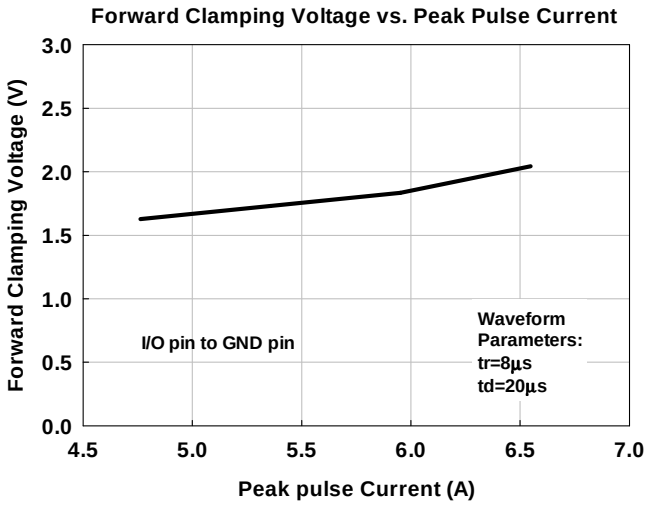
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	pin-1 to pin-2, T=25 ^{o}C.			7	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 7V, T=25 ^{o}C, pin-1 to pin-2.			1	µA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 ^{o}C, pin-1 to pin-2	8.5		12	V
Forward Voltage	V_{F}	I_{F} = 15mA, T=25 ^{o}C, pin-2 to pin-1	0.6	0.85	1.1	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, tp=8/20us, T=25 ^{o}C, pin-1 to pin-2.		12		V
ESD Clamping Voltage	V_{clamp}	IEC 61000-4-2 +6kV, T=25 ^{o}C, Contact mode, pin-1 to pin-2.		12.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+6kV, T=25 ^{o}C, Contact mode, pin-1 to pin-2.		0.16		Ω
Channel Input Capacitance	C_{IN}	V_{R} = 0V, f = 1MHz, T=25 ^{o}C, pin-1 to pin-2.		60	70	pF

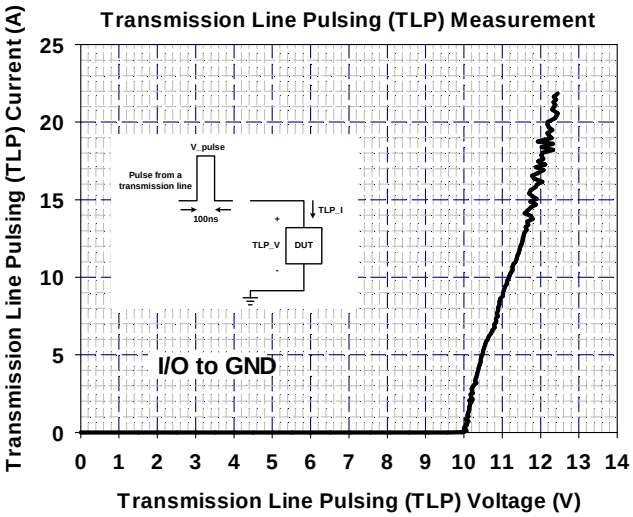
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Typical Characteristics









Applications Information

ESD Protection for Low-Speed Data Line

The AZ4007-01L is designed to protect one line against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ4007-01L is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ4007-01L should be kept as short as possible to minimize parasitic inductance in the board traces.

Fig. 2 shows another simplified example of using AZ4007-01L to protect the control lines, low speed data lines, and power lines of PCB internal circuits from ESD transient stress.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4007-01L.
- Place the AZ4007-01L near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to PCB internal circuit

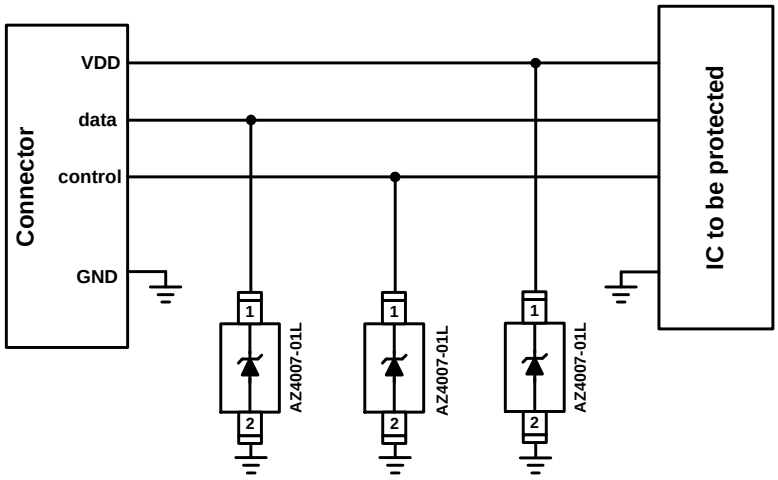


Fig. 1 ESD protection scheme by using AZ4007-01L.

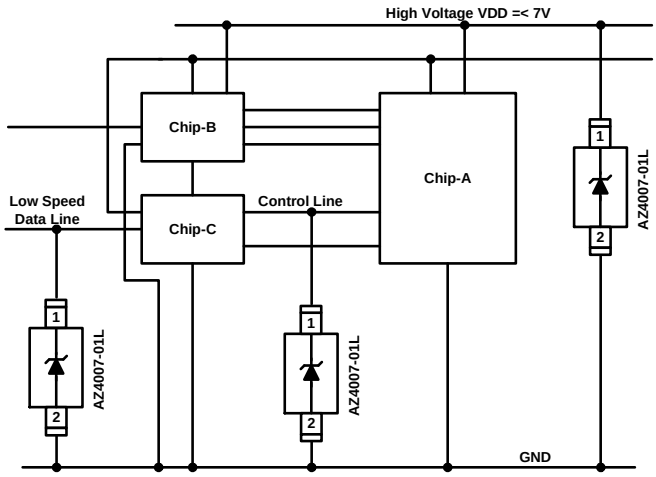


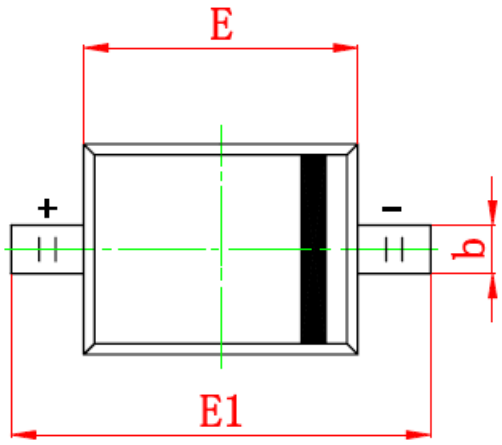
Fig. 2 ESD protection scheme for internal PCB circuits by using AZ4007-01L.

Mechanical Details

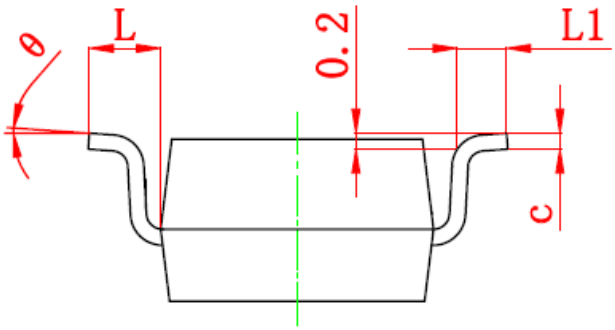
SOD-323

PACKAGE DIAGRAMS

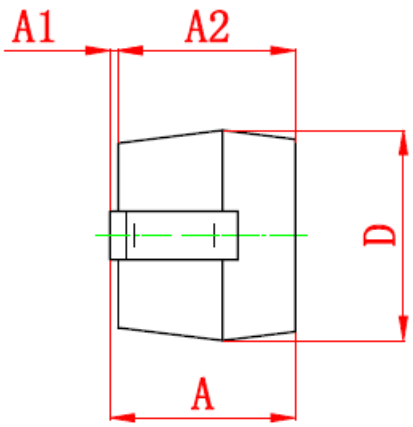
TOP VIEW



SIDE VIEW



END VIEW

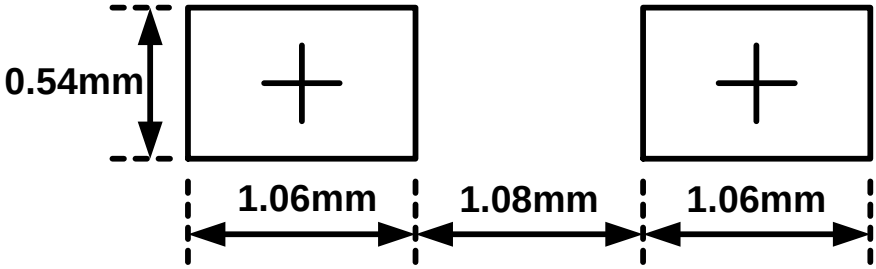


PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.8	1.0	0.031	0.039
A1	0	0.1	0.000	0.004
A2	0.8	0.9	0.031	0.035
b	0.25	0.35	0.010	0.014
C	0.08	0.15	0.003	0.006
D	1.2	1.4	0.047	0.055
E	1.6	1.8	0.063	0.071
E1	2.5	2.7	0.098	0.106
L	0.475REF		0.019 REF	
L1	0.25	0.4	0.010	0.016
θ	0^o	8^o	0^o	8^o

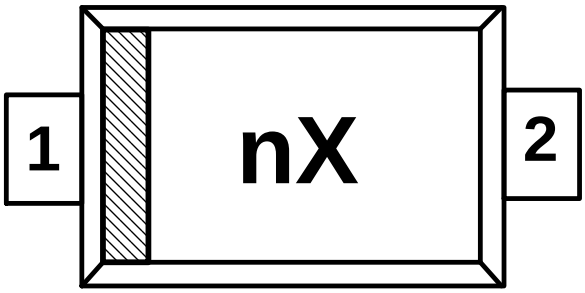
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LAND LAYOUT



Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



n = Device Code
X = Date Code

Part Number	Marking Code
AZ4007-01L	nX

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZ4007-01L.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2011/10/26	Formal Release.