ON Semiconductor®

DATASHEET

AX5031

Revision 2

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1. Overview

1.1. Features

- **Advanced multi-channel single chip UHF transmitter**
- **Configurable for usage in 400-470 MHz and 800-940 MHz ISM bands**
- **-5 dBm to +15 dBm programmable output**
- **13 mA @ 0 dBm, 868 MHz**
- **22 mA @ 10 dBm, 868 MHz**
- **44 mA @ 15 dBm, 868 MHz**
- **Wide variety of shaped modulations supported (ASK, PSK, OQPSK, MSK, FSK, GFSK, 4-FSK)**
- **Data rates from 1 to 350 kbps (FSK, MSK, GFSK, 4-FSK), 1 to 2000 kbps (ASK), 10 to 2000 kbps PSK**
- **Ultra fast settling RF frequency synthesizer for low-power consumption**
- **802.15.4 compatible**
- **RF carrier frequency and FSK deviation programmable in 1 Hz steps**
- **Fully integrated RF frequency synthesizer with VCO auto-ranging and band-width boost modes for fast locking**
- **Few external components**
- **On chip communication controller and flexible digital modulator**
- **Channel hopping 2000 hops/s**
- **Crystal oscillator with programmable transconductance and programmable internal tuning capacitors for low cost crystals**
- **SPI micro-controller interface**
- **QFN20 package**
- **Supply voltage range 2.2V - 3.6V**
- **Internal power-on-reset**
- **32 byte data FIFO**
- **Programmable Cyclic Redundancy Check (CRC-CCITT, CRC-16, CRC-32)**
- **Optional spectral shaping using a self synchronizing shift register**
- **Brown-out detection**
- **Differential antenna pins**
- **Dual frequency registers**
- **Internally generated coding for forward Viterbi error correction**
- **Software compatible to AX5051**

1.2. Applications

- Telemetry
- Sensor readout, thermostats
- AMR
- Toys
- Wireless audio
- Wireless networks
- Wireless M-Bus
- Access control
- Remote keyless entry
- Remote controls
- Active RFID
- Compatible with FCC Part 15.247, FCC Part 15.249, EN 300 220 wideband, Wireless M-Bus S/T –mode, Konnex RF, ARIB T-67

2. Block Diagram

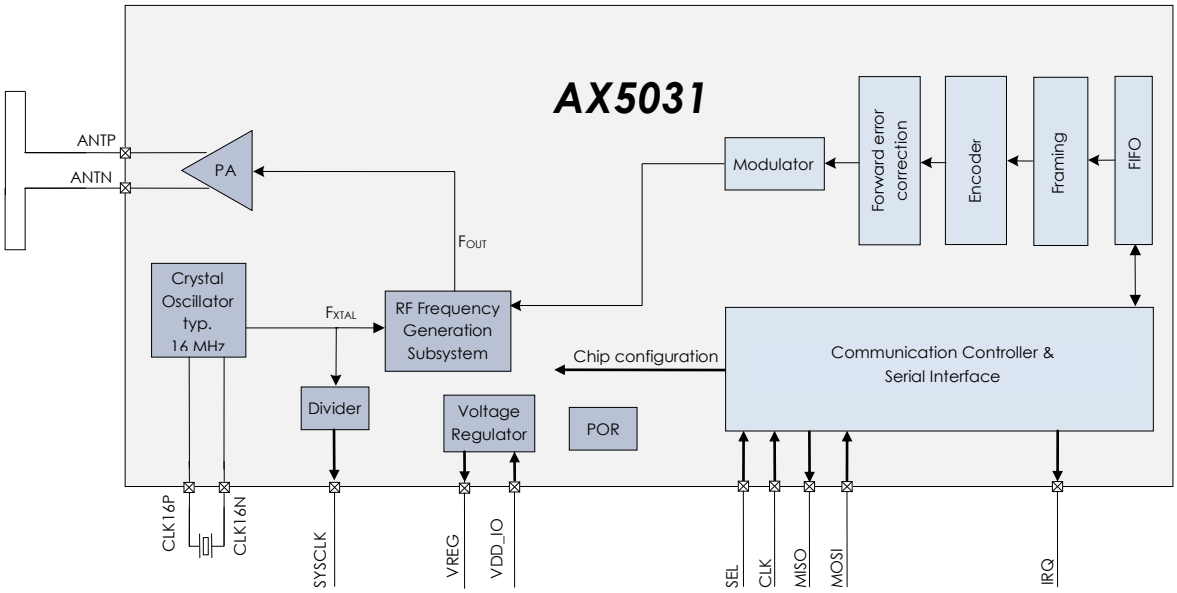


Figure 1 Functional block diagram of the AX5031

3. Pin Function Descriptions

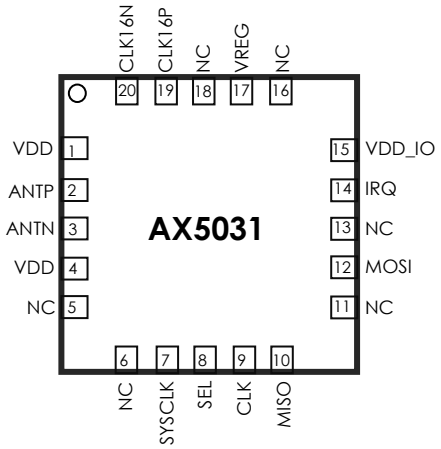
3.1. Pin List

Symbol	Pin(s)	Type	Description
VDD	1	P	Power supply, must be supplied with regulated voltage VREG
ANTP	2	A	Antenna output
ANTN	3	A	Antenna output
VDD	4	P	Power supply, must be supplied with regulated voltage VREG
NC	5	N	Not connected
NC	6	N	Not connected
SYSCLK	7	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin
SEL	8	I	Serial peripheral interface select
CLK	9	I	Serial peripheral interface clock
MISO	10	O	Serial peripheral interface data output
NC	11	N	Not connected
MOSI	12	I	Serial peripheral interface data input
NC	13	N	Not connected
IRQ	14	I/O	Default functionality: Interrupt Can be programmed to be used as a general purpose I/O pin
VDD_IO	15	P	Unregulated power supply
NC	16	N	Not connected
VREG	17	P	Regulated output voltage VDD pins must be connected to this supply voltage A 1µF low ESR capacitor to GND must be connected to this pin
NC	18	P	Not to be connected
CLK16P	19	A	Crystal oscillator input/output
CLK16N	20	A	Crystal oscillator input/output
GND	centre pad	P	Ground on center pad of QFN

A = analog signal
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible and 5V tolerant.

3.2. Pinout Drawing



GND connection is done via the exposed centre pad of the QFN package.

Figure 2: Pinout drawing (Top view)

4. Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
VDD_IO	Supply voltage		-0.5	5.5	V
IDD	Supply current			100	mA
P_{tot}	Total power consumption			800	mW
I_{I1}	DC current into any pin except ANTP, ANTN		-10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		-100	100	mA
I_O	Output current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		-0.5	5.5	V
	Input voltage digital pins		-0.5	5.5	V
V_{es}	Electrostatic handling	HBM	-2000	2000	V
T_{amb}	Operating temperature		-40	85	°C
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction Temperature			150	°C

4.2. DC Characteristics

Supplies

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
T_{AMB}	Operational ambient temperature		-40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage		2.2	3.0	3.6	V
VREG	Internally regulated supply voltage	Power-down mode PWRMODE=0x00		1.7		V
		All other power modes	2.1	2.5	2.8	V
I_{PDOWN}	Power-down current	PWRMODE=0x00		0.25		µA
I_{TX}	Current consumption TX for maximum power with default matching network at 3.3V VDD_IO, note 1	868 MHz, 15 dBm		44		mA
		433 MHz, 15 dBm		45		
TX_{VARVDD}	Variation of output power over voltage	VDD_IO > 2.5V, note 1		+/- 0.5		dB
$TX_{VARTEMP}$	Variation of output power over temperature	VDD_IO > 2.5V, note 1		+/- 0.5		dB

Notes:
1. The PA voltage is regulated to 2.5 V. For VDD_IO levels in the range of 2.2 V to 2.5 V the output power drops by typically 1 dBm.

Note on current consumption in TX mode

To achieve best output power the matching network has to be optimized for the desired output power and frequency. As a rule of thumb a good matching network produces about 50% efficiency with the **AX5031** power amplifier although over 90% are theoretically possible. A typical matching network has between 1 dB and 2 dB loss (P_{loss}).

The current consumption can be calculated as

$I_{TX}[mA]=1/PA_{efficiency}*10\text{^}((P_{out}[dBm]+P_{loss}[dB])/10)/2.5V+I_{offset}$

I_{offset} is about 12 mA for the VCO at 400-470 MHz and 11 mA for 800-940 MHz. The following table shows calculated current consumptions versus output power for P_{loss} = 1 dB, $PA_{efficiency}$ = 0.5 and I_{offset}= 11 mA at 868 MHz

Pout [dBm]	I [mA]
0	13.0
1	13.2
2	13.6
3	14.0
4	14.5
5	15.1
6	16.0
7	17.0
8	18.3
9	20.0
10	22.0
11	24.6
12	27.96
13	32.1
14	37.3
15	43.8

The **AX5031** power amplifier runs from the regulated VDD supply and not directly from the battery. This has the advantage that the current and output power do not vary much over supply voltage and temperature from 2.55 V to 3.6 V supply voltage. Between 2.55 V and 2.2 V a drop of about 1 dB in output power occurs.

Logic

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
DIGITAL INPUTS						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		-10		10	µA
DIGITAL OUTPUTS						
I_{OH}	Output Current, high	V_{OH}= 2.4V	4			mA
I_{OL}	Output Current, low	V_{OL}= 0.4V	4			mA
I_{OZ}	Tri-state output leakage current		-10		10	µA

4.3. AC Characteristics

Crystal Oscillator

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{XTAL}	Crystal frequency	Note 1, 3	15.5	16	25	MHz
gm_{osc}	Transconductance oscillator	XTALOSCGM=0000		1		mS
		XTALOSCGM=0001		2		
		XTALOSCGM =0010 default		3		
		XTALOSCGM =0011		4		
		XTALOSCGM =0100		5		
		XTALOSCGM =0101		6		
		XTALOSCGM =0110		6.5		
		XTALOSCGM =0111		7		
		XTALOSCGM =1000		7.5		
		XTALOSCGM =1001		8		
		XTALOSCGM =1010		8.5		
		XTALOSCGM =1011		9		
		XTALOSCGM =1100		9.5		
		XTALOSCGM =1101		10		
		XTALOSCGM =1110		10.5		
		XTALOSCGM =1111		11		
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	XTALCAP = 000000 default		2		pF
		XTALCAP = 111111		33		pF
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of XTALCAP			0.5		pF
A_{osc}	Oscillator amplitude at pin CLK16P	Note 2			0.5	V
RIN_{osc}	Input DC impedance		10			kΩ

Notes

1. Tolerances and start-up times depend on the crystal used.
2. If an external clock is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and XTALCAP=000000
3. Lower frequencies than 15.5 MHz or higher frequencies than 25 MHz can be used. However, not all typical RF frequencies can be generated.

RF Frequency Generation Subsystem (Synthesizer)

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{REF}	Reference frequency	Note 1		16, 24		MHz
f_{range_hi}	Frequency range	BANDSEL=0	800		940	MHz
f_{range_low}		BANDSEL=1	400		470	
f_{RESO}	Frequency resolution		1			Hz
BW_1	Synthesizer loop bandwidth	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		100		kHz
BW_2		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
BW_3		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		200		
BW_4		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		500		
T_{set1}	Synthesizer settling time for 1MHz step	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		15		µs
T_{set2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		30		
T_{set3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		7		
T_{set4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		3		
T_{start1}	Synthesizer start-up time if crystal oscillator and reference are running	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		25		µs
T_{start2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
T_{start3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		12		
T_{start4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		5		
$PN868_1$	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010	868 MHz, 50 kHz from carrier		-85		dBc/Hz
		868 MHz, 100 kHz from carrier		-90		
		868 MHz, 300 kHz from carrier		-100		
		868 MHz, 2 MHz from carrier		-110		
$PN433_1$		433 MHz, 50 kHz from carrier		-90		
		433 MHz, 100 kHz from carrier		-95		
		433 MHz, 300 kHz from carrier		-105		
		433 MHz, 2 MHz from carrier		-115		
$PN868_2$	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001	868 MHz, 50 kHz from carrier		-80		dBc/Hz
		868 MHz, 100 kHz from carrier		-90		
		868 MHz, 300 kHz from carrier		-105		
		868 MHz, 2 MHz from carrier		-115		
$PN433_2$		433 MHz, 50 kHz from carrier		-90		
		433 MHz, 100 kHz from carrier		-95		
		433 MHz, 300 kHz from carrier		-110		
		433 MHz, 2 MHz from carrier		-122		

Notes:

1. ASK, PSK and 1-200 kbps FSK with 16 MHz crystal, 200-350 kbps FSK with 24 MHz crystal

Transmitter

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate	ASK	1		2000	kbps
		FSK, note 2	1		350	
		PSK	10		2000	
		802.15.4 (DSSS) ASK and PSK	1		40	
		802.15.4 (DSSS) FSK	1		16	
PTX_{868}	Transmitter power @ 868 MHz	TXRNG=0000			-45	dBm
		TXRNG=0001		-5		
		TXRNG=0010		0.4		
		TXRNG=0011		4		
		TXRNG=0100		6.2		
		TXRNG=0101		8		
		TXRNG=0110		9.3		
		TXRNG=0111		10.3		
		TXRNG=1000		11.2		
		TXRNG=1001		11.9		
		TXRNG=1010		12.5		
		TXRNG=1011		13		
		TXRNG=1100		13.5		
		TXRNG=1101		13.8		
		TXRNG=1110		14		
		TXRNG=1111		14.5		
PTX_{433}	Transmitter power @ 433 MHz	TXRNG=1111		15.5		dBm
$PTX_{868\text{-}harm2}$	Emission @ 2nd harmonic	Note 1		-50		dBc
$PTX_{868\text{-}harm3}$	Emission @ 3rd harmonic			-55		

Notes

1. Additional low-pass filtering was applied to the antenna interface, see section 7: Application Information.
2. 1 – 200 kbps with 16 MHz crystal, 200 – 350 kbps with 24 MHz crystal

SPI Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high-Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period	Note 1	50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

Notes

1. For SPI access during power-down mode the period should be relaxed to 100ns.

For a figure showing the SPI timing parameters see section 5.11: Serial Peripheral Interface (SPI).

5. Circuit Description

The **AX5031** is a true single chip low-power CMOS transmitter primarily for use in SRD bands. The on-chip transmitter consists of a fully integrated RF front-end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication via the SPI interface.

AX5031 can be operated from a 2.2 V to 3.6 V power supply over a temperature range of -40°C to 85°C, it consumes 11 - 45 mA for transmitting, depending on the output power.

The **AX5031** features make it an ideal interface for integration into various battery powered SRD solutions such as ticketing or as transmitter for telemetric applications e.g. in sensors. As primary application, the transmitter is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 and the US Federal Communications Commission (FCC) standard CFR47, part 15. The use of **AX5031** in accordance to FCC Par 15.247, allows for improved range in the 915 MHz band. Additionally **AX5031** is compatible with the low frequency standards of 802.15.4 (ZigBee).

The **AX5031** receives data via the SPI port in frames. This standard operation mode is called Frame Mode. Pre and post ambles as well as checksums can be generated automatically. Interrupts control the data flow between a controller and the **AX5031**.

The **AX5031** behaves as a SPI slave interface. Configuration of the **AX5031** is also done via the SPI interface.

AX5031 supports any data rate from 1 kbps to 350 kbps for FSK and MSK, from 1 kbps to 2000 kbps for ASK and from 10 kbps to 2000 kbps for PSK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the **AX5031** are necessary, they are outlined in the following, for details see the **AX5031** Programming Manual.

Spreading is possible on all data rates and modulation schemes. The net transfer rate is reduced by a factor of 15 in this case. For ZigBee either 600 or 300 kbps modes have to be chosen.

5.1. Voltage Regulator

The **AX5031** uses an on-chip voltage regulator to create a stable supply voltage for the internal circuitry at pin VREG from the primary supply VDD_IO. All VDD pins of the device must be connected to VREG. The antenna pins ANTP and ANTN must be DC biased to VREG. The I/O level of the digital pins is VDD_IO.

The voltage regulator requires a 1µF low ESR capacitor at pin VREG.

In power-down mode the voltage regulator typically outputs 1.7V at VREG, if it is powered-up its output rises to typically 2.5V. At device power-up the regulator is in power-down mode.

The voltage regulator must be powered-up before transmit operations can be initiated. This is handled automatically when programming the device modes via the ***PWRMODE*** register.

Register ***VREG*** contains status bits that can be read to check if the regulated voltage is above 1.3 V or 2.3 V, sticky versions of the bits are provided that can be used to detect low power events (brown-out detection).

5.2. Crystal Oscillator

The on-chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference. Although a wider range of crystal frequencies can be handled by the crystal oscillator circuit, it is recommended to use 16 MHz as reference frequency for ASK and PSK modulations independent of the data rate. For FSK it is recommended to use a 16 MHz crystal for data rates below 200 kbps and 24 MHz for data rates above 200 kbps.

The oscillator circuit is enabled by programming the ***PWRMODE*** register. At power-up it is not enabled.

To adjust the circuit's characteristics to the quartz crystal being used without using additional external components, both the transconductance and the tuning capacitance of the crystal oscillator can be programmed.

The transconductance is programmed via register bits XTALOSCGM[3:0] in register ***XTALOSC***.

The integrated programmable tuning capacitor bank makes it possible to connect the oscillator directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register ***XTALCAP***.

5.3. SYSCLK Output

The SYSCLK pin outputs the reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[3:0] in the ***PINCFG1*** register set the divider ratio. The SYSCLK output can be disabled.

5.4. Power-on-reset (POR)

AX5031 has an integrated power-on-reset block. No external POR circuit or signal is required.

After POR the **AX5031** can be reset by SPI accesses, this is achieved by toggling the bit RST in the ***PWRMODE*** register.

After POR or reset all registers are set to their default values.

5.5. RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 µs depending on the settings (see section 4.3: AC Characteristics). Fast settling times mean fast start-up, which enables low-power system design.

The frequency must be programmed to the desired carrier frequency.

The synthesizer loop bandwidth can be programmed, this serves three purposes:

1. Start-up time optimisation, start-up is faster for higher synthesizer loop bandwidths
2. TX spectrum optimisation, phase-noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths
3. Adaptation of the bandwidth to the data-rate. For transmission of FSK and MSK it is required that the synthesizer bandwidth must be in the order of the data-rate.

VCO

An on-chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. The frequency can be programmed in 1 Hz steps in the ***FREQ*** or ***FREQB*** registers. To chose ***FREQB*** setting rather than ***FREQ***, the bit FREQSEL in register ***PLLLOOP*** must be set. For operation in the 433 MHz band, the BANDSEL bit in the ***PLLLOOP*** register must be programmed.

VCO Auto-Ranging

The **AX5031** has an integrated auto-ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power-up. The function is initiated by setting the RNG_START bit in the ***PLLRANGING*** register. The bit is readable and a 0 indicates the end of the ranging process. The RNGERR bit indicates the correct execution of the auto-ranging.

Loop Filter and Charge Pump

The **AX5031** internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The loop-filter has three configurations that can be programmed via the register bits FLT[1:0] in register ***PLLLOOP***, the charge pump current can be programmed using register bits PLLCPI[1:0] also in register ***PLLLOOP***. Synthesizer bandwidths are typically 50 - 500 kHz depending on the ***PLLLOOP*** settings, for details see the section 4.3: AC Characteristics.

Registers

Register	Bits	Purpose
PLLLOOP	FREQSEL	Switches between carrier frequencies defined by FREQ and FREQB. Using this feature allows to avoid glitches in the PLL output frequency caused by serially changing the 4 bytes required to set a carrier frequency.
	FLT[1:0]	Synthesizer loop filter bandwidth, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
	PLLCPI[2:0]	Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase-noise) for low data-rate transmissions.
	BANDSEL	Switches between 868 MHz/915 MHz and 433 MHz bands
FREQ		Programming of the carrier frequency
FREQB		Programming of the 2nd carrier frequency, switch to this carrier frequency by setting bit FREQSEL=1.
PLLRANGING		Initiate VCO auto-ranging and check results

5.6. RF Output Stage (ANTP/ANTN)

The **AX5031** uses fully differential antenna pins.

The PA drives the signal generated by the frequency generation subsystem out to the differential antenna terminals. The output power of the PA is programmed via bits TXRNG[3:0] in the register ***TXPWR***. Output power as well as harmonic content will depend on the external impedance seen by the PA, recommendations are given in the section 7: Application Information.

5.7. Encoder

The encoder is located between the Framing Unit and the Modulator. It can optionally transform the bit-stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level. Differential encoding is useful for PSK, because PSK transmissions can be received either as transmitted or inverted, due to the uncertainty of the initial phase. Differential encoding / decoding removes this uncertainty.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform Spectral Shaping. Spectral Shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self synchronizing feedback shift register.

The encoder is programmed using the register ***ENCODING***, details and recommendations on usage are given in the **AX5031** Programming Manual.

5.8. Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit-stream suitable for the modulator.

The Framing unit supports three different modes:

- HDLC
- Raw
- 802.15.4 compliant

The micro-controller communicates with the framing unit through a 32 level × 10 bit FIFO. The FIFO decouples micro-controller timing from the radio (modulator) timing. The bottom 8 bits of the FIFO contain transmit data. The top 2 bit are used to convey meta information in HDLC and 802.15.4 modes. They are unused in Raw mode. The meta information consists of packet begin / end information and the result of CRC checks. The FIFO can be written in power-down mode.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the micro-controller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. The **AX5031** signals interrupts by asserting (driving high) its IRQ line. The interrupt line is level triggered, active high. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Basic FIFO status (EMPTY, FULL, Overrun, Underrun, and the top two bits of the top FIFO word) are also provided during each SPI access on MISO while the micro-controller shifts out the register address on MOSI. See the SPI interface section for details. This feature significantly reduces the number of SPI accesses necessary.

HDLC Mode

Note: HDLC mode follows High-Level Data Link Control (HDLC, ISO 13239) protocol.

HDLC Mode is the main framing mode of the **AX5031**. In this mode, the **AX5031** performs automatic packet delimiting, and optional packet correctness check by inserting and checking a cyclic redundancy check (CRC) field.

The packet structure is given in the following table.

Flag	Address	Control	Information	FCS	(Optional Flag)
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In **AX5031** the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC-CCITT, CRC-16 or CRC-32.

For details on implementing a HDLC communication see the **AX5031** Programming Manual.

RAW Mode

In Raw mode, the **AX5031** does not perform any packet delimiting or byte synchronization. It simply serialises transmit bytes.

This mode is ideal for implementing legacy protocols in software.

802.15.4 (ZigBee)

802.15.4 uses binary phase shift keying (PSK) with 300 kbit/s (868 MHz band) or 600 kbit/s (915 MHz band) on the radio. The usable bit rate is only a 15th of the radio bit rate, however. A spreading function in the transmitter expands the user bit rate by a factor of 15, to make the transmission more robust.

In 802.15.4 mode, the **AX5031** framing unit performs the spreading according to the 802.15.4 specification.

The 802.15.4 is a universal DSSS mode, which can be used with any modulation or data rate as long as it does not violate the maximum data rate of the modulation being used. Therefore the maximum DSSS data rate is 16 kbps for FSK and 40 kbps for ASK and PSK.

5.9. Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA:

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bitrate
ASK	PA off	PA on	BW = BITRATE	2000 kBit/s
FSK / MSK /GFSK	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	BW = (1+h) ·BITRATE	350 kBit/s
PSK	$\Delta\Phi = 0^0$	$\Delta\Phi = 180^0$	BW = BITRATE	2000 kBit/s

h = modulation index. It is the ratio of the deviation compared to the bit-rate; $f_{deviation} = 0.5 \cdot h \cdot BITRATE$.

ASK = amplitude shift keying

FSK = frequency shift keying

MSK = minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation} = 0.25 \cdot BITRATE$; the advantage of MSK over FSK is that it can be demodulated more robustly.

PSK = phase shift keying

OQPSK = offset quadrature shift keying. The **AX5031** supports OQPSK. However, unless compatibility to an existing system is required, MSK should be preferred.

4-FSK = four frequencies are used to transmit two bits simultaneously during each symbol

Modulation	Symbol = 00	Symbol = 01	Symbol = 10	Symbol = 11	Max. Bitrate
4-FSK	$\Delta f = -3 \cdot f_{deviation}$	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	$\Delta f = +3 \cdot f_{deviation}$	400 kBit/s

All modulation schemes are binary.

5.10. PWRMODE Register

The ***PWRMODE*** register controls, which parts of the chip are operating.

PWRMODE **register**	**Name**	**Description**	**Typical Idd**
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltage is reduced to conserve leakage power. SPI registers are still accessible, but at a slower speed. FIFO access is possible.	0.25 µA
0100	VREGON	All digital and analog functions, except the register file, are disabled. The core voltage, however is at its nominal value for operation, and all SPI registers are accessible at the maximum speed.	140 µA
0101	STANDBY	The crystal oscillator is powered on; the transmitter is off.	500 µA
1100	SYNTHTX	The synthesizer is running on the transmit frequency. The transmitter is still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.	10 mA
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.	11 - 45 mA

A typical ***PWRMODE*** sequence for a transmit session :

Step	**PWRMODE**	**Remarks**
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	SYNTHTX	The synthesizer settling time is 5 – 50 µs depending on settings, see section AC Characteristics
4	FULLTX	Data transmission
5	POWERDOWN	

5.11. Serial Peripheral Interface (SPI)

The **AX5031** can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. Registers for setting up the **AX5031** are programmed via the serial peripheral interface in all device modes.

When the interface signal SEL is pulled low, a 16 bit configuration data stream is expected on the input signal pin MOSI, which is interpreted as D0...D7, A0...A6, R_N/W.

Data read from the interface appears on MISO.

Figure 3 shows a write/read access to the interface. The data stream is built of an address byte including read/write information and a data byte. Depending on the R_N/W bit and address bits A[6..0], data D[7..0] can be written via MOSI or read at the pin MISO.

R_N/W = 0 means read mode, R_N/W = 1 means write mode.

The read sequence starts with 7 bits of status information S[6..0] followed by 8 data bits.

The status bits contain the following information:

S6	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
PLL LOCK	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOSTAT(1)	FIFOSTAT(0)

SPI Timing

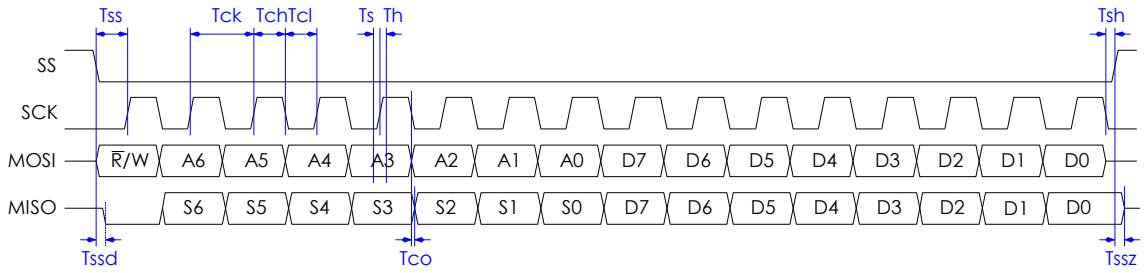


Figure 3 Serial peripheral interface timing

6. Register Bank Description

This section describes the bits of the register bank in detail. The registers are grouped by functional block to facilitate programming.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

Note Whole registers or register bits marked as reserved should be kept at their default values.

Note All addresses not documented here must not be accessed, neither in reading nor in writing.

6.1. Control Register Map

Addr	Name	Dir	Reset	Bit								Description
				7	6	5	4	3	2	1	0	
Revision & Interface Probing												
0	***REVISION***	R	00100001	SILICONREV(7:0)								Silicon Revision
1	***SCRATCH***	RW	11000101	SCRATCH(7:0)								Scratch Register
Operating Mode												
2	***PWRMODE***	RW	011-0000	RST	REFEN	XOEN	-	PWRMODE(3:0)				Power Mode
Crystal Oscillator, Part 1												
3	***XTALOSC***	RW	----0010	-	-	-	-	XTALOSCGM(3:0)				GM of Crystal Oscillator
FIFO, Part 1												
4	***FIFOCTRL***	RW	------11	FIFOSTAT(1:0)		FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOCMD(1:0)		FIFO Control
5	***FIFODATA***	RW	--------	FIFODATA(7:0)								FIFO Data
Interrupt Control												
6	***IRQMASK***	RW	-0000000	-	IRQMASK(6:0)							IRQ Mask
7	***IRQREQUEST***	R	--------	-	IRQREQUEST(6:0)							IRQ Request
Interface & Pin Control												
0C	***PINCFG1***	RW	00101000	-		IRQZ	-	SYSCLK(3:0)				Pin Configuration 1
0D	***PINCFG2***	RW	00000000	-		IRQE	-	-		IRQI	-	Pin Configuration 2
0E	***PINCFG3***	RW	0-------	reserved	-	-	SYSCLKR	-		IRQR	-	Pin Configuration 3
0F	***IRQINVERSION***	RW	-0000000	-	IRQINVERSION(6:0)							IRQ Inversion
Modulation & Framing												
10	***MODULATION***	RW	-0000010	-	MODULATION(6:0)							Modulation
11	***ENCODING***	RW	---00010	-	-	-	ENC NOSYNC	ENC MANCH	ENC SCRAM	ENC DIFF	ENC INV	Encoder/Decoder Settings

12	***FRAMING***	RW	-0000000	-	HSUPP	CRCMODE(1:0)		FRMMODE(2:0)		-		Framing settings
14	***CRCINIT3***	RW	11111111	CRCINIT(31:24)								CRC Initialization Data or Preamble
15	***CRCINIT2***	RW	11111111	CRCINIT(23:16)								CRC Initialization Data or Preamble
16	***CRCINIT1***	RW	11111111	CRCINIT(15:8)								CRC Initialization Data or Preamble
17	***CRCINIT0***	RW	11111111	CRCINIT(7:0)								CRC Initialization Data or Preamble
Voltage Regulator												
1B	***VREG***	R	--------	-	-	-	-	SSDS	SSREG	SDS	SREG	Voltage Regulator Status
Synthesizer												
1C	***FREQB3***	RW	00111001	FREQB(31:24)								2nd Synthesizer Frequency
1D	***FREQB2***	RW	00110100	FREQB(23:16)								2nd Synthesizer Frequency
1E	***FREQB1***	RW	11001100	FREQB(15:8)								2nd Synthesizer Frequency
1F	***FREQB0***	RW	11001101	FREQB(7:0)								2nd Synthesizer Frequency
20	***FREQ3***	RW	00111001	FREQ(31:24)								Synthesizer Frequency
21	***FREQ2***	RW	00110100	FREQ(23:16)								Synthesizer Frequency
22	***FREQ1***	RW	11001100	FREQ(15:8)								Synthesizer Frequency
23	***FREQ0***	RW	11001101	FREQ(7:0)								Synthesizer Frequency
25	***FSKDEV2***	RW	00000010	FSKDEV(23:16)								FSK Frequency Deviation
26	***FSKDEV1***	RW	01100110	FSKDEV(15:8)								FSK Frequency Deviation
27	***FSKDEV0***	RW	01100110	FSKDEV(7:0)								FSK Frequency Deviation
2C	***PLLLOOP***	RW	00011101	FREQSEL	reserved	BANDSEL	PLLCPI(2:0)			FLT(1:0)		Synthesizer Loop Filter Settings
2D	***PLLRANGING***	RW	00001000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCOR(3:0)				Synthesizer VCO Auto-Ranging
Transmitter												
30	***TXPWR***	RW	----1000	–	–	–	–	TXRNG(3:0)				Transmit Power
31	***TXRATEHI***	RW	00001001	TXRATE(23:16)								Transmitter Bitrate

32	***TXRATEMID***	RW	10011001	TXRATE(15:8)								Transmitter Bitrate
33	***TXRATELO***	RW	10011010	TXRATE(7:0)								Transmitter Bitrate
34	***MODMISC***	RW	------11	–	–	–	–	–	–	reserved	PTTLCK GATE	Misc RF Flags
FIFO, Part 2												
35	***FIFOCOUNT***	R	--000000	–	–	FIFOCOUNT(5:0)						FIFO Fill state
36	***FIFOTHRESH***	RW	--000000	–	–	FIFOTHRESH(5:0)						FIFO Threshold
37	***FIFOCONTROL2***	RW	0-----00	CLEAR	–	–	–	–	–	STOPONERR(1:0)		Additional FIFO control
Crystal Oscillator, Part 2												
4F	***XTALCAP***	RW	--000000	–	–	XTALCAP(5:0)						Crystal oscillator tuning capacitance
4-FSK control												
50	***FOURFSK***	RW	-------0	–	–	–	–	–	–	FOURFSKENA		4-FSK Control

7. Application Information

7.1. Typical Application Diagram

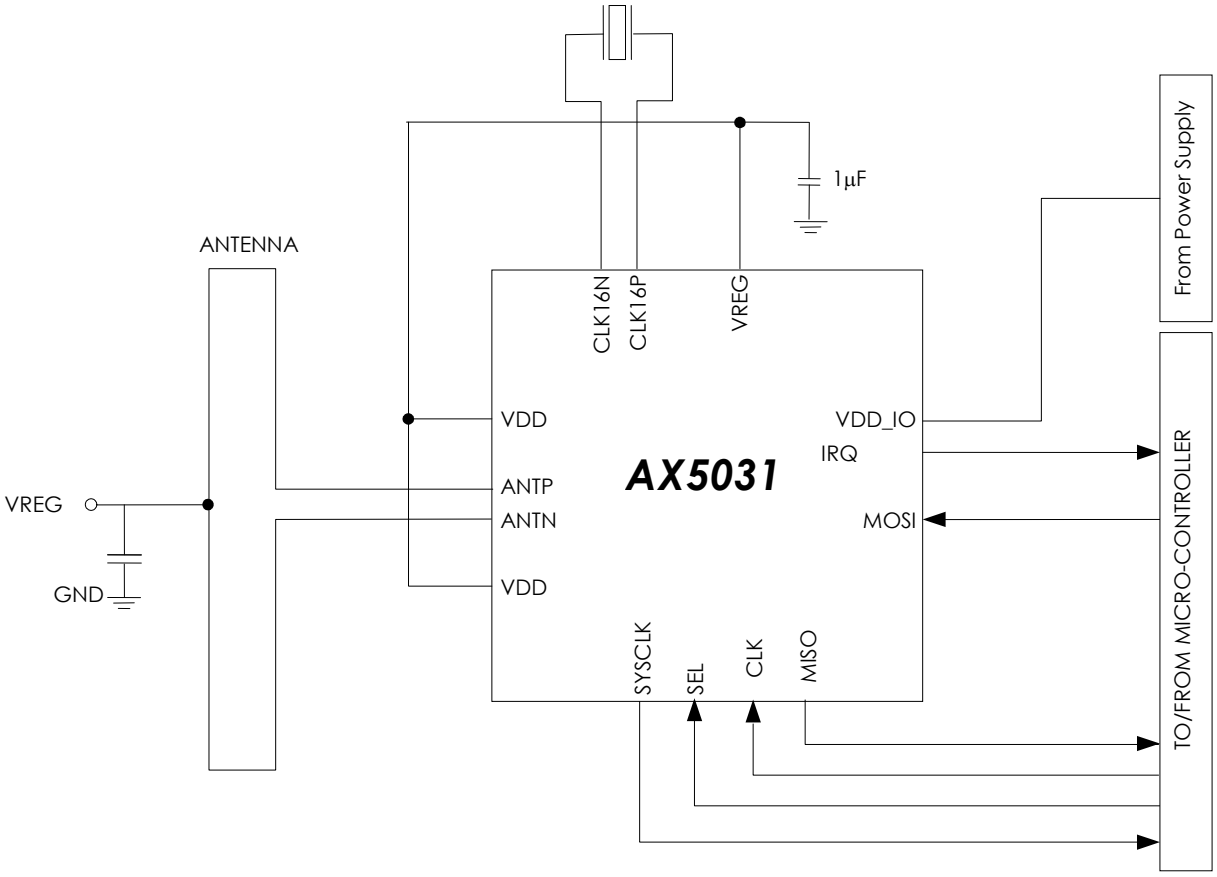


Figure 4 Typical application diagram

The GND connection to **AX5031** is made via the exposed center pad of the QFN package. It is mandatory to connect this pad to GND.

It is mandatory to add 1 µF (low ESR) between VREG and GND.
Decoupling capacitors are not all drawn. It is recommended to add 100 nF decoupling capacitor for every VDD and VDD_IO pin. In order to reduce noise on the antenna inputs it is recommended to add 27 pF on the VDD pins close to the antenna interface.

7.2. Antenna Interface Circuitry

A small antenna can be directly connected to the **AX5031** ANTP and ANTN pins with an optional translation network. The network must provide DC power to the PA. A biasing to VREG is necessary.

Beside biasing and impedance matching, the proposed network also provides low pass filtering to limit spurious emission.

Single-Ended Antenna Interface

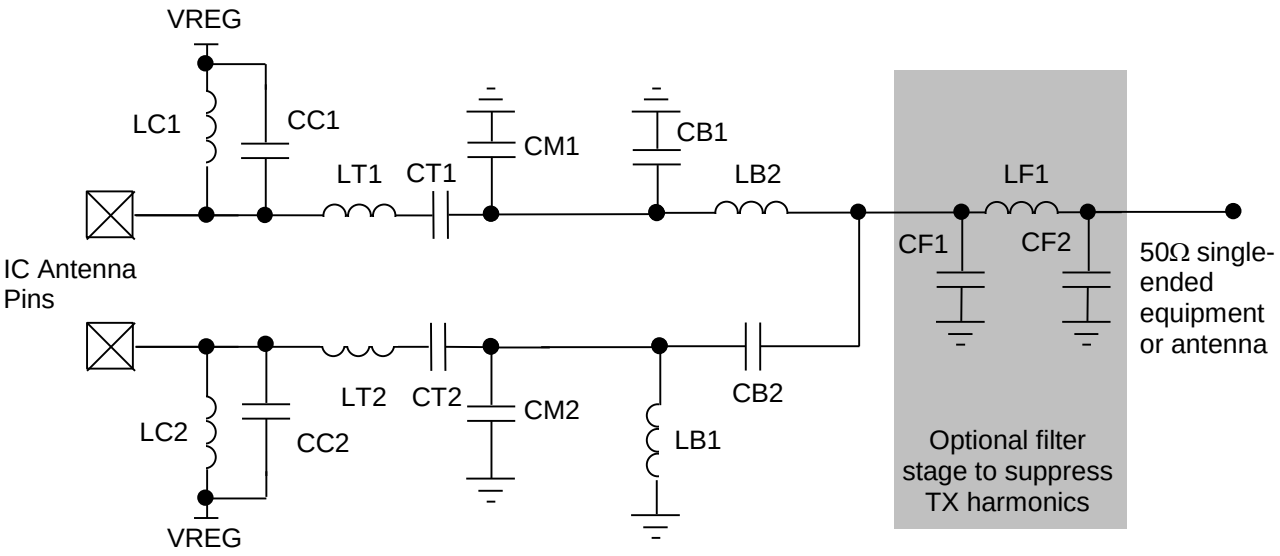


Figure 5 Structure of the antenna interface to 50 Ω single-ended equipment or antenna

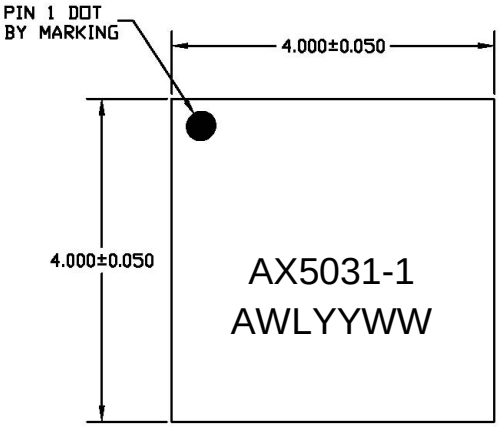
Frequency Band	LC1,2 [nH]	CC1,2 [pF]	LT1,2 [nH]	CT1,2 [pF]	CM1,2 [pF]	LB1,2 [nH]	CB1,2 [pF]	LF1 [nH]	CF1,2 [pF]
868 / 915 MHz	68	1.2	12	18	2.4	12	2.7	0 OHM	N.C.
433 MHz	120	2.7	39	7.5	6.0	27	5.2	0 OHM	N.C

7.3. Voltage Regulator

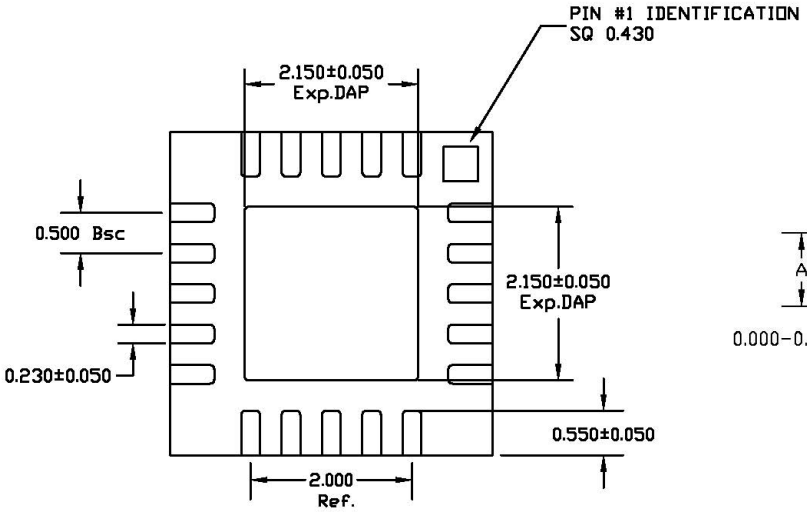
The **AX5031** has an integrated voltage regulator which generates a stable supply voltage VREG from the voltage applied at VDD_IO. Use VREG to supply all the VDD supply pins.

8. QFN20 Package Information

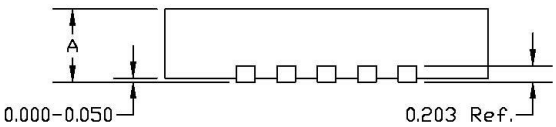
8.1. Package Outline QFN20



TOP VIEW



BOTTOM VIEW



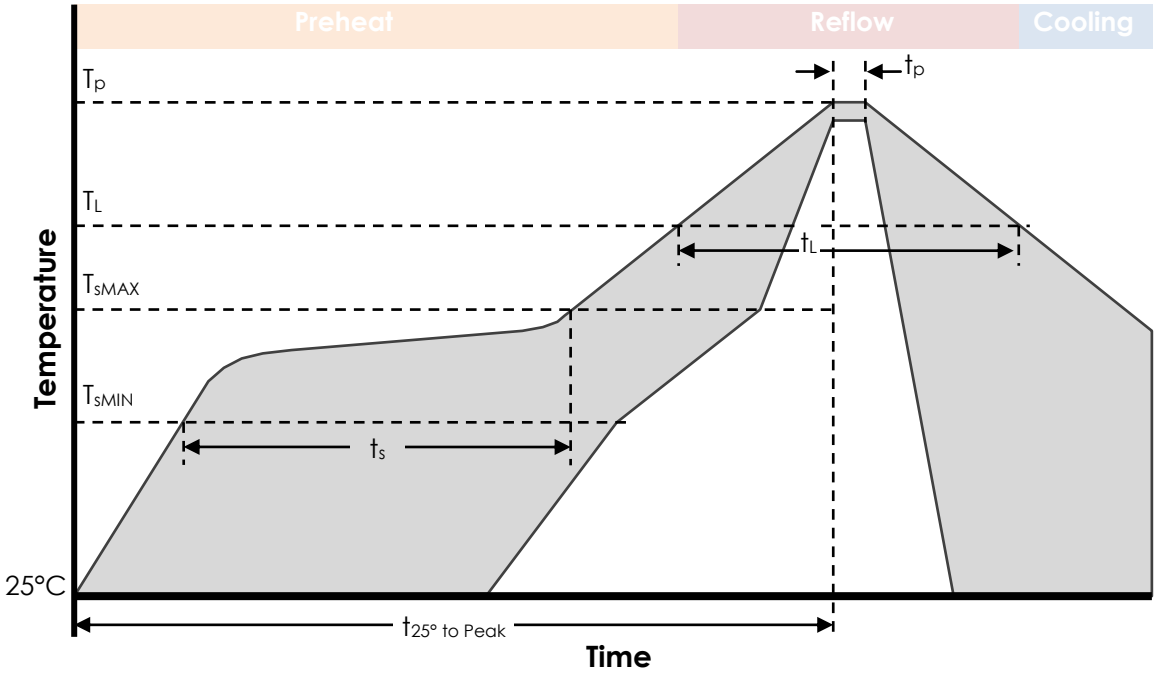
SIDE VIEW

A	MAX.	0.9
	NOM.	0.85
	MIN.	0.5

Notes

1. JEDEC ref MO-220
2. All dimensions are in millimetres
3. AWLYYWW is the packaging lot code
4. RoHS

8.2. QFN Soldering Profile

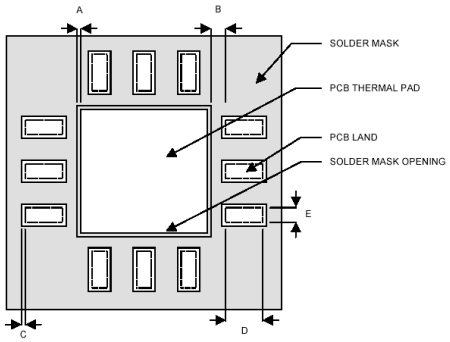


Profile Feature		Pb-Free Process
Average Ramp-Up Rate		3°C/sec max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 – 180 sec
Time 25°C to Peak Temperature	$T_{25\,°\,to\,Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 – 150 sec
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 – 40 sec
Cooling Phase		
Ramp-down rate		6°C/sec max.

Notes:
All temperatures refer to the top side of the package, measured on the package body surface.

8.3. QFN Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 6.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads
D = PCB land length = QFN solder pad length + 0.1mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 6: PCB land and solder mask recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.

3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

8.4. Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.

2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.

3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 7.

4. The aperture opening for the signal pads should be between 50-80% of the QFN pad area as shown in Figure 8.

5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.

6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.

7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

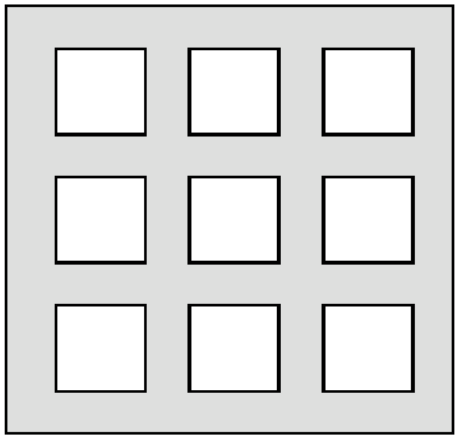


Figure 7: Solder paste application on exposed pad

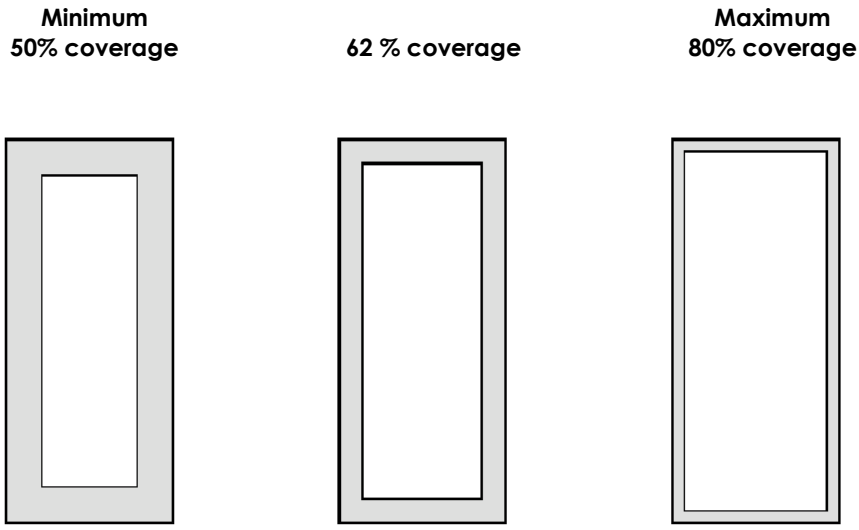


Figure 8: Solder paste application on pins



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