6-Key Capacitive Touch Controller Integrated with 3-LED Driver

FEATURES

- Configurable Touch Sensitivity
- RF Noise Filter
- Support Customize Gestures(slide and click)
- Automatic Calibration for Environmental Change
- Intrinsic Capacitance Compensation
- 8-grade LED Driver Maximum Current
- 9 bits PWM Resolution
- 256-grade Linear/Logarithmic PWM Dimming
- Internal Relation of Capacitive Touch to LED Driver
- Compatible I²C Interface(i2c addr: 0x2C/0x2D), Interface Voltage Range: 1.8V ~ 3.3V
- Single Power Supply, Voltage Range:3.0V~4.5V
- QFN3mm×3mm_20L Package

APPLICATIONS

Mobile Phones, MID

Portable Media Player

Home Appliances

GENERAL DESCRIPTION

AW9163 integrates 3 channel intelligent LED driver and 6 capacitive touch keys detection. The innovative “Dual Core” relates touch detection and LED driver. AW9163 can achieve the different LED effects depending on gesture without external MCU, which will reduce the power consumption and enhance the interactive experience in the application.

AW9163 scans the slight capacitance diff of touch keys with SIGMA-DELTA CDC(Capacitance Digital Convert) and detects the key touch with internal algorithm and reports the touch event.

AW9163 LED driver module uses co-anode current source and PWM dimming. LED driver has 8-grade maximum driver current. LED dimming can be controlled by external MCU or internal ASP module.

AW9163 supports the compatible I²C interface to communicate with external MCU. It supports 400kHz in fast mode. AW9163 is available in QFN3mm×3mm_20L package. The operating voltage range is 3.0V-4.5V.

TYPICAL APPLICATION CIRCUIT

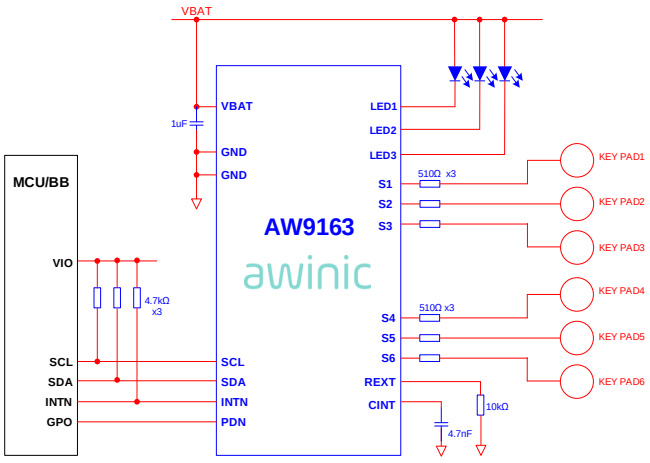


Figure 1 AW9163 Typical Application Circuit

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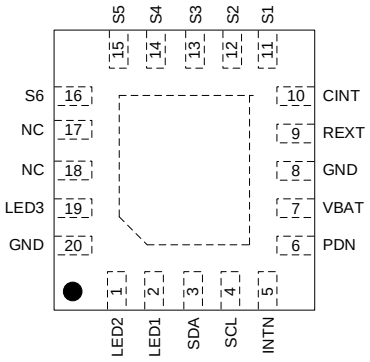
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1 PIN CONFIGURATION AND TOP MARK

AW9163 TOP View



AW9163 Marking



AW9163-AW9163QNR
XXXX-Producation Tracing Code

2 PIN DEFINITION

No.	NAME	DESCRIPTION
1	LED2	LED2 Cathode Driver, Anode connected to VBAT
2	LED1	LED1 Cathode Driver, Anode connected to VBAT
3	SDA	Serial Data I/O for I^2C Interface
4	SCL	Serial Clock Input for I^2C Interface
5	INTN	Interrupt Output (Open-drain), Low Active. (Typically tie 4.7kΩ resistor to V_{IO}).
6	PDN	Power Down Pin, Low Active(internal 1MΩ pull-down resistor)
7	VBAT	Power Supply (3.0V to 4.5V)
8	GND	Power Ground
9	REXT	External Resistor for adjusting sensitivity (typical is 10kΩ)
10	CINT	External Reference Capacitor(typical is 4.7nF)
11	S1	Capacitive Touch Input S1
12	S2	Capacitive Touch Input S2
13	S3	Capacitive Touch Input S3
14	S4	Capacitive Touch Input S4
15	S5	Capacitive Touch Input S5
16	S6	Capacitive Touch Input S6
17	NC	NC
18	NC	NC
19	LED3	LED3 Cathode Driver, Anode connected to VBAT
20	GND	Power Ground

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3 FUNCTIONAL BLOCK DIAGRAM

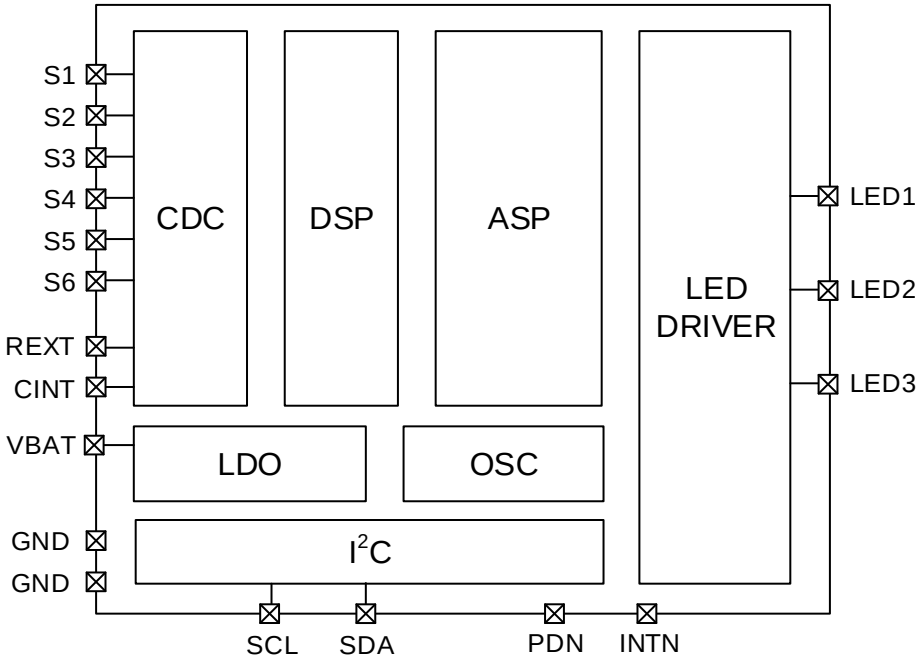


Figure 2 FUNCTIONAL BLOCK DIAGRAM

4 TYPICAL APPLICATION CIRCUITS

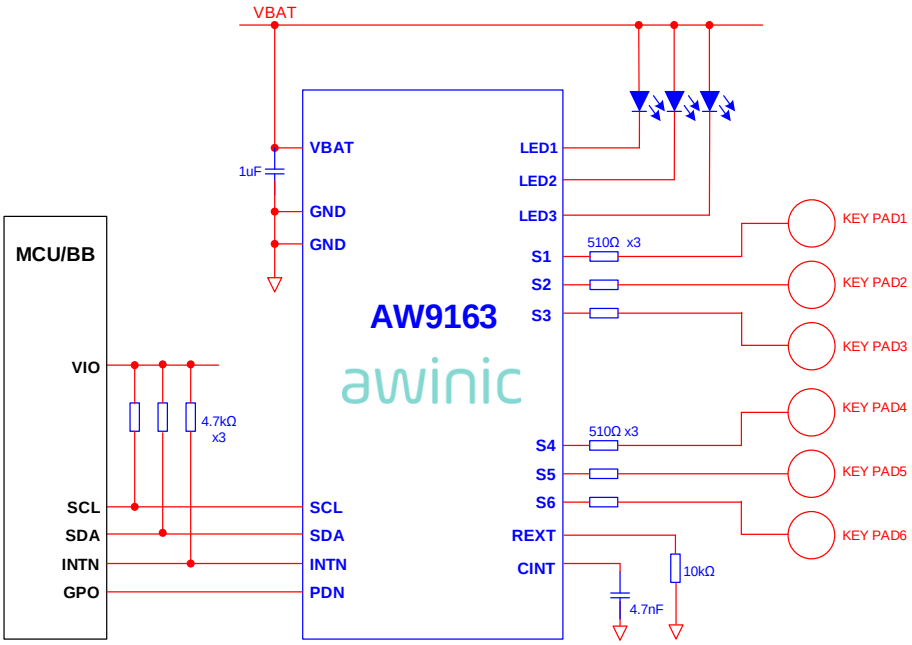


Figure 3 AW9163 Typical Application Circuit

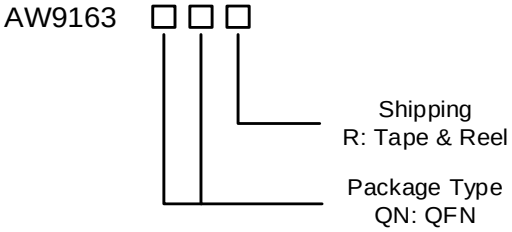
NOTE1、Pin S1/S2/S3 must be connected to a 500Ω ~ 600Ω resistor.

NOTE2、CINT and R_{EXT} should be placed as close as possible to the chip.

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5 ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9163QNR	-40℃～85℃	QFN3X3-20L	AW9163	MSL3	ROHS+HF	6000 units/ Tape and Reel



6 ABSOLUTE MAXIMUM RATINGS(NOTE 3)

PARAMETERS		RANGE
Supply voltage range V_{BAT}		-0.3V to 5V
Input voltage range	SCL, SDA	-0.3V to 3.6V
	PDN, LED1~3	-0.3V to 4.5V
Output voltage range	SDA, INTN	-0.3V to 3.6V
Junction-to-ambient thermal resistance θ_{JA}		45℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-55℃ to 125℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 4)		
HBM (human body model)		±4kV
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		+IT：450mA -IT：-450mA

NOTE3: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE4: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

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7 ELECTRICAL CHARACTERISTICS

V_{BAT}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

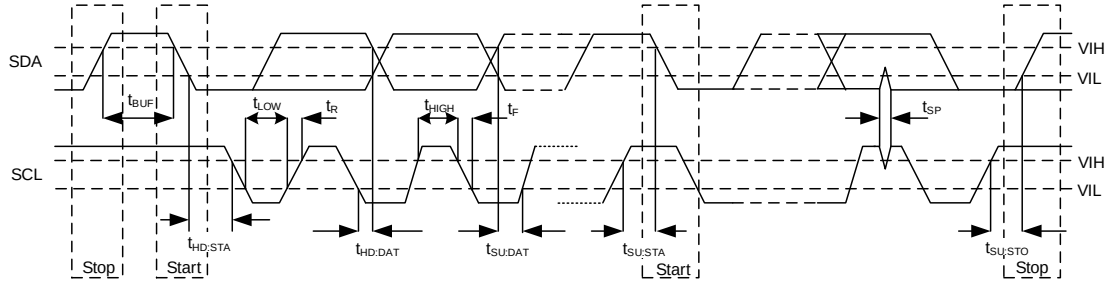
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{BAT}	Power supply	-	3.0	3.8	4.5	V
$I_{SHUTDOWN}$	Current in Shutdown mode	PDN=GND		8	15	μA
$I_{STANDBY}$	Current in Standby mode	PDN=V_{IO}		130	160	μA
I_{ACTIVE}	Current in LED Active mode	PDN=V_{IO}, GCR=0x01		0.55	0.8	mA
	Current in Touch Active mode	PDN=V_{IO}, GCR=0x02		0.85	1.0	mA
	Current in Touch & LED Active mode	PDN=V_{IO}, GCR=0x03		1.0	1.5	mA
F_{OSC}	Internal oscillator Frequency		14.8	16	17.2	MHz
Digital Logical Interface						
V_{IL}	Logic input high level	SDA,SCL,AD,PDN	-0.3		0.45	V
V_{IH}	Logic input low level	SDA,SCL,AD,PDN	0.9			V
I_{IL}	Low level input current	SDA,SCL,AD,PDN		5		nA
I_{IH}	High level input current	SDA,SCL,AD,PDN		5		nA
V_{OL}	Logic output low level	SDA, INTN I_{OUT}=3mA			0.4	V
I_{OL}	Maximum output current	SDA, INTN			10	mA
I_L	Output leakage current	SDA,INTN open drain			1	μA
I^2C Interface						
F_{SCL}	I^2C-BUS clock frequency				400	kHz
$T_{Deglitch}$	SCL deglitch time			200		ns
	SDA deglitch time			250		ns
Capacitance Button						
CX_{range}	Range(NOTE5)	CX	0		80	pF
$CX_{resolution}$	Resolution(NOTE5)	CX	0.02			pF
F_{SCAN}	Scan frequency			30		Hz
T_{DET}	Response time			100		ms
LED Driver						
I_{MAX}	LED MAX Current	I_{LED}=24.5mA	18.5	24.5	30.5	mA
I_{MATCH}	Matching accuracy	I_{LED}=24.5mA			10	%
V_{DROP}	Drop-out voltage	I_{LED}=24.5mA			300	mV
F_{PWM}	PWM frequency	LCR.FREQ=1	110	122	135	Hz
		LCR.FREQ =0	220	244	270	Hz

NOTE5：the value is tested in default configuration.

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8 I²C INTERFACE TIMING

Parameter Name			MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs



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9 FUNCTIONAL DESCRIPTION

9.1 WORK MODE

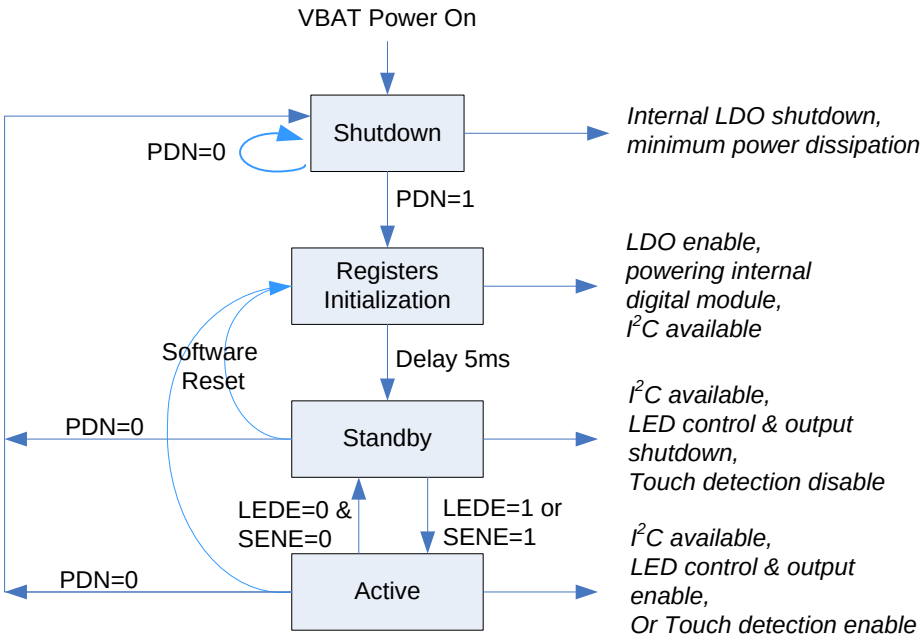


Figure 4 AW9163 Work Mode

AW9163 is in shut down mode and the consumption is less than 10μA if PDN pin is connected to low level. AW9163 generates power-on reset signal and initializes all internal register when PDN pin is changed from low level to high level. AW9163 will be in standby mode and I²C interface starts to work. Enable the Touch Module by configuring GCR.SENE=1 and enable the LED module by configuring GCR.LEDE=1. Then AW9163 enter the active mode.

9.2 RESET

9.2.1 Hardware Reset

When PDN pin changes from low level to high level, the power-up reset signal is generated and the whole chips registers will be reset.

9.2.2 Software Reset

Writing 0x55AA to register RSTR through I²C interface will produce a software reset and reset all registers.

9.3 I²C INTERFACE

AW9163 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW9163 can support different high level (1.8V~3.3V) of this I²C interface.

9.3.1 Device Address

The I²C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW9163 is 0x2C.

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0	1	0	1	1	0	0	R/$\overline{W}$

Figure 5 Device Address Configuration

9.3.2 Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

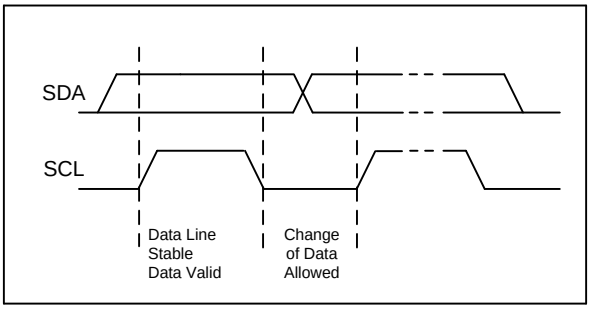


Figure 6 Data Validation Diagram

9.3.3 ACK(Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be releases; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, AW9163 sends 8bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, AW9163 sends the next data. If ACK is not sent by master, AW9163 stops to send data and waits for I²C stop.

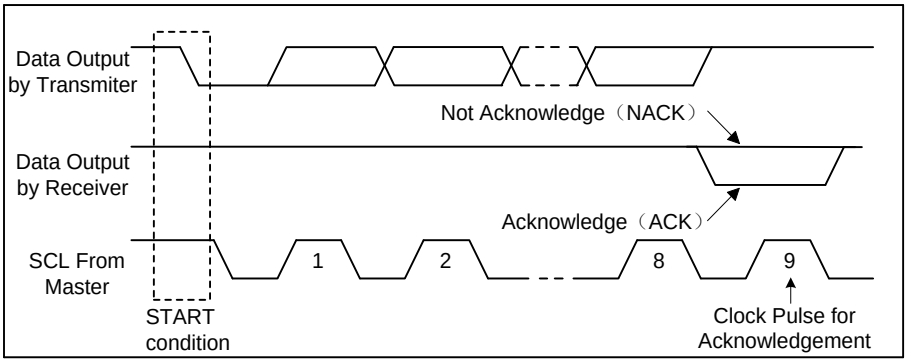


Figure 7 I²C ACK Timing

9.3.4 I²C Start/Stop

I2C start: SDA changes form high level to low level when SCL is high level.

I2C stop: SDA changes form low level to high level when SCL is high level.

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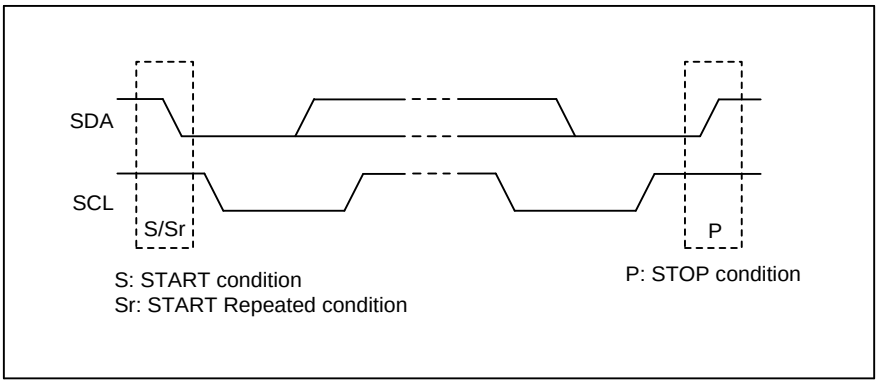


Figure 8 I²C Start/Stop Condition Timing

9.3.5 Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data high 8Bit to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends data low 8Bit to be written to the addressed register

I) Slave sends acknowledge signal

j) Master generates STOP condition to indicate write cycle end

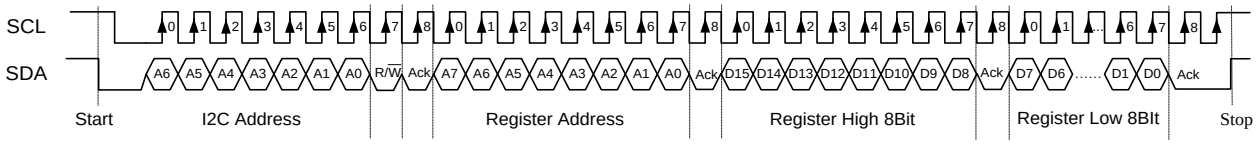


Figure 9 AW9163 I²C Write Timing

9.3.6 Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

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b) Master device sends slave address (7-bit) and the data direction bit (w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data high 8Bit from addressed register.

j) Master sends acknowledge signal

k) Slave sends data low 8Bit from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.

m) If the master device generates STOP condition, the read cycle is ended.

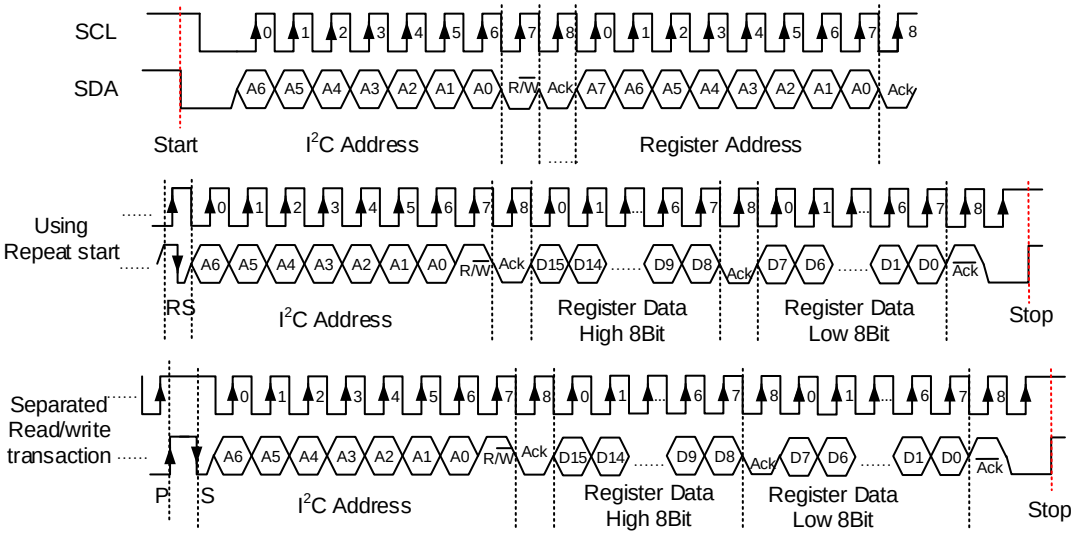


Figure 10 AW9163 I²C Read Timing

9.4 OSCILLATOR

AW9163 has an internal OSC for Capacitive touch module and LED driver module. GCR.SENE=1 can enable capacitive touch mode and GCR.LENE=1 can enable LED driver. The OSC start work and the start-up time is about 5 us. When GCR.SENE=0 & GCR.LEDE=0, the OSC module stops.

9.5 CAPACITIVE TOUCH DETECTION

AW9163 with self capacitive touch SIGMA-DELTA CDC detects the difference of capacitive sensor and judges the finger touch or not. Typically the key capacitance consist of the sensing electrode and GND without finger touching. When the finger with a conductive characteristics approaches, finger-Media-PCB constitute a parallel plate capacitor and the key capacitance parallel capacitor on the parasitic capacitance, resulting in buttons increasing capacitance. In general, because of the difference of electrode size and dielectric materials, the capacitive value of finger input is about 0.5pF～5pF.

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The resolution of AW9163 SIGMA-DELTA CDC is 12Bit. The CDC module transports the capacitive sample to DSP(digital filter, key judge function) and store the key status to register.

The capacitive sensitivity can be adjusted by REXT resistance. The bigger the REXT value, the higher the sensitivity. The default is 10KΩ to GND.

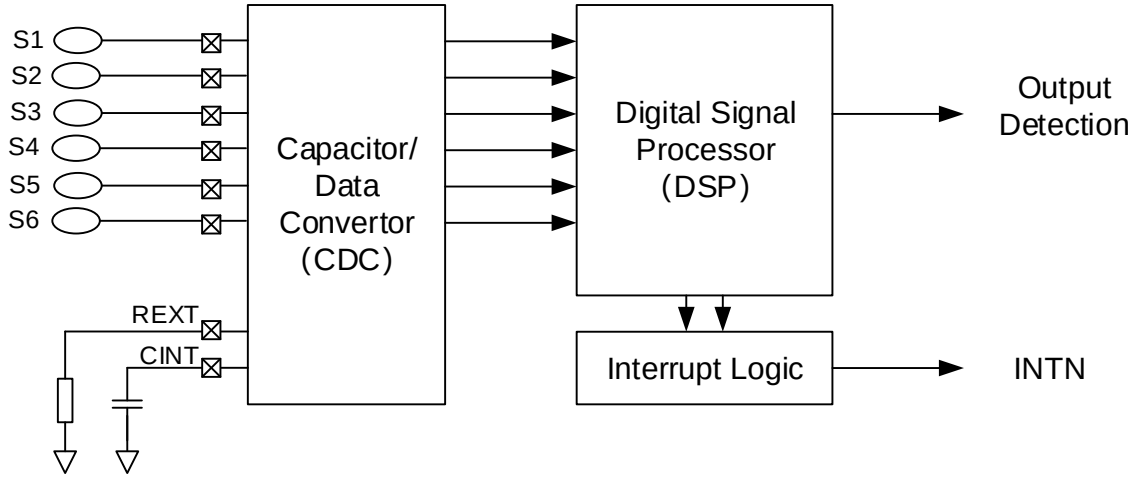


Figure 11 Functional Block of Capacitive Touch Detection Circuit

GCR.SENE=0 can reset all capacitive touch detection circuit. When GCR.SENE=1, the SLPR register control the enable/disable of every channel. SLPR.SLPx=1 will disable the x channel and save the consumption.

9.5.1 Key Status

AW9163 can detect 6-channel touch key and the key status can be read by register KEYST (0x31).

AW9163 supports the adjacent suppression function, identify and output the most likely key when multiple keys touch on the same time. Using the adjacent suppression function need set the register AKSCR (0x07) and select the keys.

Touching keys can generate the interrupt and the key interrupt can be selected by setting register KINTER (0x03). The interrupt mode is decided by KINTER.KIMD register.

- 00 interrupt generates when key press;
- 01 interrupt generates when key release;
- 10 interrupt generates when key status change;
- 11 interrupt generates when key status is 1.

The INTN pin will be pulled to GND when interrupt generates. The interrupt status can be clear by reading the register KISR (0x32) and INTN pin will be pull to V_{IO}.

9.5.2 Gesture Status

AW9163 with gesture detection function can identify the slide and click(single, double and triple click). The gesture module will report interrupt when detecting the setting gesture. It will save the external MCU consumption and improve the usability.

a) SLIP

SLIP detects the finger moving on control panel. When finger moves on touch keys, the capacitive change of key can be detected one by one. The gesture module can identify the order of touch key and judge the slide gesture.

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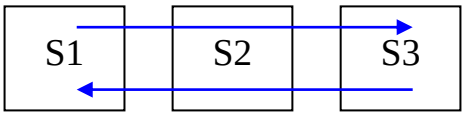


Figure 12 Gesture Detection Diagram

When finger slides key 1-2-3, the setting gesture is right slide; when finger slide 3-2-1, the setting gesture is left slide. AW9163 can report the setting gesture and the external MCU can perform the different operations.

b) TAP

When finger click the touchpad quickly, it can detect the single/double/triple click. The fast click will load the key status on temple ON status. With this touch feature, the TAP can be detected. In order to avoid inadvertently, the advice is using the double click function in the application.

The register GDCFGR (0x20) defines the gesture configure. GDCFGR.Bit4~2 set the gesture detection sensor channel. GDCFGR.Bit9~8 set the report mode.

GSTR1~2 can set 2 slide gesture and TAPR sets the click gesture.

Register GSTR:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	KCODE1			0	KCODE2			0	KCODE3			0	KCODE4		

KCODE1～4 define 3Bit key code.

KCODE： 1 --- S1
2 --- S2
3 --- S3
4 --- S4
5 --- S5
6 --- S6
0 --- No key

Register TAPR:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	CSEL						TIMES	

TIMES defines the click type, TIMES = 1, single click; TIMES=2, double click; TIMES=3, triple click.

CSEL selects the click keys. For example: CSEL=000001, key1 is used for click detection; CSEL=000011, key1 and key2 is used for click detection, any key of key1 and key2 is effective.

The register GIER(0x2D) can enable/disable corresponding gesture. The gesture result is transported to register GISR(0x2E). GISR.Bitx= 1 means the gesture is triggered. The GISR will be clear by reading.

9.6 LED DRIVER

AW9163 uses co-anode current source driver and control 3 channel LED through the ASP module.

GCR.LEDE=0 can reset LED driver circuit and disable LED output. LER.LENx=0 will disable the corresponding LED channel.

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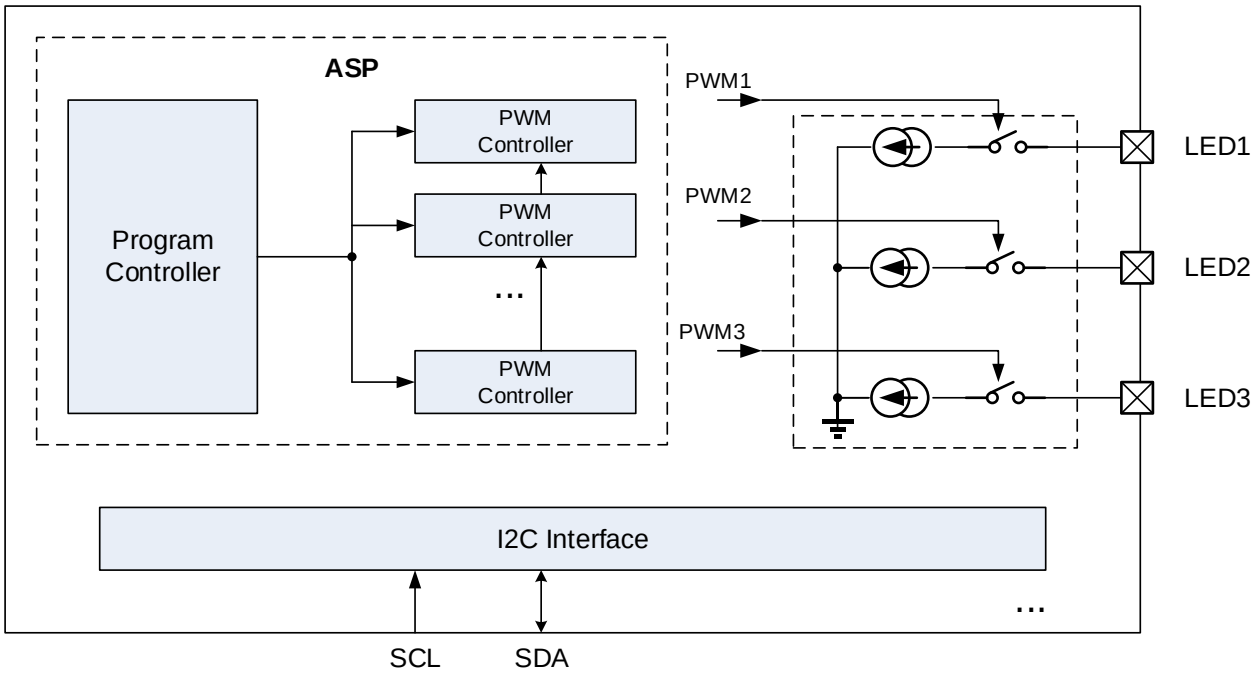


Figure 13 AW9163 LED Dimming Control Module Diagram

9.6.1 LED brightness controller

AW9163 uses 9Bit resolution PWM for dimming control. The PWM frequency is configured to 122/244Hz by register LCR.FREQ.

ASP generates the PWM signal with LED control instruction and controls 3 channel LED constant current source driver, achieving delicate brightness adjustment.

The LED control instruction ASP module executes comes from LED SRAM or external I^2C instruction. The register CTRS can choose the LED instruction source.

- CTRS[x] = 0, channel x LED controller uses the internal SRAM instruction;
- CTRS[x] = 1, channel x LED controller uses the external I^2C instruction.

9.6.2 LED Constant current driver

The output max current is 8-file optional set by register IMAXn. The LED constant current module achieve the brightness adjustment with ASP PWM signal.

9.6.3 ASP

ASP module is consist of one program controller and 3-channel PWM controller.

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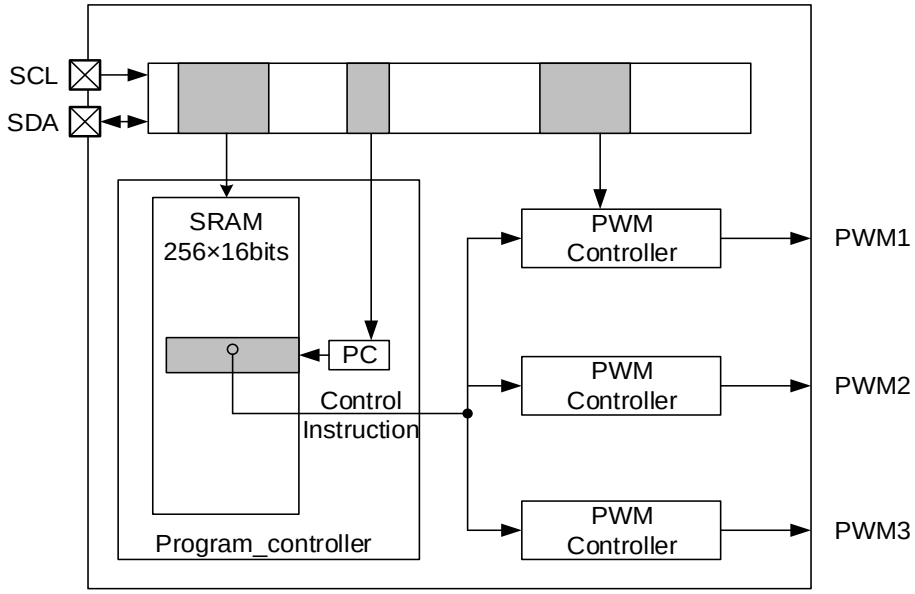


Figure 14 ASP Structure Diagram

9.6.3.1 Program Controller

The clock frequency of program controller is 32kHz and one instruction is executed per cycle. The programmer controller includes SRAM, internal registers.

256x16bit internal SRAM, loading the LED effect to SRAM by I2C interface and run/stop the program; Internal program registers RA/RB/RC/RD, used for LED effect program algorithm;

18x8bit internal data registers, 8bits data register R1~R8 and 10 particular registers. The address allocation and illustration is showed in the following table.

Table 1 Internal data register address allocation and illustration

Register	Address(HEX)	Illustration
R1	00	R1 data temporary register，8bit，I²C reading
R2	01	R2 data temporary register，8bit，I²C reading
R3	02	R3 data temporary register，8bit，I²C reading
R4	03	R4 data temporary register，8bit，I²C reading
R5	04	R5 data temporary register，8bit，I²C reading
R6	05	R6 data temporary register，8bit，I²C reading
R7	06	R7 data temporary register，8bit，I²C reading
R8	07	R8 data temporary register，8bit，I²C reading
KST_AKS	08	Key AKS status register
KST	09	Key original status register
TISR1	0a	Key interrupt status register, clear by reading
TISR2	0b	Key interrupt status register, clear by reading
-	0c	reserved
GMSK	0d	Global control mask register(M6~M1)
-	0e	reserved
-	0f	reserved
-	10	reserved
	11	reserved

Table 2 Particular registers detail illustration

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Register	B7	B6	B5	B4	B3	B2	B1	B0	Illustration
KST	-	-	K6	K5	K4	K3	K2	K1	Key original status, Kx=1, Sx is touched.
KST_AKS	-	-	AST6	AST5	AST4	AST3	AST2	AST1	Key AKS status, ASTx=1, Sx is touched.
TISR1	-	-	KINT6	KINT5	KINT4	KINT3	KINT2	KINT1	Key interrupt status, KINTx=1, Sx generate the interrupt. Clear by reading.
TISR2	-	-	-	TAP	-	-	G2	G1	Slide gesture1~2 and TAP interrupt status register. Clear by reading.
GMSK	-	-	-	M3	M2	M1	-	-	All LED controller instruction runs with shielding the setting channel(Mx=1).

9.6.3.2 PWM Controller

The PWM controller is the LED effect instruction execution unit. 3 PWM controllers receive the LED effect instruction and generate 8bit signal, transformed to 9bit brightness signal by Log/Lin algorithm. When LCR.LOGLN=00, the algorithm is about $\log_e$ logarithm; when LCR.LOGLN=01, the algorithm is $\log_{10}$ logarithm; when LCR.LOGLN=10, the algorithm is linearity. 9bit brightness signal is transformed to PWM signal controlling the LED driver by PWM generator.

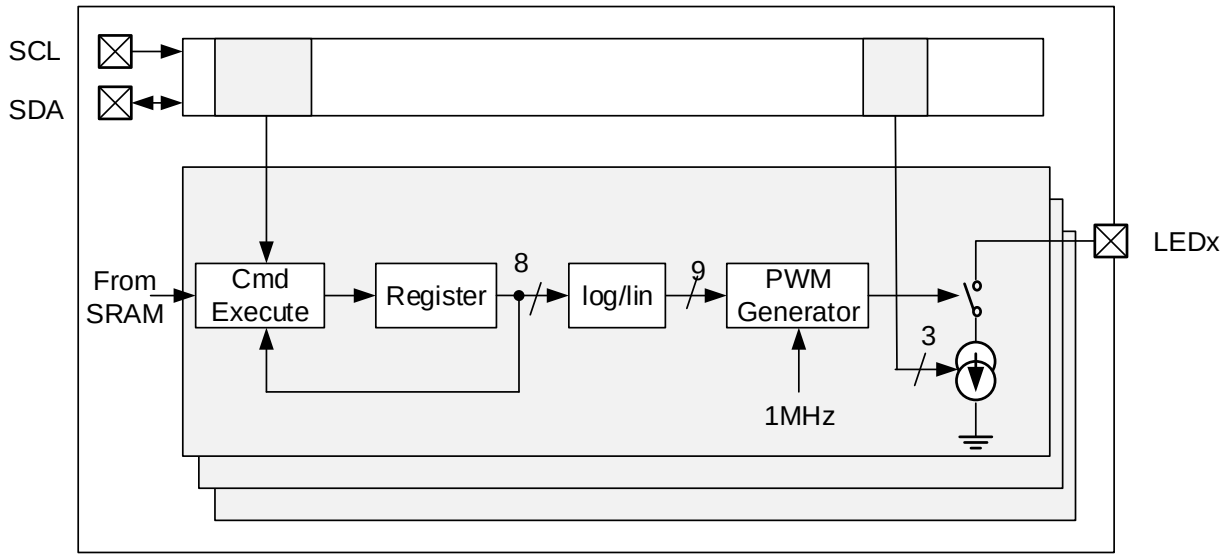


Figure 15 PWM Controller Schematic Diagram

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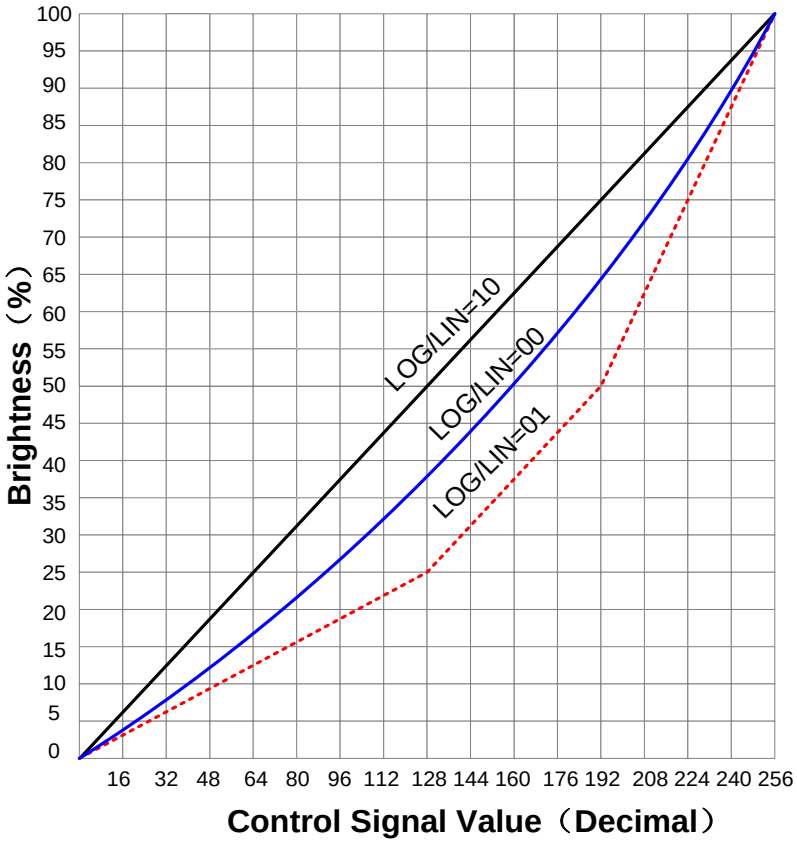


Figure 16 PWM Dimming Curve

9.6.3.3 Program Loading and controller

a) Program loading

Program loading can work only when PMD.PROGMD=00. The internal program can be read/write by I²C interface. When loading program, write the SRAM loading address to register WADDR(0x7E) and then write the 16bit LED effect instruction to register WDATA(0x7F). AW9163 supports sequential writing and the register WADDR will self plus 1 after writing the 16bit instruction.

b) Program controller

PMD.PROGMD and RMD.RUNMD can set the work mode of program controller.

Table 3 PMD.PUNMD illustration

PMD. PROGMD	Illustration
0 0	shutdown mode, used for loading program and setting PC point.
0 1	restart mode, set PC point as register SADDR and PMD.PROGMD changed to 10 automatically, the instruction start to run.
1 0	run mode, instruction runs with register RMD.RUNMD.

Table 4 RMD.RUNMD illustration

RMD.RUNMD	Illustration
0 0	Hold mode, program stop and PC hold.

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0 1	Step mode, execute the current instruction, PC add 1 and point to next instruction, set RMD.RUMND to be 00(Hold mode). It can be used for debugging SRAM program.
1 0	Run mode, program run from the PC point.
1 1	Repeat-run mode, execute the current instruction and PC hold. Set RMD.RUMD to be 00(Hold mode). It can be used for debugging SRAM program.

9.6.3.4 LED Effect Instruction

ASP uses efficient LED effect instruction to control LED dimming. It includes computing and jump instruction and achieve the complex LED effect.

The Rx/Ry/Rz of Instruction list means the internal register RA/RB/RC/RD.

Table 5 LED Effect Instruction

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JP	0	0	0	0	0	0	0	0	ADDR[7:0]							
NOP	0	0	0	0	0	0	0	1	-	-	-	-	-	-	-	-
-----	0	0	0	0	0	0	1	X								
JPZ Addr	0	0	0	0	0	1	0	0	ADDR[7:0]							
JPNZ Addr	0	0	0	0	0	1	0	1	ADDR[7:0]							
JPS Addr	0	0	0	0	0	1	1	0	ADDR[7:0]							
JPNS Addr	0	0	0	0	0	1	1	1	ADDR[7:0]							
LD Rz Im	0	0	0	0	1	0	Rz		Im[7:0]							
CMPI Rz Im	0	0	0	0	1	1	Rz		Im[7:0]							
ANDR Rz Im	0	0	0	1	0	0	Rz		Im[7:0]							
ORR Rz Im	0	0	0	1	0	1	Rz		Im[7:0]							
RDR Rz Addr	0	0	0	1	1	0	Rz		ADDR[7:0]							
WDR Rz Addr	0	0	0	1	1	1	Rz		ADDR[7:0]							
ADDI Rz Im	0	0	1	0	0	0	Rz		Im[7:0]							
AUBI Rz Im	0	0	1	0	0	1	Rz		Im[7:0]							
ADDR Rx Ry	0	0	1	0	1	0	Rz		-	-	-	-	Rx		Ry	
SUBR Rx Ry	0	0	1	0	1	1	Rz		-	-	-	-	Rx		Ry	
CMPR Rx Ry	0	0	1	1	0	0	0	0	-	-	-	-	Rx		Ry	
----	0	0	1	1	0	0	X	X								
END Int Rst	0	0	1	1	0	1	0	0	-	-	-	-	-	-	Int	Rst
INTN_MASKOFF	0	0	1	1	0	1	1	0	-	-	-	-	-	-	-	-
INTN_MASKON	0	0	1	1	0	1	1	1	-	-	-	-	-	-	-	-
WAITI Pre Time	0	0	1	1	1	Pre	T[9:0]									
SETPWMR Rx Ry	0	1	0	0	0	0	0	-	-	0	0	0	Rx		Ry	
RAMPR Dir Rx Ry	0	1	0	0	0	0	1	Dir	-	0	0	0	Rx		Ry	
SETSTEPTMRR Pre Rx Ry	0	1	0	0	0	1	0	-	Pre	0	0	0	Rx		Ry	

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SETSTEPTMRI Pre Ch Im	1	0	0	Ch[4:0]	Pre	-	Im[5:0]
SETPWMI Ch Im	1	0	1	Ch[4:0]	Im[7:0]		
RAMPI Dir Ch Im	1	1	Dir	Ch[4:0]	Im[7:0]		

LED Controller Instruction:

- **SETPWM:** set the LEDx brightness, 0~255;
- **RAMP：** set the LEDx Fade in/out steps, 0~255;
- **SETSTEP：** set the LEDx RAMP step time;

The LED controller instruction supports register parameters and immediate data in internal SRAM mode. The register is RA/RB/RC/RD.

With the internal SRAM instruction, when the Rx/Ch is '11111', the channel of CTRSR.bitx=0 is effective; when Rx/Ch is '11110', the channel of GMSKx=0 is effective.

When using the external I²C instruction, the LED controller instruction can only support immediate data mode.

Table 6 LED Control Instruction Illustration

Instruction	Illustration
Register Parameter	
SETPWMR Rx Ry	**Encoding: 0x40xx** **Set the PWM brightness level** Rx: LED channel number, 2~4 Ry: Brightness level, 0~255
RAMPR Dir Rx Ry	**Encoding: 0x43xx(Fade-in)/0x42xx(Fade-out)** **Set the steps of Fade-in/Fade-out** Dir: 1: Fade-in; 0: Fade-out Rx: LED channel number, 2~4 Ry: the steps of Fade-in/Fade-out
SETSTEPTMRR Pre Rx Ry	**Encoding: 0x44xx** **Set the RAMP step time** Pre: basic unit of time, 0: 0.5ms; 1: 16ms Rx: LED channel number, 2~4 Ry: RAMP step time = (Ry+1)*Pre, 0~255
Immediate Data	
SETPWMI Ch Im	**Encoding: 0xAxxx-0xBxxx** **Set the PWM brightness level** Ch: LED channel number, 2~4 Im: Brightness level, 0~255
RAMPI Dir Ch Im	**Encoding: 0xExxx-0xFxxx(Fade-in)** **0xCxxx-0xDxxx(Fade-out)** **Set the steps of Fade-in/Fade-out** Dir: 1: Fade-in; 0: Fade-out Ch: LED channel number, 2~4 Im: the steps of Fade-in/Fade-out
SETSTEPTMRI Pre Ch Im	**Encoding: 0x8xxx** **Set the RAMP step time** Pre: basic unit of time, 0: 0.5ms; 1: 16ms Ch: LED channel number, 2~4 Im: RAMP step time = (Im +1)*Pre, 0~255

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Table 7 Program Control and Compute Instruction Illustration

Instruction	Encoding	Illustration
Jump Instruction		
JP Addr	0x00xx	Immediate Jump, PC = Addr
JPZ Addr	0x04xx	Conditional Jump, Rz = 0, PC = Addr
JPNZ Addr	0x05xx	Conditional Jump, Rz != 0, PC = Addr
JPS Addr	0x06xx	Conditional Jump, Rz < 0, PC = Addr
JPNS Addr	0x07xx	Conditional Jump, Rz >= 0, PC = Addr
Data Transfer Instruction		
LD Rz Im	0x08xx - 0x0bxx	Transfer Immediate data to internal register Rz
RDR Rz Addr	0x18xx - 0x1bxx	Read the data of Addr and store to register Rz, hold flag S/Z
WDR Rz Addr	0x1cxx - 0x1fxx	Write the data of register Rz to Addr
Computation Instruction		
CMPI Rz Im	0x0cxx - 0x0fxx	Rz - Im, affect sign bit ‘S’ and zero flag ‘Z’
CMPR Rx Ry	0x30xx	Rz - Ry, affect sign bit ‘S’ and zero flag ‘Z’
ANDR Rz Im	0x10xx - 0x13xx	Rz = Rz & Im, affect sign bit ‘S’ and zero flag ‘Z’
ORR Rz Im	0x14xx - 0x17xx	Rz = Rz | Im, affect sign bit ‘S’ and zero flag ‘Z’
ADDI Rz Im	0x20xx - 0x23xx	Rz = Rz + Im, affect sign bit ‘S’ and zero flag ‘Z’
SUBI Rz Im	0x24xx - 0x27xx	Rz = Rz - Im, affect sign bit ‘S’ and zero flag ‘Z’
ADDR Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rz + Ry, affect sign bit ‘S’ and zero flag ‘Z’
SUBR Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rz - Ry, affect sign bit ‘S’ and zero flag ‘Z’
Control Instruction		
END Int Rst	0x34xx	Reset register RMD as 0 and choose interrupt/PC reset or not

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		Int: 0: no interrupt after instruction end; 1: generate interrupt after instruction end Rst: 0: PC add 1 after instruction end; 1: reset PC to SADDR after instruction end
INTN_MASKOFF	0x36xx	Unmask internal interrupt
INTN_MASKON	0x37xx	Mask internal interrupt
WAITI Pre Time	0x38xx - 0x3fxx	Wait time Pre: basic time unit, 0: 0.5ms; 1: 16ms Time: maximum:1023, wait time=Pre*Time

9.6.3.5 Example

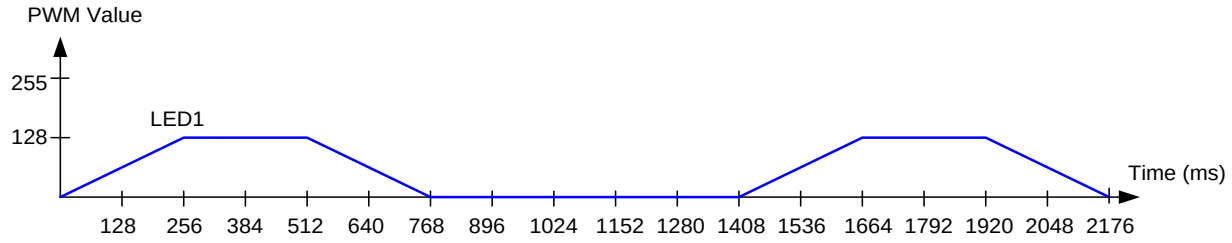


Figure 17 LED Effect Programming Diagram

Table 8 Reference Instruction of LED Effect Programming

PC	Assembly	Encoding	Illustration
0	SETSTEPTMRI 0x00 0x1F 0x03	0x9F03	RAMPI step time: 2ms
1	SETPWMI 0x1F 0x00	0xBF00	ALL LED turn off
	START:		
2	RAMPI 0x01 0x02 0x80	0xE280	LED1 fade in, 128 steps breath
3	WAITI 0x01 0x20	0x3C20	Wait 512ms
4	RAMPI 0x00 0x02 0x80	0xC280	LED1 fade out, 128 steps breath
5	WAITI 0x01 0x38	0x3C38	Wait 896ms
6	JP START	0x0002	Jump to START, PC=2

Step1: Power On, configure register

- VBAT power on, 4.2V
- Pull PDN to 3V
- Wait 5ms
- GCR = 0x0001
- LER = 0x0004
- IMAX1 = 0x0100
- PMD.PROGRMD = 00 (hold mode)
- RMD.RUNMD = 00 (hold mode)

Step2: Load Instruction to SRAM

- WADDR = 0x0000
- WDATA = 0x9F03
- WDATA = 0xBF00
- WDATA = 0xE280
- WDATA = 0x3C20
- WDATA = 0xC280

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- WDATA = 0x3C38
- WDATA = 0x0002

Step3: Run

- SADDR = 0x0000
- RMD.RUNMD = 10 (hold mode to run mode)
- PMD.PROGMD = 01 (run)

9.7 ASSOCIATE TOUCH KEY AND LED DRIVER

AW9163 supports 2 kinds of internal association between capacitive touch key and LED driver. They are immediate output association and ASP internal association with interrupt.

The immediate output association is transporting the touch key status to LEDx and generating the default LED effect.

ASP internal association with interrupt is that ASP can read key or gesture interrupt and trigger the interrupt program with complex LED effect.

9.7.1 Immediate Output Association

The touch key status is transport to the corresponding LEDx with configuring register OSRx. When pressing key, LED on; when releasing key, LED off.

When OSRx.OEx=1, Sx(x=1~6) status is transported to LED pin defined by OSRx.SELx.

- OSRx.LSELx=2, Sx output is LED1;
- OSRx.LSELx=3, Sx output is LED2;
- OSRx.LSELx=4, Sx output is LED3;

Register OSRx.FONx controls the LED mode from OFF to ON.

- OSRx.FONx=1, LEDx Fade in when key presses;
- OSRx.FONx=0, LEDx turns on immediately when key presses;

Register OSRx.FOFx controls the LED mode from ON to OFF.

- OSRx.FOFx=1, LEDx Fade out when key releases;
- OSRx.FOFx=0, LEDx turn off immediately when key releases;

When OSRx.FOFx/FONx=1, the speed of fade in/fade out can be configured by SETSTEP.

The recommended configuration is OSRx.FONx=0 and OSRx.FOFx=1.

9.7.2 ASP Internal Association

Key and gesture touch can trigger ASP interrupt handler and PC point will jump to the interrupt address of register TIVEC. The interrupt handler reads the interrupt status register TISRx and key status register KST/KST_AKS and generate the different LED effect with the interrupt source. Reading TISRx should be done at the beginning of interrupt handler and will clear the interrupt status.

ASP has 3 interrupt source and can be masked by configuring register TIER

- 6 key interrupt, choosing the interrupt mode by configuring LCR.LINMD
- 3 gesture interrupt (2 slide gesture and 1 tap gesture)

The key and gesture event interrupt has no priority.

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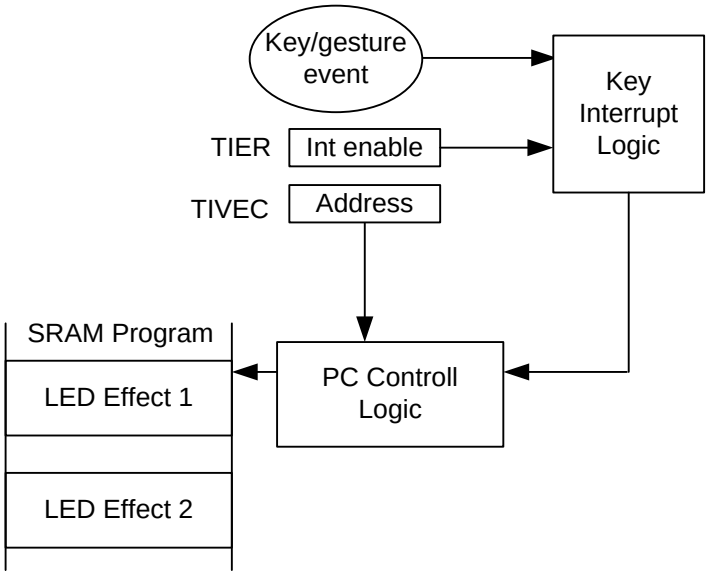


Figure 18 ASP Interrupt Response Diagram

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10 REGISTER DESCRIPTION

10.1 REGISTER CONFIGURATION

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IDRST	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	GCR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENE	LEDE
0x02	SLPR	0	0	0	0	0	0	0	0	0	0	SLP6	SLP5	SLP4	SLP3	SLP2	SLP1
0x03	KINTER	0	0	0	0	0	0	KIMD		FRME	0	IE6	IE5	IE4	IE3	IE2	IE1
0x04	OSR1	OE2	FON2	FOF2	0	0	LSEL2			OE1	FON1	FOF1	0	0	LSEL1		
0x05	OSR2	OE4	FON4	FOF4	0	0	LSEL4			OE3	FON3	FOF3	0	0	LSEL3		
0x06	OSR3	OE6	FON6	FOF6	0	0	LSEL6			OE5	FON5	FOF5	0	0	LSEL5		
0x07	AKSCR	0										ASEL					
0x08	SLSR	0	0	SLID_INTERVAL						TT	0	SLIDSEL					
0x09	-	RESERVED															
0x0a - 0x0f	JDGTHR1 - JDGTHR3	CLRTH								SETTH							
0x10	NOISETHR	0x08								NOISTH							
0x11	SCFG1	0	0	0		0		0		SCMD	0	NSMD	SCNUM				
0x12	SCFG2	0	0	0	0	0	SEED			RFFLTEN		0	SENS				
0x13	OFSR1	0	0	0	EN2	OFFSET2				0	0	0	EN1	OFFSET1			
0x14	OFSR2	0	0	0	EN4	OFFSET4				0	0	0	EN3	OFFSET3			
0x15	OFSR3	0	0	0	EN6	OFFSET6				0	0	0	EN5	OFFSET5			
0x16	DOFCR1	DOF4				DOF3				DOF2				DOF1			
0x17	DOFCR2	0	0	0	0	0	0	0	0	DOF6				DOF5			
0x18	IDLECR	INCR[7:0]								0	IPER[6:0]						
0x19	TIMR	0								MPT							
0x1A	DISMAX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x1B	SETCNT	CCNT								SCNT							
0x1C	BLCTH	BLU								BLD							
0x1D	BLDTH	0	0	0	0	0	0	0	0	BLDTH							
0x1E	MCR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSEL	
0x1F	-	RESERVED															
0x20	GDCFGR	0	0	0	0	0	0	GSTMD		AKST	AKSG	S6	S5	S4	S3	S2	S1
0x21	GDTR	0	0	0	0	0	0	0	0	GOFFMAX							
0x22	TDTR	ONMAX								TOFFMAX							

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Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x23	GEST1	0	KEY1			0	KEY2			0	KEY3			0	KEY4		
0x24	GEST2	0	KEY1			0	KEY2			0	KEY3			0	KEY4		
0x25	-	RESERVED															
0x26	-	RESERVED															
0x27	TAPR	0	0	0	0	0	0	0	0	K6	K5	K4	K3	K2	K1	TIMES	
0x28 - 0x2C	-	RESERVED															
0x2D	GIE	0	0	0	0	0	0	0	0	0	0	0	TIE1	0	0	GIE2	GIE1
0x2E	GIS	0	0	0	0	0	0	0	0	0	0	0	TIS1	0	0	GIS2	GIS1
0x2F	GTIM	0	0	0	0	0	0	0	0	GESTTIMER							
0x30	KISR	0	0	0	0	0	0	0	IDST	0	-	INT6	INT5	INT4	INT3	INT2	INT1
0x31	RAWST	0	0	0	0	0	0	0	0	0	0	S6	S5	S4	S3	S2	S1
0x32	KEYST	0	0	0	0	0	0	0	0	SBI	0	S6	S5	S4	S3	S2	S1
0x33 - 0x34	-	RESERVED															
0x35	SMOVCNT	0								MOVCNT							
0x36 ~ 0x3B	KDATA1 ~ KDATA6	KDATA															
0x3C	DUM0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
0x3D	DUM1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	LER	0	0	0	0	0	0	0	0	0	0	0	LE3	LE2	LE1	0	0
0x51	-	RESERVED															
0x52	LCR	0	0	0	0	0	0	0	SRMINI	LIRMD		TIMD		LIE	FREQ	LOG/LIN	
0x53	PROGMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	
0x54	RUNMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMOD	
0x55	CTRS	0	0	0	0	0	0	0	0	CTRSEL						0	
0x56	-	RESERVED															
0x57	IMAX1	0	IMAX2			0	IMAX1			0				0			
0x58	IMAX2	0	0			0	0			0	0			0	IMAX3		
0x59 - 0x5B	-	RESERVED															
0x5C	TIER	0	0	0	0	0	TIE1	0	0	GIE2	GIE1	KIE6	KIE5	KIE4	KIE3	KIE2	KIE1
0x5D	TIVEC	0	0	0	0	0	0	0	0	TIVEC							
0x5E	ISR2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS

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Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x5F	SADDR	0	0	0	0	0	0	0	0	SADDR							
0x60	PCR	0	0	0	0	0	0	0	0	PC							
0x61	CMDR	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x62	RA	0	0	0	0	0	0	0	0	RA							
0x63	RB	0	0	0	0	0	0	0	0	RB							
0x64	RC	0	0	0	0	0	0	0	0	RC							
0x65	RD	0	0	0	0	0	0	0	0	RD							
0x66 ~ 0x6D	R1 ~ R8	0								R1 ~ R8							
6E	GRP	0	0	0	0	0	0	0	0	GRPSEL						0	0
6F	-	RESERVED															
70 ~ 76	-	RESERVED															
7D	WP	WPW								0	0	0	0	0	0	0	0
7E	WAD	0	0	0	0	0	0	0	0	ADDR							
7F	WDA	CODE															

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10.2 GLOBAL REGISTER DESCRIPTION

10.2.1 IDRST, Chip ID and Software Reset

Address: 0x00, R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit	Symbol		Description												
15:0	IDRST		Chip ID: 0xB223 Software Reset: write 0x55AA to IDRST, reset all chip.												

10.2.2 GCR, Global Control Register

Address: 0x01, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENE	LEDE
Bit	Symbol		Description												
0	LEDE		LED driver function 0: disable LED driver 1: enable LED driver												
1	SENE		Touch Key detection function 0: disable touch key detection 1: enable touch key detection												

10.3 CAPACITIVE TOUCH DETECTION REGISTERS

10.3.1 SLPR, Sensor Channel Sleep Register

Address: 0x02, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	SLP6	SLP5	SLP4	SLP3	SLP2	SLP1
Bit	Symbol		Description												
5:0	SLP6~SLP1		Channel sleep control 0: Sx turn on 1: Sx shut down												

10.3.2 KINTER, Key Interrupt Enable Register

Address: 0x03, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	KIMD		FRME	0	IE6	IE5	IE4	IE3	IE2	IE1
Bit	Symbol		Description												
5:0	IEx		Key Interrupt enable register, pull INTN to GND when triggering interrupt. 0: disable interrupt 1: enable interrupt												
6	-		Reserved, must be 0												
7	FRME		Frame interrupt enable register 0: disable frame interrupt 1: enable frame interrupt												
9:8	KIMD		Interrupt mode 00: key status change, interrupt generate 01: key release, interrupt generate 10: key press, interrupt generate 11: key status is 1, interrupt generate												

10.3.3 OSR1~3, Associate Touch Status and LED Register

Address: 0x04~0x06, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OE2	FON2	FOF2	0	0	LSEL2			OE1	FON1	FOF1	0	0	LSEL1		
OE4	FON4	FOF4	0	0	LSEL4			OE3	FON3	FOF3	0	0	LSEL3		
OE6	FON6	FOF6	0	0	LSEL6			OE5	FON5	FOF5	0	0	LSEL5		

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Bit	Symbol	Description
15/7	OEx	Associate Sensor Channel(Sx) status and LEDx register 0: Disable association 1: Enable association
14/6	FONx	LED on effect mode 0: LED turn on immediately 1: LED fade in
13/5	FOFx	LED off effect mode 0: LED turn off immediately 1: LED fade out
10:8/ 2:0	LSELx	Binding LEDx with Sx (multiple keys binding to sample LEDx) LSEL=2, LED1 output LSEL=3, LED2 output LSEL=4, LED3 output LSEL=5, LED4 output LSEL=6, LED5 output LSEL=7, LED6 output
12:11/4:3	-	Reserved, must be 0

10.3.4 AKSCR, Adjacent Key Suppression Configuration Register

Address: 0x07, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	ASEL					

Bit	Symbol	Description
5:0	ASEL	Adjacent Key Suppression Configuration, only one of ASEL=1 keys can be triggered.

10.3.5 SLSR, Slide Configuration Register

Address: 0x08, R/W, default: 0x0200

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SLID_INTERVAL						TT	0	0	SLIDSEL			0	0

Bit	Symbol	Description
4:3	SLIDSEL	Slide Configuration 0: Unused for slide configuration 1: Used for slide configuration
6	-	Reserved, must be 0
7	TT	Sliders coordinate detection mode 0: Not end to end mode 1: End to end mode
13:8	SLD_INTERVAL	Key interval time of slider detection effective, T=SLIDINTVAL*Tscan(one frame cycle)

10.3.6 JDGTHRn, key status judge configuration register

Address: 0x0A~0x0F, R/W, default: 0x080F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRTH								SETTH							

Bit	Symbol	Description
7:0	SETTH	Touch on threshold
15:8	CLRTH	Touch off threshold

10.3.7 NOISETHR, Noise Threshold Register

Address: 0x10, R/W, default: 0x080F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x08								NOISETH							

Bit	Symbol	Description
7:0	NOISETH	Noise threshold
15:8	-	Reserved

10.3.8 SCFG1, Scan Configuration Register

Address: 0x11, R/W, default: 0x0004

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0		0		0		SCNMD	0	NSMD	SCNUM				

Bit	Symbol	Description
4:0	SCNUM	Scan cycle number, default is 4. The bigger scan cycle number, the longer scan time, the higher sensitivity. N=0, 256 N!=0, N*512
5	NSMD	Not scan channel configuration, default is 0. 0: connected to GND 1: hold Hi-Z
6	-	Reserved, must be 0
7	SCNMD	Scan mode 0: scan all keys, the cycle time is constant 1: scan the selected keys
15:8	-	Reserved, must be 0

10.3.9 SCFG2, Scan Configuration Register

Address: 0x12, R/W, default: 0x0107

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					SEED			RFFLTEN		0		SENS			

Bit	Symbol	Description
3:0	SENS	Sensitivity configuration, the litter SENS, the higher sensitivity (16 level sensitivity) 0000: 1 highest sensitivity 0001: 2 half of highest sensitivity 0011: 4 0111: 8 (default) 1111: 16
5:4	-	Reserved, must be 0
7:6	RFFLTEN	RF filter enable, when enable RF filter, SCFG1.SCNUM should be bigger than 4. 00: RF filter off 01: RF filter mode 1 enable 10: RF filter mode2 enable 11: RF filter off
10:8	SEED	ADC output data mode 000: ADC/16 001: ADC/8 010: ADC/4 011: ADC/2 100: ADC/1

10.3.10 OFSR1, Key Capacitance Offset Register

Address: 0x13, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFSEN2	OFFSET2				0	0	0	OFSEN1	OFFSET1			

Bit	Symbol	Description
3:0	OFFSET1	S1 capacitance offset value
4	OFSEN1	S1 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET2	S2 capacitance offset value
12	OFSEN2	S2 capacitance offset enable
15:13	-	Reserved, must be 0

10.3.11 OFSR2, Key Capacitance Offset Register

Address: 0x14, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFFSEN4	OFFSET4				0	0	0	OFSEN3	OFFSET3			

Bit	Symbol	Description

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3:0	OFFSET3	S3 capacitance offset value
4	OFSEN3	S3 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET4	S4 capacitance offset value
12	OFSEN4	S4 capacitance offset enable
15:13	-	Reserved, must be 0

10.3.12 OFSR3, Key Capacitance Offset Register

Address: 0x15, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFSEN6	OFFSET6				0	0	0	OFSEN5	OFFSET5			

Bit	Symbol	Description
3:0	OFFSET5	S5 capacitance offset value
4	OFSEN5	S5 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET6	S6 capacitance offset value
12	OFSEN6	S6 capacitance offset enable
15:13	-	Reserved, must be 0

10.3.13 DOFCR1-2, ADC Digital Offset Register

Address: 0x16-0x17, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOF4				DOF3				DOF2				DOF1			
-								DOF6				DOF5			

Bit	Symbol	Description
15:0	DOF6 DOF5 DOF4 DOF3 DOF2 DOF1	DOFx: ADC digital offset of Sx channel ADC data will over 12 Bits when key parasitic capacitance oversize. The digital offset can make the ADC data within acceptable range by minus the setting offset. 0000 : offset is 0 0001: offset is 2000 0010: offset is 4000 0011: offset is 6000 0100: offset is 8000 0101: offset is 10000 0110: offset is 12000 0111: offset is 14000 1xxx: undefined

10.3.14 IDLECR, IDLE Status Configuration Register

Address: 0x18, R/W, default: 0x1805															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INCR								0	IPER						

Bit	Symbol	Description
6:0	IPER	Scan key every n cycle time, default is 05H
7	-	Reserved, must be 0
15:8	INCR	Time of entering IDLE mode without touching, T=INCR*T_{SCAN}*16。

10.3.15 MPTR, Maximum permissible Time Register

Address: 0x19, R/W, default:0x0010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								MOT							

Bit	Symbol	Description
7:0	MOT	Maximum time of keeping touch status, T= MOT*T_{SCAN}*128 T_{SCAN} : capacitance touch key scanning cycle. T_{SCAN} = Keys * SCNUM * 2us
15:8	-	Reserved, must be 0

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10.3.16 DISMAX, Maximum Margin of Valid Data

Address: 0x1A, R/W, default: 0x0040																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
DISMAX																
Bit	Symbol	Description														
15:0	DISMAX	Maximum margin of valid data When the diff of two consecutive raw data over DISMAX, discard the raw data.														

10.3.17 SETCNT, Key Judge De-bounce Counter

Address: 0x1B, R/W, default: 0x0404															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT								SCNT							
Bit	Symbol	Description													
7:0	SCNT	Touch on de-bounce timer When detecting the touch delta over SETTHR n times continuously, touching on triggers interrupt.													
15:8	CCNT	Touch release de-bounce timer When detecting the touch delta below CLRTHR n times continuously, touching release triggers interrupt.													

10.3.18 BLCTH, Baseline Trace Configuration Register

Address: 0x1C, R/W, default: 0x1008															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLU								BLD							
Bit	Symbol	Description													
7:0	BLD	Baseline trace down The bigger the BLD, the slower the trace.													
15:8	BLU	Baseline trace up The bigger the BLU, the slower the trace.													

10.3.19 BLDTH, Baseline Reset Threshold

Address: 0x1D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								BLDTH							
Bit	Symbol	Description													
7:0	BLDTH	Baseline reset function is used for preventing raw data below the baseline abnormally. 0: baseline reset when baseline minus raw data over SETTHR x: Baseline reset when baseline minus raw data over BLDTH													
15:8	-	Reserved, must be 0													

10.3.20 MCR, Key Monitor Control Register

Address: 0x1E, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-			DSEL	
Bit	Symbol	Description													
1：0	DSEL	KDATA Output Mode 00: 0 01: delta of sensor 10: baseline of sensor 11: raw data of sensor													

10.3.21 GDCFGR, Gesture Detection Configuration Register

Address: 0x20, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	GSTMD		AKST	AKSG	S6	S5	S4	S3	S2	S1

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Bit	Symbol	Description
5:0	S6~S1	Gesture detection channel choice 0: disable gesture detection 1: enable gesture detection
6	AKSG	0: gesture detection without AKS key status 1: gesture detection with AKS key status
7	AKST	0: tap detection without AKS key status 1: tap detection with AKS key status
9:8	GSTMD	Gesture detection interrupt report mode 00: report after some time when finger leaving 01: report when finger leaving 1x: report when detecting gesture

10.3.22 GDTR, Gesture Detection Time Register

Address: 0x21, R/W, default: 0x07														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	GOFFMAX							

Bit	Symbol	Description
7:0	GOFFMAX	Maximum touch off time of gesture detection When finger moves, the touching cannot be detected some times. The gesture ends when the time of touch off over T_{OFFMAX}=GOFFMAX*T_{SCAN}.

10.3.23 TDTR, Tap Detection Register

Address: 0x22, R/W, default: 0x080F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TONMAX								TOFFMAX							

Bit	Symbol	Description
15:8	TONMAX	Maximum touch on time of tap detection The tap is invalid when touch on time over T_{ONMAX}=TONMAX*T_{SCAN}.
7:0	TOFFMAX	Maximum touch off time of tap detection When finger taps, the touching cannot be off some times. The tap ends when the time of touch off over T_{OFFMAX}=TOFFMAX*T_{SCAN}.

10.3.24 GSTR1~2, Gesture Configuration Register

GSTR1: address: 0x23, R/W, default: 0x2340
GSTR2: address: 0x24, R/W, default: 0x4320

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	KCODE1			0	KCODE2			0	KCODE3			0	0	0	0

Bit	Symbol	Description
14:12	KCODE1	Gesture order of number 1 sensor channel 0: None 1: S1 2: S2 3: S3 4: S4 5: S5 6: S6
10:8	KCODE2	Gesture order of number 2 sensor channel 0: None 1: S1 2: S2 3: S3 4: S4 5: S5 6: S6
6:4	KCODE3	Gesture order of number 3 sensor channel 0: None 1: S1 2: S2

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		3: S3 4: S4 5: S5 6: S6
3:0	-	Reserved, must be 0

The sensor channel is touched one by one when finger moves. AW9163 judges the touch order is the predefined order or not.

KCODE1 is the first touching sensor channel and then KCODE2/3 is detected.

Every gesture configuration must be more than 2 sensor channel and the other is set to 0.

The register is invalid if KCODE1 is 0.

10.3.25 TAPR, Tap Configuration Register

Address: 0x27, R/W, default: 0x12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	CSEL						TIMES	

Bit	Symbol	Description
1:0	TIMES	Click times 1: single click 2: double click 3: triple click
7:2	CSEL	Tap sensor channel selection

10.3.26 GIER, Gesture Interrupt Enable Register

Address: 0x2D, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	TIE	0	0	GIE2	GIE1

Bit	Symbol	Description
1:0	GIE2~1	Gesture detection interrupt 0: disable interrupt 1: enable interrupt
4	TIE	Tap detection interrupt 0: disable interrupt 1: enable interrupt
15:5	-	Reserved, must be 0

10.3.27 GISR, Gesture Interrupt Status Register

Address: 0x2E, R(clear by reading), default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	TIS	0	0	GIS2	GIS1

Bit	Symbol	Description
1:0	GIS2～1	Gesture detection interrupt status 0: no gesture interrupt 1: gesture interrupt
4	TIS	Tap detection interrupt status 0: no tap interrupt 1: tap interrupt
15:5	-	Reserved

10.3.28 GTIMR, Gesture Duration Register

Address: 0x2F, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	GTIMR							

Bit	Symbol	Description
7:0	GTIM	Gesture duration timer, from touch on to touch off T_{GEST} = GTIMR*T_{SCAN}, 0: no limit

10.3.29 RAWST, Raw Key Status Register

Address: 0x30, R, default: 0x0000

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IDLST	0	0	S6	S5	S4	S3	S2	S1

Bit	Symbol	Description
5:0	S6～1	Touch status 0: no touch 1: touch on
8	IDST	IDLE status 0: normal scan 1: IDLE mode status

10.3.30 KEYST, AKS Key Status Register

Address: 0x31, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	S6	S5	S4	S3	S2	S1

Bit	Symbol	Description
5:0	S6～1	AKS key status 0: no touch 1: touch on

10.3.31 KISR, Key Interrupt Status Register

Address:0x32, R(clear by reading), default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SBI	-	IS6	IS5	IS4	IS3	IS2	IS1

Bit	Symbol	Description
5:0	IS6～1	Key interrupt status 0: no key interrupt 1: key interrupt
6	-	Reserved
7	SBI	Set 1 every frame, clear by reading

10.3.32 MOVCNTR, Slider Move Counter Register

Address: 0x35, R(clear by reading), default: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	MOVCNTR							

Bit	Symbol	Description
7:0	MOVCNTR	Bit7 is sign bit, means the slide direction. Bit6-0 is the slide data.

10.3.33 KDATAn, Key Data Register

Address: 0x36~0x3B, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KDATAn															

Bit	Symbol	Description
15:0	KDATAn	Sn channel key data (refer register MCR(0x1E))

10.3.34 DUM0, Reserved Register

Address: 0x3C, R/W, default: 0x0FFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUM0															

Bit	Symbol	Description
15:0	DUM0	Reserved register, default is 0x0FFF

10.3.35 DUM1, Reserved Register

Address: 0x3D, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUM1															

Bit	Symbol	Description

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15:0	DUM1	Reserved register, default is 0x0000

10.4 LED EFFECT REGISTER

10.4.1 LER1, LED Driver Enable Register

Address: 0x50, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	LE3	LE2	LE1	0	0

Bit	Symbol	Description
4:2	LEx	LEDx output enable 0: disable output 1: enable output
15:8/1:0	-	Reserved, must be 0

10.4.2 LCR, LED Effect Configuration Register

Address: 0x52, R/W, default: 0x0080

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SRMINI	LIRMD		TIMD		LIE	FREQ	LOGLIN	

Bit	Symbol	Description
1:0	Log/Lin	Log/Linear dimming 00: log dimming 1, log(e) 01: log dimming 2, log10 1x: linear dimming
2	FREQ	PWM frequency 0: 244Hz 1: 122Hz
3	LIE	LED effect end interrupt 0: disable interrupt 1: enable interrupt
5:4	TIMD	Touch key interrupt mode for LED module 00: key status change, interrupt generate 01: key release, interrupt generate 10: key press, interrupt generate 11: key status is 1, interrupt generate
7:6	LIRMD	LED effect code run mode after interrupt request 00: hold mode, PC point can be changed, program hold and wait for RMD.RUNMD 01: step mode 10: run mode (default)
8	SRMINI	SRAM reset bit, write 1, reset SRAM; read SRAM status, default is 0.

10.4.3 PMD, Program Mode Register

Address: 0x53, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	

Bit	Symbol	Description
1:0	PROGMD	Program control mode 00: load program by I²C interface (default) 01: overload program and execute, set PC point to SADDR and change PROGMD to 10, run program 10: run program 11: undefined

10.4.4 RMD, Program Run Mode Register

Address: 0x54, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMD	

Bit	Symbol	Description
1:0	RUNMD	SRAM program run mode (CTRSEL=0)

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		00: hold mode, program stop and hold PC point 01: step mode, execute the current program, PC point add 1 and set RUNMD to 00 10: run mode, program run from PC point 11: repeat mode, execute the current program, set PC point to 00

10.4.5 CTRSR, LED Control Source Register

Address: 0x55, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	CTRSEL			0	
Bit	Symbol		Description												
4:2	CTRSEL		LED control source 0: SRAM control 1: I²C interface control												

10.4.6 IMAX1～IMAX6, LEDx Maximum Output Current Register

Address: 0x57~0x58, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IMAX2			0	IMAX1			0							
0												0	IMAX3		
Bit	Symbol		Description												
10:8 14:12 2:0	IMAX1 IMAX2 IMAX3		LEDx maximum output current 000: 0mA 001: 3.5mA 010: 7.0mA 011: 10.5mA 100: 14.0mA 101: 17.5mA 110: 21.0mA 111: 24.5mA												

10.4.7 TIER, Touch Key Interrupt for LED Enable Register

Address: 0x5C, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	TIE	0	0	GIE2	GIE1	KIE6	KIE5	KIE4	KIE3	KIE2	KIE1
Bit	Symbol		Description												
5:0	KIE6~1		Touch key interrupt enable 0: disable interrupt 1: enable interrupt												
7:6	GIE2~1		Gesture interrupt enable 0: disable interrupt 1: enable interrupt												
10	TIE		Tap interrupt enable 0: disable interrupt 1: enable interrupt												

10.4.8 TIVEC, Touch Key Interrupt Vector Register

Address: 0x5D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TIVEC							
Bit	Symbol		Description												
7:0	TIVEC		Touch key interrupt trigger, SRAM PC point jump target address.												

10.4.9 LISR, LED Interrupt Status Register

Address: 0x5E, R(clear by reading), default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS
Bit	Symbol		Description												
0	LIS		LED program end interrupt status, END can request interrupt to report external MCU												

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		when LED SRAM code finish. 0: no interrupt 1: interrupt request

10.4.10 SADDR, Program Start Address Register

Address: 0x5F, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SADDR							
Bit	Symbol		Description												
7:0	SADDR		SRAM program start address Program start to run from SADDR when PMD.PROGMD=01.												

10.4.11 PCR, LED Program Control Point Register

Address: 0x60, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ADDR							
Bit	Symbol		Description												
7:0	ADDR		Program control point(PC) PC point can be changed by I²C interface. Generally set the PC point when PMD.PROGMD is 00 and program jump to PC when PMD.PROGMD changed form 00 to 10.												

10.4.12 CMDR, LED Command Register

Address: 0x61, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD															
Bit	Symbol		Description												
15:0	CMD		CMDR is used to send external LED command when CTRSR is I²C interface control mode.												

10.4.13 RA/RB/RC/RD,LED Internal Program Register

Address: 0x62~0x65, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	RA							
0	0	0	0	0	0	0	0	RB							
0	0	0	0	0	0	0	0	RC							
0	0	0	0	0	0	0	0	RD							
Bit	Symbol		Description												
7:0	RA/RB/RC/RD		LED internal program register												

10.4.14 R1~R8, LED Internal Data Register

Address: 0x66~0x6D, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	R1							
0	0	0	0	0	0	0	0	R2							
0	0	0	0	0	0	0	0	R3							
0	0	0	0	0	0	0	0	R4							
0	0	0	0	0	0	0	0	R5							
0	0	0	0	0	0	0	0	R6							
0	0	0	0	0	0	0	0	R7							
0	0	0	0	0	0	0	0	R8							
Bit	Symbol		Description												
7:0	R1～R8		LED internal data register												

10.4.15 GRP, LED Group Operation Register

Address: 0x6E, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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0	0	0	0	0	0	0	0	0	0	0	GRPSEL	0	0
Bit	Symbol		Description										
4:2	GRPSEL		LEDx group operation, used for massing LED instruction When the LED instruction channel is 0x1E, the channel of GRPSEL is effective.										

10.4.16 WADDR, LED Program Loading Address Register

Address: 0x7E, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ADDR							
Bit	Symbol		Description												
7:0	ADDR		LED program loading address												

10.4.17 WDATA, LED Program Loading Data Register

Address: 0x7F, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE															
Bit	Symbol		Description												
15:0	CODE		16bit LED program code												

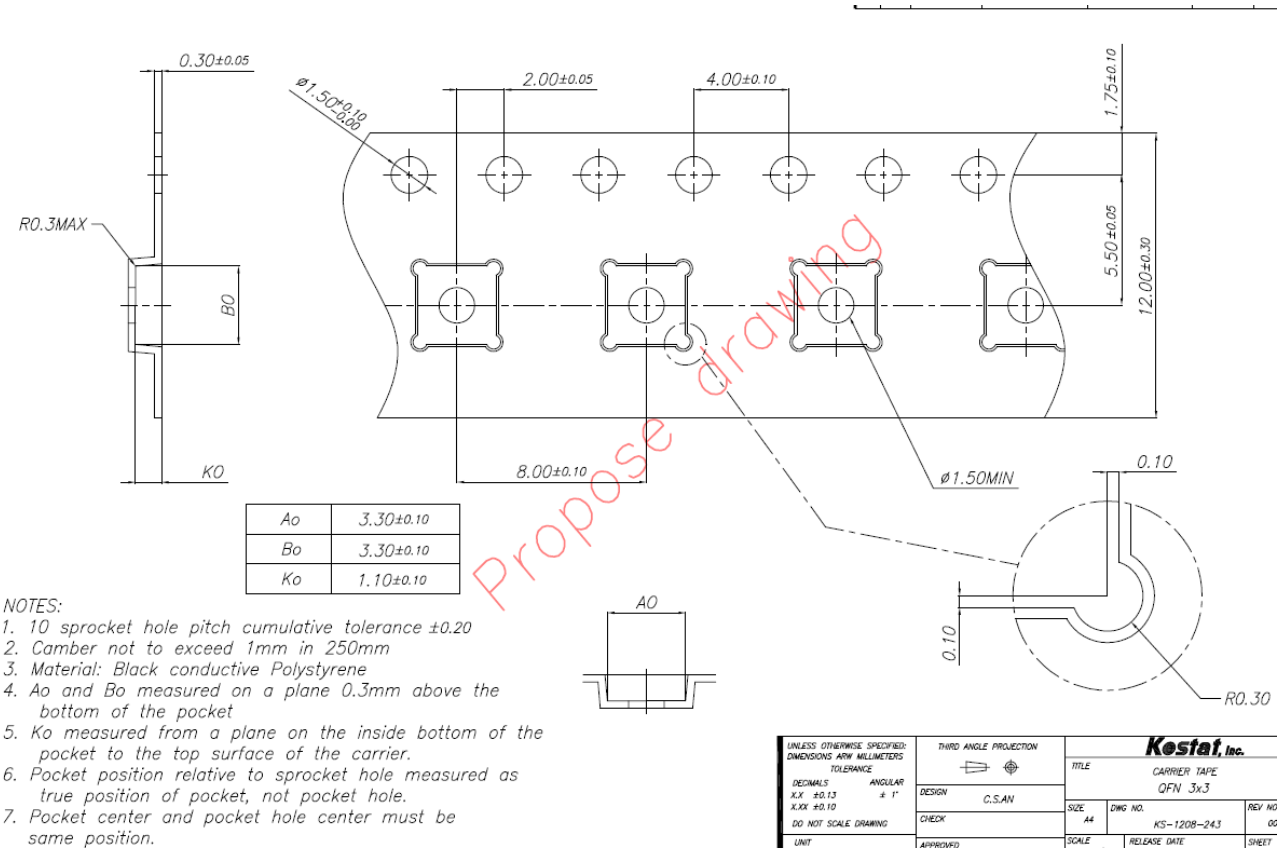
10.4.18 WPR, Writing Protection Register

Address: 0x7D, R/W, default: 0x5500															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPW								0	0	0	0	0	0	0	0
Bit	Symbol		Description												
15:8	WPW		8bit writing protection When WPW is 55H, I2C interface can write other registers; when WPW is not 55H, the other registers cannot be written.												

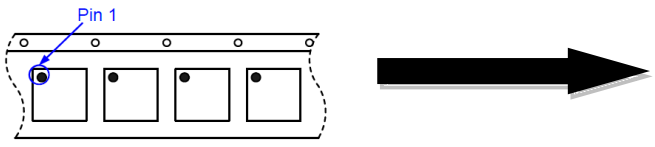
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11 TAPE AND REEL INFORMATION

11.1 Carrier Tape



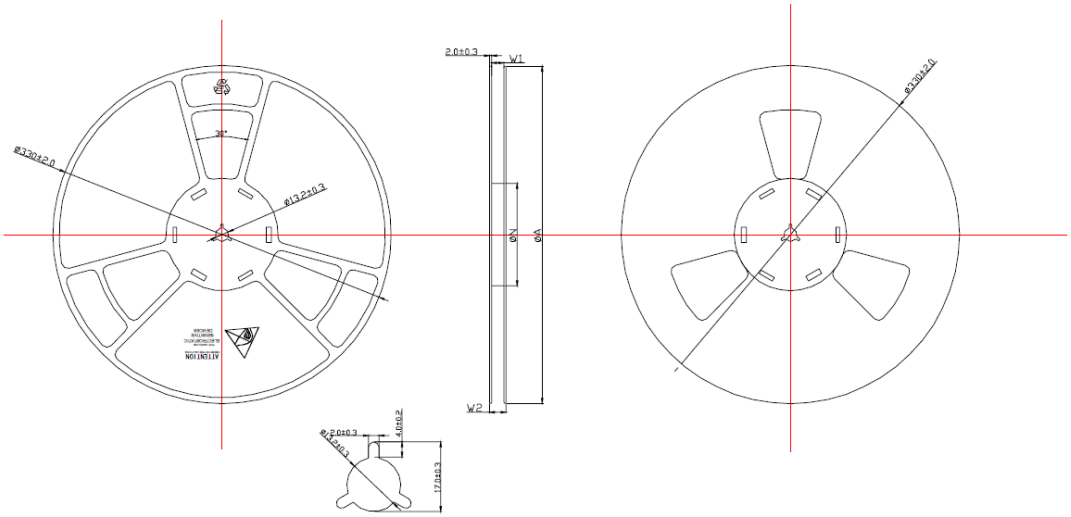
11.2 PIN1 Direction



User Direction of Feed

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11.3 Reel



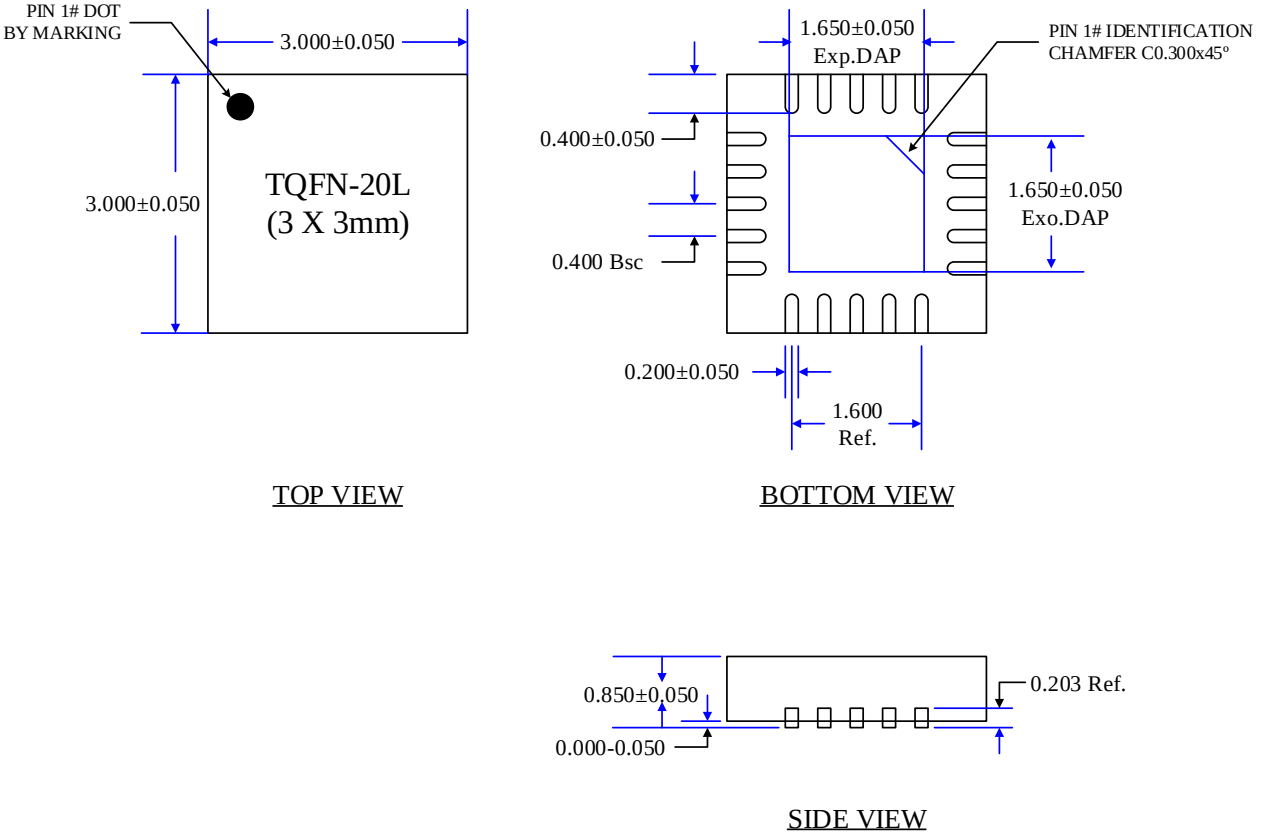
PRODUCT SPECIFICATIONS				
TYPE WIDTH	∅A	∅N	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4

Notes:

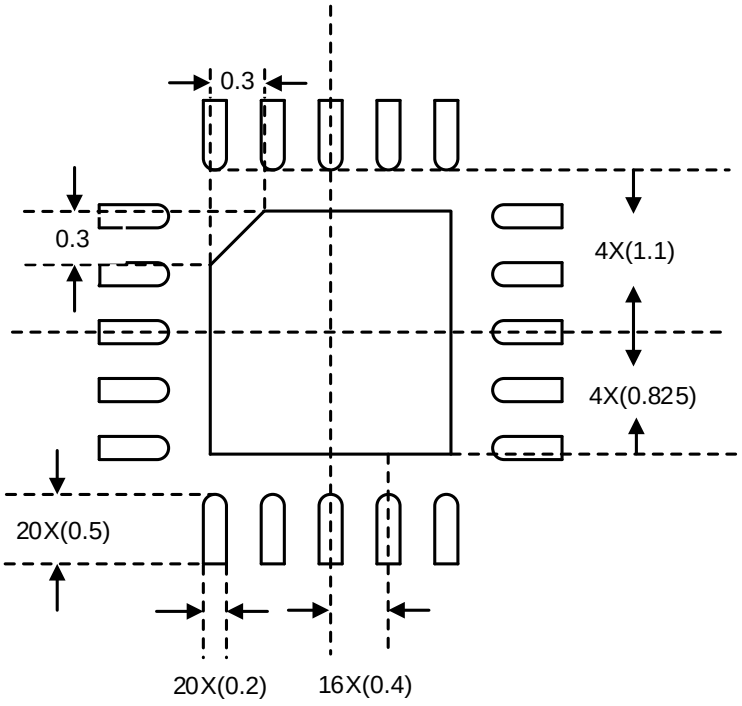
i. Material: polystyrene
ii. Flatness: maximum permissible 3mm
iii. All dimensions are in millimeters
iv. Surface resistivity: 10^5 to 10^{11} ohms/sq or less
v. All unmarked tolerance: ±0.5

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12 PACKAGE DESCRIPTION



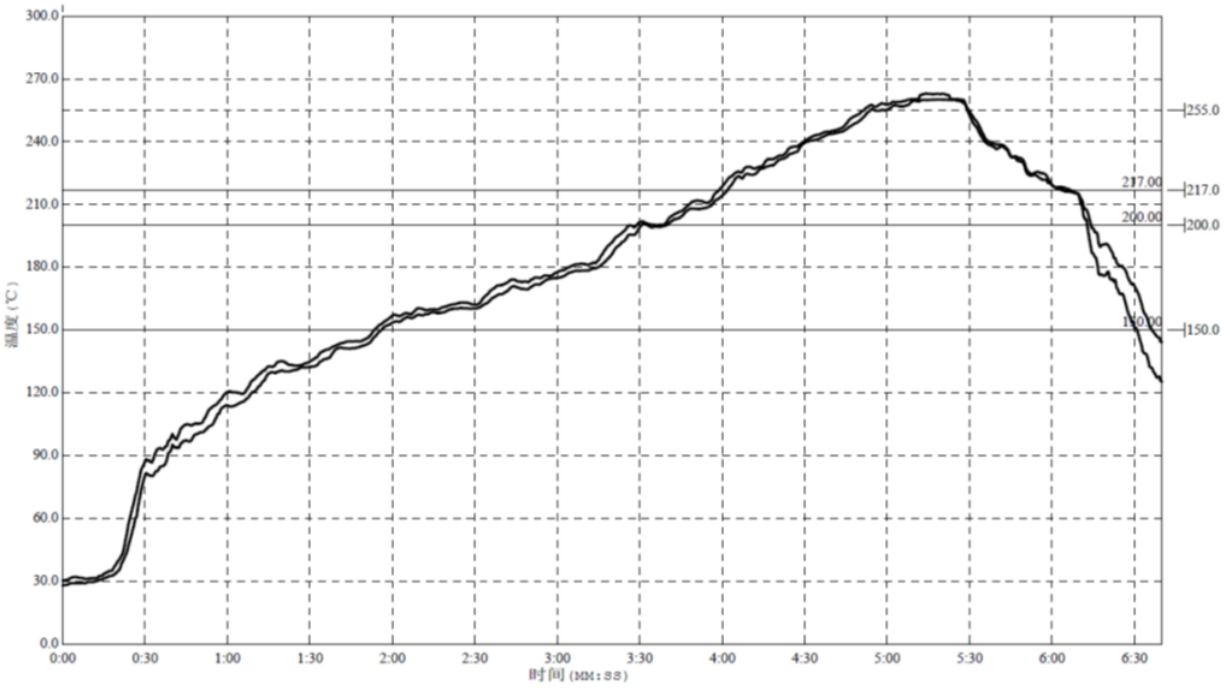
13 RECOMMENDED LAND PATTERN



TOP VIEW

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14 REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

Package Reflow Standard Profile

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW9163 adopted the Pb-Free assembly.

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15 REVISION HISTORY

Vision	Date	Change Record
V1.0	March 2015	Officially Released
V1.0.1	April 2015	Correct the package thickness
V1.0.2	March 2017	Update electrical characteristics and package thickness
V1.1	Nov. 2017	Remove the Chinese description Update the ordering information
V1.2	May. 2018	Update OSFR register description Update ASP example Update the electrical characteristics Update the reflow information

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