

Features

- High Performance, Low Power AVR[®] 8-Bit Microcontroller
- Advanced RISC Architecture
 - 123 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- High Endurance Non-volatile Memory Segments
 - 4K/8K Bytes of In-System Self-Programmable Flash Program Memory
 - 64/64 Bytes EEPROM
 - 256/512 Bytes Internal SRAM
 - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
 - Data Retention: 20 years at 85°C / 100 years at 25°C
 - Programming Lock for Software Security
- Peripheral Features
 - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
 - One 16-bit Timer/Counter with Prescaler, and Compare and Capture Modes
 - 6- or 8-channel 10-bit ADC
 - Master/Slave SPI Serial Interface
 - Byte-oriented 2-wire Serial Interface (Philips I²C Compatible)
 - Programmable Watchdog Timer with Separate On-Chip Oscillator
 - On-Chip Analog Comparator
 - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
 - debugWIRE On-Chip Debug System
 - In-System Programmable via SPI Port
 - Power-On Reset and Programmable Brown-Out Detection
 - Internal Calibrated Oscillator
 - External and Internal Interrupt Sources
 - Three Sleep Modes: Idle, ADC Noise Reduction and Power-Down
 - On-Chip Temperature Sensor
- I/O and Packages
 - 24 Programmable I/O Lines:
 - 28-pin PDIP
 - 28-pad QFN/MLF
 - 28 Programmable I/O Lines:
 - 32-lead TQFP
 - 32-pad QFN/MLF
 - 32-ball UFBGA
- Operating Voltage:
 - 1.8 – 5.5V
- Temperature Range:
 - -40°C to +85°C
- Speed Grade:
 - 0 – 4 MHz @ 1.8 – 5.5V
 - 0 – 8 MHz @ 2.7 – 5.5V
 - 0 – 12 MHz @ 4.5 – 5.5V
- Low Power Consumption
 - Active Mode: 1 MHz, 1.8V: 240 µA
 - Power-Down Mode: 0.1 µA at 1.8V



8-bit AVR[®] Microcontroller with 4/8K Bytes In-System Programmable Flash

ATtiny48/88

Preliminary

Summary

Rev. 8008FS-AVR-06/10



1. Pin Configurations

Figure 1-1. Pinout of ATtiny48/88

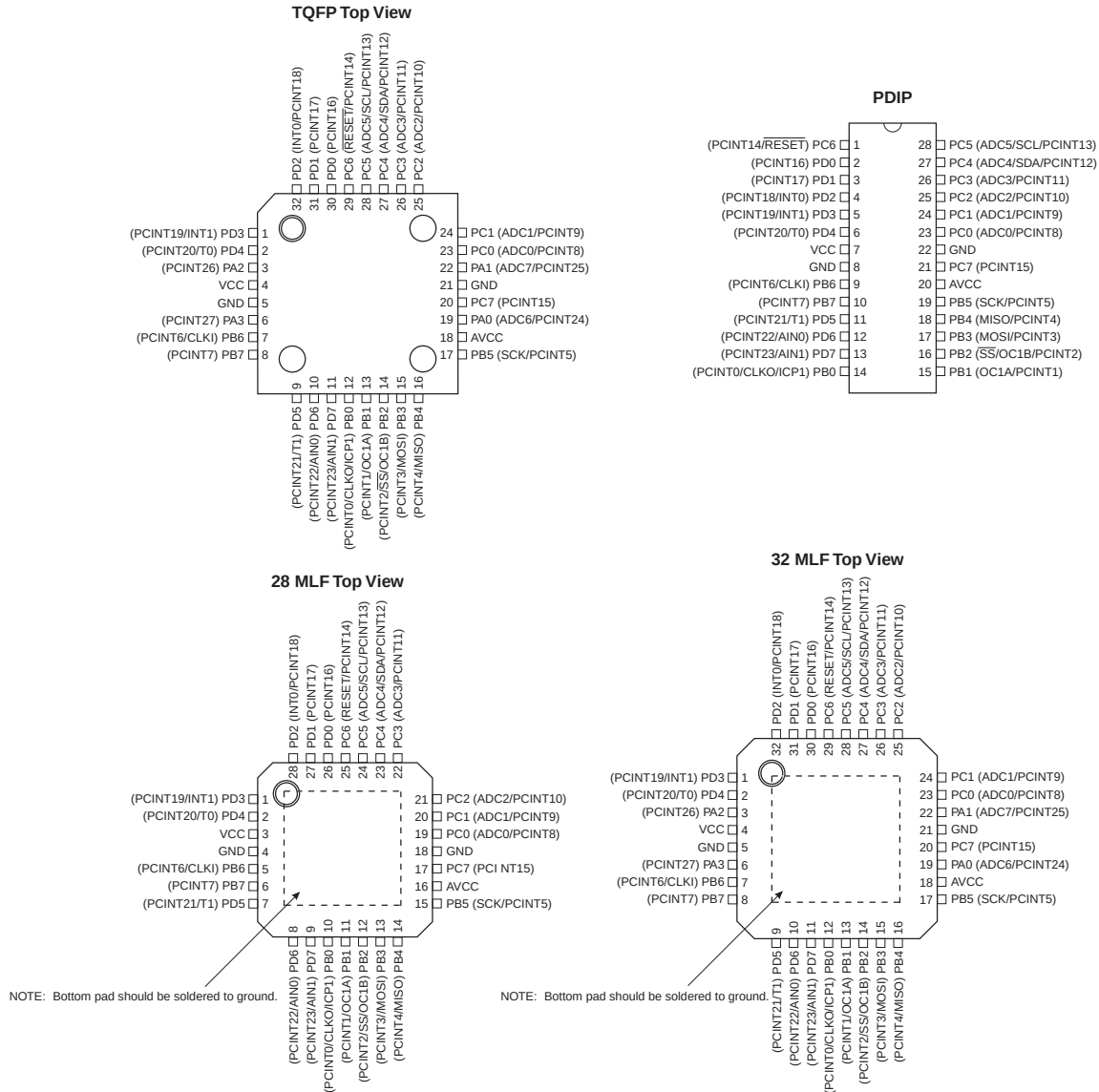


Table 1-1. 32UFBGA - Pinout ATtiny48/88

	1	2	3	4	5	6
A	PD2	PD1	PC6	PC4	PC2	PC1
B	PD3	PD4	PD0	PC5	PC3	PC0
C	GND	PA2			PA1	GND
D	VDD	PA3			PC7	PA0
E	PB6	PD6	PB0	PB2	AVDD	PB5
F	PB7	PD5	PD7	PB1	PB3	PB4

1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port A (PA3:0) (in 32-lead TQFP and 32-pad QFN/MLF packages, only)

Port A is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit) in 32-lead TQFP and 32-pad QFN/MLF package. The PA[3:0] output buffers have symmetrical drive characteristics with both sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.4 Port B (PB7:0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the internal clock operating circuit.

The various special features of Port B are elaborated in [“Alternate Functions of Port B” on page 67](#) and [“System Clock and Clock Options” on page 25](#).

1.1.5 Port C (PC7, PC5:0)

Port C is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC7 and PC[5:0] output buffers have symmetrical drive characteristics with both sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.6 PC6/RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a reset input. A low level on this pin for longer than the minimum pulse width will generate a reset, even if the clock is not running. The minimum pulse length is given in [Table 21-3 on page 207](#). Shorter pulses are not guaranteed to generate a reset.

The various special features of Port C are elaborated in [“Alternate Functions of Port C” on page 70](#).

1.1.7 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PD[7:4] output buffers have symmetrical drive characteristics with both sink and source capabilities, while the PD[3:0] output buffers have high sink capabilities. As inputs, Port D pins that are

externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The various special features of Port D are elaborated in [“Alternate Functions of Port D” on page 73](#).

1.1.8 AV_{CC}

AV_{CC} is the supply voltage pin for the A/D converter and a selection of I/O pins. This pin should be externally connected to V_{CC} even if the ADC is not used. If the ADC is used, it is recommended this pin is connected to V_{CC} through a low-pass filter, as described in [“Analog Noise Canceling Techniques” on page 169](#).

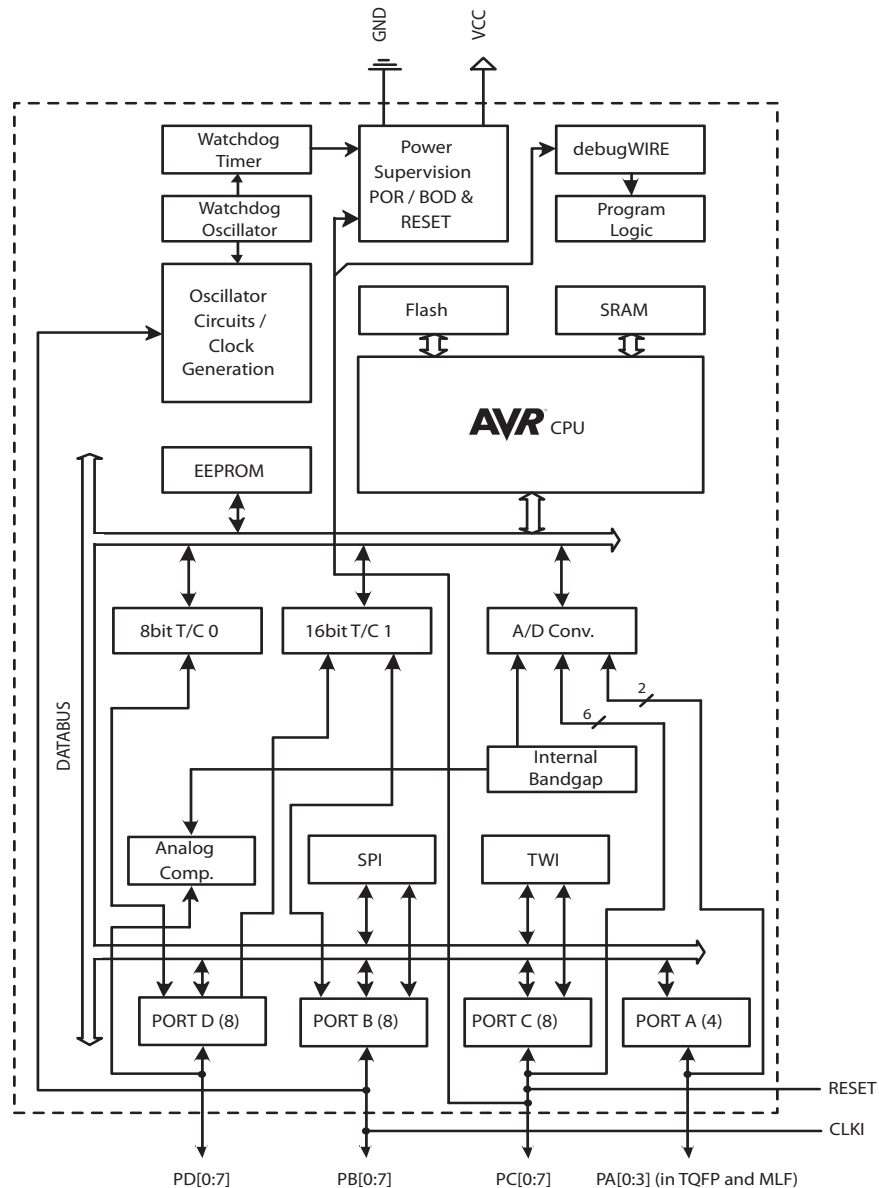
The following pins receive their supply voltage from AV_{CC} : PC7, PC[5:0] and (in 32-lead packages) PA[1:0]. All other I/O pins take their supply voltage from V_{CC} .

2. Overview

The ATtiny48/88 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny48/88 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny48/88 provides the following features: 4/8K bytes of In-System Programmable Flash, 64/64 bytes EEPROM, 256/512 bytes SRAM, 24 general purpose I/O lines (28 I/Os in 32-lead TQFP and 32-pad QFN/MLF packages), 32 general purpose working registers, two flexible Timer/Counters with compare modes, internal and external interrupts, a byte-oriented 2-wire serial interface, an SPI serial port, a 6-channel 10-bit ADC (8 channels in 32-lead TQFP and 32-pad QFN/MLF packages), a programmable Watchdog Timer with internal oscillator, and three software selectable power saving modes. Idle mode stops the CPU while allowing Timer/Counters, 2-wire serial interface, SPI port, and interrupt system to continue functioning. Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset. ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, and helps to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an on-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Flash memory. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny48/88 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny48/88 AVR is supported by a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators and evaluation kits.

2.2 Comparison Between ATtiny48 and ATtiny88

The ATtiny48 and ATtiny88 differ only in memory sizes. [Table 2-1](#) summarizes the different memory sizes for the two devices.

Table 2-1. Memory Size Summary

Device	Flash	EEPROM	RAM
ATtiny48	4K Bytes	64 Bytes	256 Bytes
ATtiny88	8K Bytes	64 Bytes	512 Bytes

3. General Information

3.1 Resources

A comprehensive set of development tools, application notes and datasheets are available for download at <http://www.atmel.com/avr>.

3.2 About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBR”, “SBRC”, “SBR”, and “CBR”.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.



4. Register Summary

[illegible]

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBE)	TWHSR	–	–	–	–	–	–	–	TWHS	157
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	–	157
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	154
(0xBB)	TWDR	2-wire Serial Interface Data Register								156
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	156
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	155
(0xB8)	TWBR	2-wire Serial Interface Bit Rate Register								154
(0xB7)	Reserved	–	–	–	–	–	–	–	–	
(0xB6)	Reserved	–	–	–	–	–	–	–	–	
(0xB5)	Reserved	–	–	–	–	–	–	–	–	
(0xB4)	Reserved	–	–	–	–	–	–	–	–	
(0xB3)	Reserved	–	–	–	–	–	–	–	–	
(0xB2)	Reserved	–	–	–	–	–	–	–	–	
(0xB1)	Reserved	–	–	–	–	–	–	–	–	
(0xB0)	Reserved	–	–	–	–	–	–	–	–	
(0xAF)	Reserved	–	–	–	–	–	–	–	–	
(0xAE)	Reserved	–	–	–	–	–	–	–	–	
(0xAD)	Reserved	–	–	–	–	–	–	–	–	
(0xAC)	Reserved	–	–	–	–	–	–	–	–	
(0xAB)	Reserved	–	–	–	–	–	–	–	–	
(0xAA)	Reserved	–	–	–	–	–	–	–	–	
(0xA9)	Reserved	–	–	–	–	–	–	–	–	
(0xA8)	Reserved	–	–	–	–	–	–	–	–	
(0xA7)	Reserved	–	–	–	–	–	–	–	–	
(0xA6)	Reserved	–	–	–	–	–	–	–	–	
(0xA5)	Reserved	–	–	–	–	–	–	–	–	
(0xA4)	Reserved	–	–	–	–	–	–	–	–	
(0xA3)	Reserved	–	–	–	–	–	–	–	–	
(0xA2)	Reserved	–	–	–	–	–	–	–	–	
(0xA1)	Reserved	–	–	–	–	–	–	–	–	
(0xA0)	Reserved	–	–	–	–	–	–	–	–	
(0x9F)	Reserved	–	–	–	–	–	–	–	–	
(0x9E)	Reserved	–	–	–	–	–	–	–	–	
(0x9D)	Reserved	–	–	–	–	–	–	–	–	
(0x9C)	Reserved	–	–	–	–	–	–	–	–	
(0x9B)	Reserved	–	–	–	–	–	–	–	–	
(0x9A)	Reserved	–	–	–	–	–	–	–	–	
(0x99)	Reserved	–	–	–	–	–	–	–	–	
(0x98)	Reserved	–	–	–	–	–	–	–	–	
(0x97)	Reserved	–	–	–	–	–	–	–	–	
(0x96)	Reserved	–	–	–	–	–	–	–	–	
(0x95)	Reserved	–	–	–	–	–	–	–	–	
(0x94)	Reserved	–	–	–	–	–	–	–	–	
(0x93)	Reserved	–	–	–	–	–	–	–	–	
(0x92)	Reserved	–	–	–	–	–	–	–	–	
(0x91)	Reserved	–	–	–	–	–	–	–	–	
(0x90)	Reserved	–	–	–	–	–	–	–	–	
(0x8F)	Reserved	–	–	–	–	–	–	–	–	
(0x8E)	Reserved	–	–	–	–	–	–	–	–	
(0x8D)	Reserved	–	–	–	–	–	–	–	–	
(0x8C)	Reserved	–	–	–	–	–	–	–	–	
(0x8B)	OCR1BH	Timer/Counter1 — Output Compare Register B High Byte								112
(0x8A)	OCR1BL	Timer/Counter1 — Output Compare Register B Low Byte								112
(0x89)	OCR1AH	Timer/Counter1 — Output Compare Register A High Byte								112
(0x88)	OCR1AL	Timer/Counter1 — Output Compare Register A Low Byte								112
(0x87)	ICR1H	Timer/Counter1 — Input Capture Register High Byte								112
(0x86)	ICR1L	Timer/Counter1 — Input Capture Register Low Byte								112
(0x85)	TCNT1H	Timer/Counter1 — Counter Register High Byte								111
(0x84)	TCNT1L	Timer/Counter1 — Counter Register Low Byte								111
(0x83)	Reserved	–	–	–	–	–	–	–	–	
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	111
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	110
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	108
(0x7F)	DIDR1	–	–	–	–	–	–	AIN1D	AIN0D	160
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	177
(0x7D)	Reserved	–	–	–	–	–	–	–	–	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7C)	ADMUX	–	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	173
(0x7B)	ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	159, 176
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	174
(0x79)	ADCH	ADC Data Register High byte								176
(0x78)	ADCL	ADC Data Register Low byte								176
(0x77)	Reserved	–	–	–	–	–	–	–	–	
(0x76)	Reserved	–	–	–	–	–	–	–	–	
(0x75)	Reserved	–	–	–	–	–	–	–	–	
(0x74)	Reserved	–	–	–	–	–	–	–	–	
(0x73)	Reserved	–	–	–	–	–	–	–	–	
(0x72)	Reserved	–	–	–	–	–	–	–	–	
(0x71)	Reserved	–	–	–	–	–	–	–	–	
(0x70)	Reserved	–	–	–	–	–	–	–	–	
(0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	112
(0x6E)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	85
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	56
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	56
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	57
(0x6A)	PCMSK3	–	–	–	–	PCINT27	PCINT26	PCINT25	PCINT24	57
(0x69)	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00	53
(0x68)	PCICR	–	–	–	–	PCIE3	PCIE2	PCIE1	PCIE0	55
(0x67)	Reserved	–	–	–	–	–	–	–	–	
(0x66)	OSCCAL	Oscillator Calibration Register								30
(0x65)	Reserved	–	–	–	–	–	–	–	–	
(0x64)	PRR	PRTWI	–	PRTIM0	–	PRTIM1	PRSPI	–	PRADC	37
(0x63)	Reserved	–	–	–	–	–	–	–	–	
(0x62)	Reserved	–	–	–	–	–	–	–	–	
(0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	31
(0x60)	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	47
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	9
0x3E (0x5E)	SPH	–	–	–	–	–	–	SP9	SP8	12
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	12
0x3C (0x5C)	Reserved	–	–	–	–	–	–	–	–	
0x3B (0x5B)	Reserved	–	–	–	–	–	–	–	–	
0x3A (0x5A)	Reserved	–	–	–	–	–	–	–	–	
0x39 (0x59)	Reserved	–	–	–	–	–	–	–	–	
0x38 (0x58)	Reserved	–	–	–	–	–	–	–	–	
0x37 (0x57)	SPMCSR	–	RWWBSB	–	CTPB	RFLB	PGWRT	PGERS	SELFPRGEN	185
0x36 (0x56)	Reserved	–	–	–	–	–	–	–	–	
0x35 (0x55)	MCUCR	–	BODS	BODSE	PUD	–	–	–	–	37, 75
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	47
0x33 (0x53)	SMCR	–	–	–	–	–	SM1	SM0	SE	36
0x32 (0x52)	Reserved	–	–	–	–	–	–	–	–	
0x31 (0x51)	DWDR	debugWire Data Register								179
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	159
0x2F (0x4F)	Reserved	–	–	–	–	–	–	–	–	
0x2E (0x4E)	SPDR	SPI Data Register								126
0x2D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	125
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	124
0x2B (0x4B)	GPOR2	General Purpose I/O Register 2								24
0x2A (0x4A)	GPOR1	General Purpose I/O Register 1								24
0x29 (0x49)	Reserved	–	–	–	–	–	–	–	–	
0x28 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B								85
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								84
0x26 (0x46)	TCNT0	Timer/Counter0 (8-bit)								84
0x25 (0x45)	TCCR0A	–	–	–	–	CTC0	CS02	CS01	CS00	83
0x24 (0x44)	Reserved	–	–	–	–	–	–	–	–	
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	–	PSRSYNC	116
0x22 (0x42)	Reserved	–	–	–	–	–	–	–	–	
0x21 (0x41)	EEARL	EEPROM Address Register Low Byte								22
0x20 (0x40)	EEDR	EEPROM Data Register								22
0x1F (0x3F)	EEDR	–	–	EEP01	EEP00	EERIE	EEMPE	EEPE	EERE	22
0x1E (0x3E)	GPOR0	General Purpose I/O Register 0								24
0x1D (0x3D)	EIMSK	–	–	–	–	–	–	INT1	INT0	54
0x1C (0x3C)	EIFR	–	–	–	–	–	–	INTF1	INTF0	54
0x1B (0x3B)	PCIFR	–	–	–	–	PCIF3	PCIF2	PCIF1	PCIF0	55

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
0x19 (0x39)	Reserved	–	–	–	–	–	–	–	–	
0x18 (0x38)	Reserved	–	–	–	–	–	–	–	–	
0x17 (0x37)	Reserved	–	–	–	–	–	–	–	–	
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	113
0x15 (0x35)	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0	85
0x14 (0x34)	Reserved	–	–	–	–	–	–	–	–	
0x13 (0x33)	Reserved	–	–	–	–	–	–	–	–	
0x12 (0x32)	PORTCR	BBMD	BBMC	BBMB	BBMA	PUDD	PUDC	PUDB	PUDA	75
0x11 (0x31)	Reserved	–	–	–	–	–	–	–	–	
0x10 (0x30)	Reserved	–	–	–	–	–	–	–	–	
0x0F (0x2F)	Reserved	–	–	–	–	–	–	–	–	
0x0E (0x2E)	PORTA	–	–	–	–	PORTA3	PORTA2	PORTA1	PORTA0	76
0x0D (0x2D)	DDRA	–	–	–	–	DDA3	DDA2	DDA1	DDA0	76
0x0C (0x2C)	PINA	–	–	–	–	PINA3	PINA2	PINA1	PINA0	76
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	77
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	77
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	77
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	76
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	76
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	77
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	76
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	76
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	76
0x02 (0x22)	Reserved	–	–	–	–	–	–	–	–	
0x01 (0x21)	Reserved	–	–	–	–	–	–	–	–	
0x00 (0x20)	Reserved	–	–	–	–	–	–	–	–	

- Note:
- For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 - I/O Registers within the address range 0x00 – 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 - Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 - When using the I/O specific commands IN and OUT, the I/O addresses 0x00 – 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATtiny48/88 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 – 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if $(V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if $(I = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if $(I = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow.	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(Z) \leftarrow R1:R0$	None	-
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATtiny48

Speed (MHz)	Power Supply	Ordering Code ⁽¹⁾	Package ⁽²⁾	Operational Range
12	1.8 – 5.5	ATtiny48-MMU ATtiny48-MMH ATtiny48-MMHR ATtiny48-PU ATtiny48-AU ATtiny48-AUR ATtiny48-CCU ATtiny48-CCUR ATtiny48-MU ATtiny48-MUR	28M1 28M1 28M1 28P3 32A 32A 32CC1 32CC1 32M1-A 32M1-A	Industrial (-40°C to +85°C) ⁽³⁾

Notes: 1. Code indicators:

- H: NiPdAu lead finish
- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
32CC1	32-ball (6 x 6 Array), 0.50 mm Pitch, 4 x 4 x 0.6 mm, Ultra Thin, Fine-Pitch Ball Grid Array Package (UFBGA)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.2 ATtiny88

Speed (MHz)	Power Supply	Ordering Code ⁽¹⁾	Package ⁽²⁾	Operational Range
12	1.8 – 5.5	ATtiny88-MMU ATtiny88-MMH ATtiny88-MMHR ATtiny88-PU ATtiny88-AU ATtiny88-AUR ATtiny88-CCU ATtiny88-CCUR ATtiny88-MU ATtiny88-MUR	28M1 28M1 28M1 28P3 32A 32A 32CC1 32CC1 32M1-A 32M1-A	Industrial (-40°C to +85°C) ⁽³⁾

Notes: 1. Code indicators:

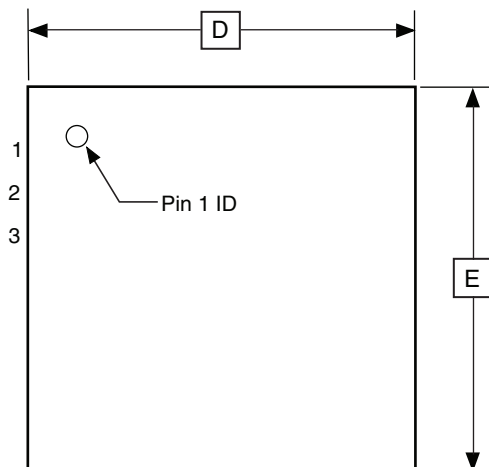
- H: NiPdAu lead finish
- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

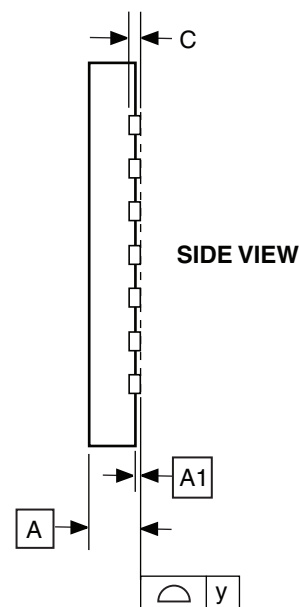
Package Type	
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
32CC1	32-ball (6 x 6 Array), 0.50 mm Pitch, 4 x 4 x 0.6 mm, Ultra Thin, Fine-Pitch Ball Grid Array Package (UFBGA)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7. Packaging Information

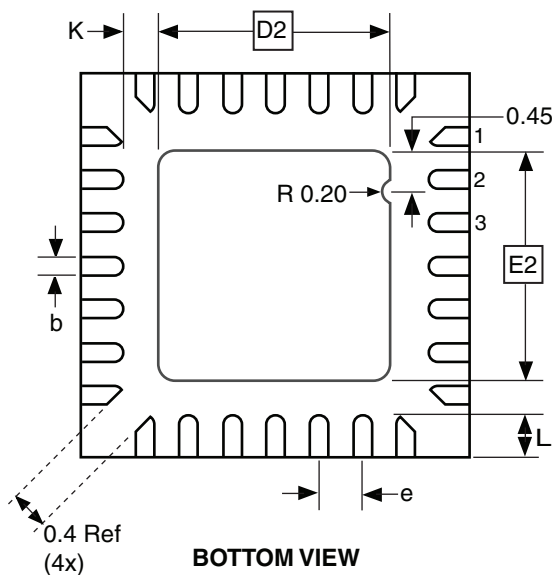
7.1 28M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: The terminal #1 ID is a Laser-marked Feature.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.17	0.22	0.27	
C	0.20 REF			
D	3.95	4.00	4.05	
D2	2.35	2.40	2.45	
E	3.95	4.00	4.05	
E2	2.35	2.40	2.45	
e	0.45			
L	0.35	0.40	0.45	
y	0.00	—	0.08	
K	0.20	—	—	

10/24/08



Package Drawing Contact:
packagedrawings@atmel.com

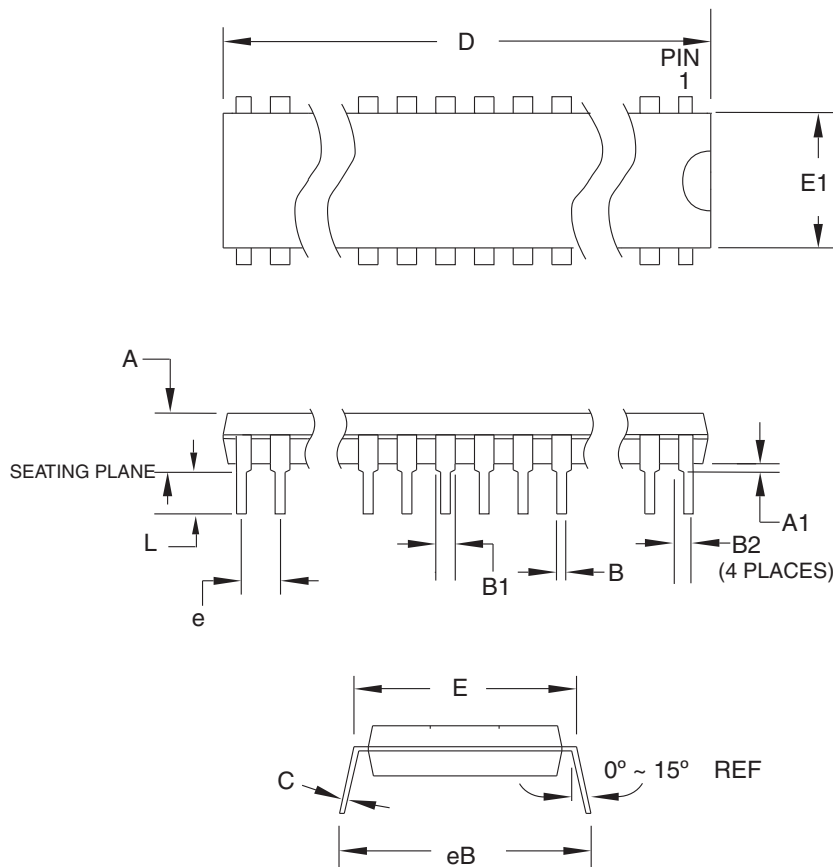
TITLE
28M1, 28-pad, 4 x 4 x 1.0 mm Body, Lead Pitch 0.45 mm,
2.4 x 2.4 mm Exposed Pad, Thermally Enhanced
Plastic Very Thin Quad Flat No Lead Package (VQFN)

GPC
ZBV

DRAWING NO.
28M1

REV.
B

7.2 28P3



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.5724	
A1	0.508	—	—	
D	34.544	—	34.798	Note 1
E	7.620	—	8.255	
E1	7.112	—	7.493	Note 1
B	0.381	—	0.533	
B1	1.143	—	1.397	
B2	0.762	—	1.143	
L	3.175	—	3.429	
C	0.203	—	0.356	
eB	—	—	10.160	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

28P3, 28-lead (0.300"/7.62 mm Wide) Plastic Dual
Inline Package (PDIP)

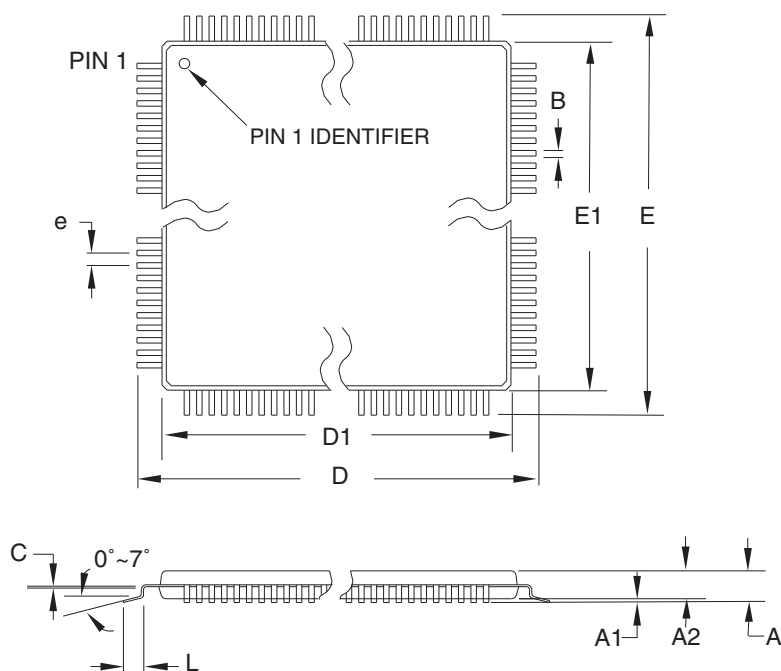
DRAWING NO.

28P3

REV.

B

7.3 32A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	—	0.45	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32A, 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness,
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

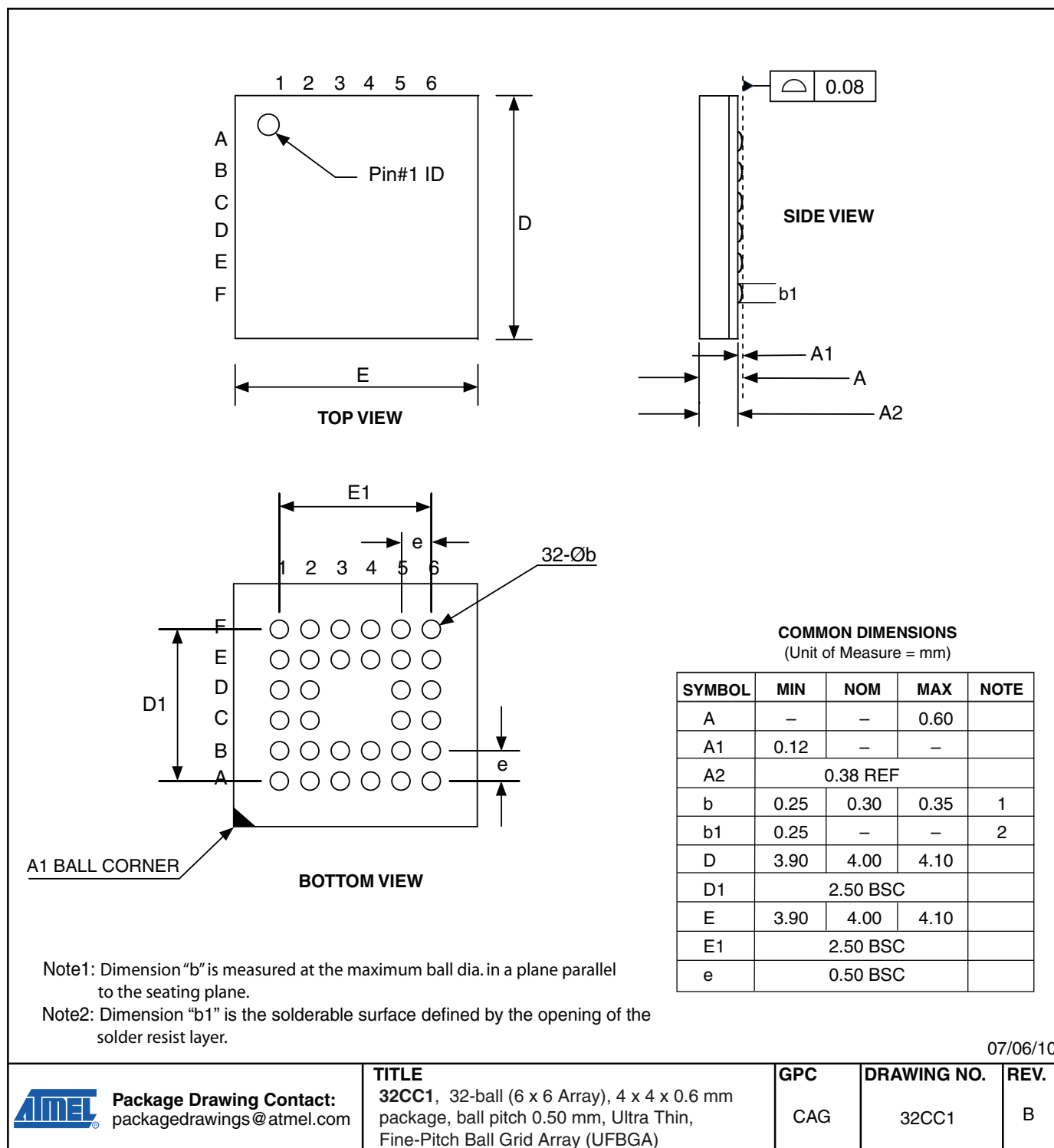
DRAWING NO.

32A

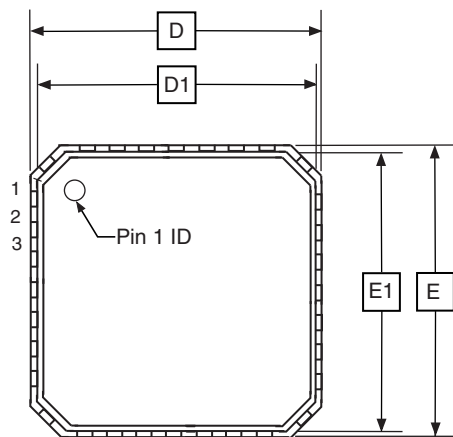
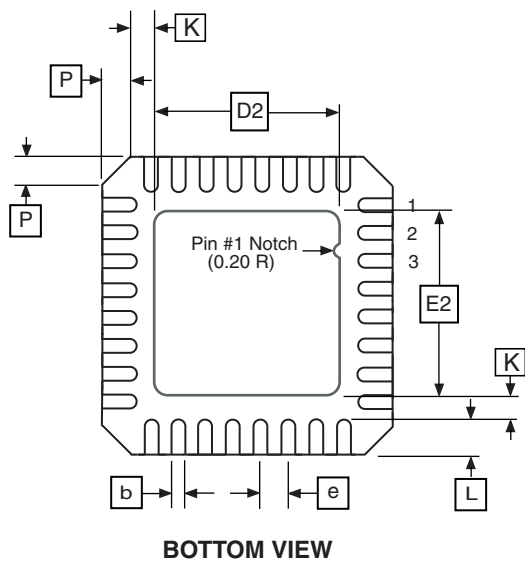
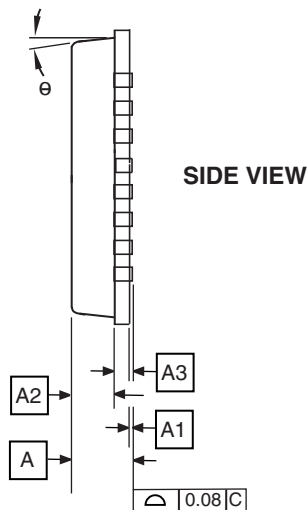
REV.

B

7.4 32CC1



7.5 32M1-A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A2	—	0.65	1.00	
A3	0.20 REF			
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e	0.50 BSC			
L	0.30	0.40	0.50	
P	—	—	0.60	
θ	—	—	12°	
K	0.20	—	—	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32M1-A, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm,
3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

32M1-A

REV.

E

8. Errata

8.1 ATtiny48

8.1.1 Rev. C

No known errata.

8.1.2 Rev. B

Not sampled.

8.1.3 Rev. A

Not sampled.

8.2 ATtiny88

8.2.1 Rev. C

No known errata.

8.2.2 Rev. B

No known errata.

8.2.3 Rev. A

Not sampled.

9. Datasheet Revision History

Please note that page references in this section refer to the current revision of this document.

9.1 Rev. 8008F - 06/10

1. Updated notes 1 and 10 in table in [Section 21.2 “DC Characteristics” on page 204](#).
2. Updated package drawing in [Section 7.4 “32CC1” on page 19](#).
3. Updated bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0].

9.2 Rev. 8008E - 05/10

1. [Section 4. “Register Summary” on page 8](#), added SPH at address 0x3E.
2. [Section 7.1 “28M1” on page 16](#) updated with correct package drawing.

9.3 Rev. 8008D - 03/10

1. Separated Typical Characteristic plots, added [Section 22.2 “ATtiny88” on page 247](#).
2. Updated:
 - [Section 1.1 “Pin Descriptions” on page 3](#), Port D, adjusted texts ‘sink and source’ and ‘high sink’.
 - [Table 6-3 on page 28](#) adjusted, to fix TBD.
 - [Section 6.4 “128 kHz Internal Oscillator” on page 28](#) adjusted, to fix TBD.
 - [Section 8.4 “Watchdog Timer” on page 43](#), updated.
 - [Section 21.2 “DC Characteristics” on page 204](#), updated TBD in notes 5 and 8.
3. Added:
 - UFBGA package (32CC1) in, [“Features” on page 1](#), [“Pin Configurations” on page 2](#), [Section 6. “Ordering Information” on page 14](#), and [Section 7. “Packaging Information” on page 16](#)
 - Addresses in all Register Desc. tables, with cross-references to Register Summary
 - Tape and reel in [Section 6. “Ordering Information” on page 14](#)

9.4 Rev. 8008C - 03/09

1. Updated sections:
 - [“Features” on page 1](#)
 - [“Reset and Interrupt Handling” on page 13](#)
 - [“EECR – EEPROM Control Register” on page 22](#)
 - [“Features” on page 127](#)
 - [“Bit Rate Generator Unit” on page 133](#)
 - [“TWBR – TWI Bit Rate Register” on page 154](#)
 - [“TWHSR – TWI High Speed Register” on page 157](#)
 - [“Analog Comparator” on page 158](#)
 - [“Overview” on page 161](#)
 - [“Operation” on page 162](#)
 - [“Starting a Conversion” on page 163](#)

- “Programming the Lock Bits” on page 198
- “Absolute Maximum Ratings*” on page 204
- “DC Characteristics” on page 204
- “Speed” on page 206
- “Register Summary” on page 8
- 2. Added sections
 - “High-Speed Two-Wire Interface Clock – $\text{clk}_{\text{TWIHS}}$ ” on page 26
 - “Analog Comparator Characteristics” on page 208
- 3. Updated Figure 6-1 on page 25.
- 4. Updated order codes on page 14 and page 15 to reflect changes in leadframe composition.

9.5 Rev. 8008B - 06/08

1. Updated introduction of “I/O-Ports” on page 58.
2. Updated “DC Characteristics” on page 204.
3. Added “Typical Characteristics” on page 218.

9.6 Rev. 8008A - 06/08

1. Initial revision.



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