

Appendix A – ATtiny13A Specification at 105°C

This document contains information specific to devices operating at temperatures up to 105°C. Only deviations are covered in this appendix, all other information can be found in the complete datasheet. The complete datasheet can be found at www.atmel.com.



8-bit AVR[®]
Microcontroller
with 1K Bytes
In-System
Programmable
Flash

ATtiny13A

Appendix A

Rev. 8126E-Appendix A-AVR-08/11



1. Electrical Characteristics

1.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-0.5V to $V_{CC}+0.5V$
Voltage on $\overline{\text{RESET}}$ with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.2 DC Characteristics

Table 1-1. DC Characteristics, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage, Any Pin as I/O	$V_{CC} = 1.8 - 2.4V$	-0.5		$0.2V_{CC}^{(1)}$	V
		$V_{CC} = 2.4 - 5.5V$	-0.5		$0.3V_{CC}^{(1)}$	V
	Input Low Voltage, $\overline{\text{RESET}}$ Pin as Reset ⁽²⁾	$V_{CC} = 1.8 - 5.5V$	-0.5		$0.2V_{CC}^{(1)}$	V
V_{IH}	Input High Voltage, Any Pin as I/O	$V_{CC} = 1.8 - 2.4V$	$0.7V_{CC}^{(3)}$		$V_{CC} + 0.5$	V
		$V_{CC} = 2.4 - 5.5V$	$0.6V_{CC}^{(3)}$		$V_{CC} + 0.5$	V
	Input High Voltage, $\overline{\text{RESET}}$ Pin as Reset ⁽²⁾	$V_{CC} = 1.8 - 5.5V$	$0.9V_{CC}^{(3)}$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage, Pins PB0 and PB1 ⁽⁴⁾	$I_{OL} = 20 \text{ mA}, V_{CC} = 5V$			0.8	V
		$I_{OL} = 10 \text{ mA}, V_{CC} = 3V$			0.6	V
	Output Low Voltage, Pins PB2, PB3 and PB4 ⁽⁴⁾	$I_{OL} = 10 \text{ mA}, V_{CC} = 5V$			0.8	V
		$I_{OL} = 5 \text{ mA}, V_{CC} = 3V$			0.6	V
V_{OH}	Output High Voltage, Pins PB0 and PB1 ⁽⁵⁾	$I_{OH} = -20 \text{ mA}, V_{CC} = 5V$	4.0			V
		$I_{OH} = -10 \text{ mA}, V_{CC} = 3V$	2.3			V
	Output High Voltage, Pins PB2, PB3 and PB4 ⁽⁵⁾	$I_{OH} = -10 \text{ mA}, V_{CC} = 5V$	4.2			V
		$I_{OH} = -5 \text{ mA}, V_{CC} = 3V$	2.5			V
I_{LIL}	Input Leakage Current I/O Pin	$V_{CC} = 5.5V$, pin low	-1		1	μA
I_{LIH}	Input Leakage Current I/O Pin	$V_{CC} = 5.5V$, pin high	-1		1	μA
R_{PU}	Pull-Up Resistor, I/O Pin	$V_{CC} = 5.5V$, input low	20		50	$k\Omega$
	Pull-Up Resistor, Reset Pin	$V_{CC} = 5.5V$, input low	30		80	$k\Omega$

Table 1-1. DC Characteristics, $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Supply Current, Active Mode ⁽⁶⁾	$f = 1\text{MHz}$, $V_{CC} = 2\text{V}$		0.2	0.35	mA
		$f = 4\text{MHz}$, $V_{CC} = 3\text{V}$		1.2	1.8	mA
		$f = 8\text{MHz}$, $V_{CC} = 5\text{V}$		3.6	6	mA
	Supply Current, Idle Mode	$f = 1\text{MHz}$, $V_{CC} = 2\text{V}$		0.03	0.2	mA
		$f = 4\text{MHz}$, $V_{CC} = 3\text{V}$		0.2	1	mA
		$f = 8\text{MHz}$, $V_{CC} = 5\text{V}$		0.7	3	mA
	Supply Current, Power-Down Mode	WDT enabled, $V_{CC} = 3\text{V}$		3.9	10	μA
		WDT disabled, $V_{CC} = 3\text{V}$		0.15	2	μA

- Notes:
1. “Max” means the highest value where the pin is guaranteed to be read as low.
 2. Not tested in production.
 3. “Min” means the lowest value where the pin is guaranteed to be read as high.
 4. Although each I/O port can under non-transient, steady state conditions sink more than the test conditions, the sum of all I_{OL} (for all ports) should not exceed 60 mA. If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
 5. Although each I/O port can under non-transient, steady state conditions source more than the test conditions, the sum of all I_{OH} (for all ports) should not exceed 60 mA. If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
 6. Measured with all I/O modules turned off (PRR = 0xFF).

1.3 Clock Characteristics

1.3.1 Accuracy of Calibrated Internal Oscillator

It is possible to manually calibrate the internal oscillator to be more accurate than default factory calibration. Note that the oscillator frequency depends on temperature and voltage. Voltage and temperature characteristics can be found in [Figure 2-53 on page 32](#), [Figure 2-54 on page 33](#), [Figure 2-55 on page 33](#), and in [Figure 2-56 on page 34](#).

Table 1-2. Calibration Accuracy of Internal Oscillator

Calibration Method	Target Frequency	V_{CC}	Temperature	Accuracy at given Voltage & Temperature ⁽¹⁾
Factory Calibration	4.8 / 9.6 MHz	3V	25°C	$\pm 10\%$
User Calibration	Fixed frequency within: 4 – 5 MHz / 8 – 10 MHz	Fixed voltage within: 1.8V – 5.5V	Fixed temperature within: -40°C to +105°C	$\pm 2\%$

- Notes:
1. Accuracy of oscillator frequency at calibration point (fixed temperature and fixed voltage).

1.4 System and Reset Characteristics

1.4.1 Enhanced Power-On Reset

Table 1-3. Characteristics of Enhanced Power-On Reset. $T_A = -40$ to $+105^\circ\text{C}$

Symbol	Parameter	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Units
V_{POR}	Release threshold of power-on reset ⁽²⁾	1.1	1.4	1.6	V
V_{POA}	Activation threshold of power-on reset ⁽³⁾	0.6	1.3	1.6	V
SR_{ON}	Power-On Slope Rate	0.01			V/ms

Note: 1. Values are guidelines only.
 2. Threshold where device is released from reset when voltage is rising.
 3. The Power-on Reset will not work unless the supply voltage has been below V_{POA} .

1.5 ADC Characteristics

Table 1-4. ADC Characteristics, Single Ended Channels. $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution				10	Bits
	Absolute accuracy (Including INL, DNL, and Quantization, Gain and Offset Errors)	$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200 kHz		3		LSB
		$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 1 MHz		4		LSB
		$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200 kHz, Noise Reduction Mode		2.5		LSB
		$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 1 MHz, Noise Reduction Mode		3.5		LSB
	Integral Non-Linearity (INL) (Accuracy after Offset and Gain Calibration)	$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200 kHz		1		LSB
	Differential Non-linearity (DNL)	$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200 kHz		0.5		LSB
	Gain Error	$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200 kHz		3.5		LSB
	Offset Error	$V_{REF} = 4V$, $V_{CC} = 4V$, ADC clock = 200 kHz		2.5		LSB
	Conversion Time	Free Running Conversion	13		260	μs
	Clock Frequency		50		1000	kHz
V_{IN}	Input Voltage		GND		V_{REF}	V
	Input Bandwidth			38.5		kHz
V_{INT}	Internal Voltage Reference		1.0	1.1	1.2	V
R_{AIN}	Analog Input Resistance			100		$M\Omega$

1.6 Analog Comparator Characteristics

Table 1-5. Analog Comparator Characteristics, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{AIO}	Input Offset Voltage	$V_{CC} = 5V, V_{IN} = V_{CC} / 2$		< 10	40	mV
I_{LAC}	Input Leakage Current	$V_{CC} = 5V, V_{IN} = V_{CC} / 2$	-50		50	nA
t_{APD}	Analog Propagation Delay (from saturation to slight overdrive)	$V_{CC} = 2.7V$		750		ns
		$V_{CC} = 4.0V$		500		
	Analog Propagation Delay (large step change)	$V_{CC} = 2.7V$		100		
		$V_{CC} = 4.0V$		75		
t_{DPD}	Digital Propagation Delay	$V_{CC} = 1.8V - 5.5$		1	2	CLK

Note: All parameters are based on simulation results.

1.7 Serial Programming Characteristics

Table 1-6. Serial Programming Characteristics, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	$V_{CC} = 1.8 - 5.5V$	0		1	MHz
t_{CLCL}	Oscillator Period		1000			ns
$1/t_{CLCL}$	Oscillator Frequency	$V_{CC} = 2.7 - 5.5V$	0		9.6	MHz
t_{CLCL}	Oscillator Period		104			ns
$1/t_{CLCL}$	Oscillator Frequency	$V_{CC} = 4.5 - 5.5V$	0		20	MHz
t_{CLCL}	Oscillator Period		50			ns
t_{SHSL}	SCK Pulse Width High	$V_{CC} = 1.8 - 5.5V$	$2 t_{CLCL}^{(1)}$			ns
t_{SLSH}	SCK Pulse Width Low		$2 t_{CLCL}^{(1)}$			ns
t_{OVSH}	MOSI Setup to SCK High		t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High		$2 t_{CLCL}$			ns

Note: 1. $2 t_{CLCL}$ for $f_{ck} < 12 \text{ MHz}$, $3 t_{CLCL}$ for $f_{ck} \geq 12 \text{ MHz}$

2. Typical Characteristics

The data contained in this section is largely based on simulations and characterization of similar devices in the same process and design methods. Thus, the data should be treated as indications of how the part will behave.

The following charts show typical behavior. These figures are not tested during manufacturing. During characterisation devices are operated at frequencies higher than test limits but they are not guaranteed to function properly at frequencies higher than the ordering code indicates.

All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. Current consumption is a function of several factors such as operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

A sine wave generator with rail-to-rail output is used as clock source but current consumption in Power-Down mode is independent of clock selection. The difference between current consumption in Power-Down mode with Watchdog Timer enabled and Power-Down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

The current drawn from pins with a capacitive load may be estimated (for one pin) as follows:

$$I_{CP} \approx V_{CC} \times C_L \times f_{SW}$$

where V_{CC} = operating voltage, C_L = load capacitance and f_{SW} = average switching frequency of I/O pin.

2.1 Current Consumption in Active Mode

Figure 2-1. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 9.6 MHz)

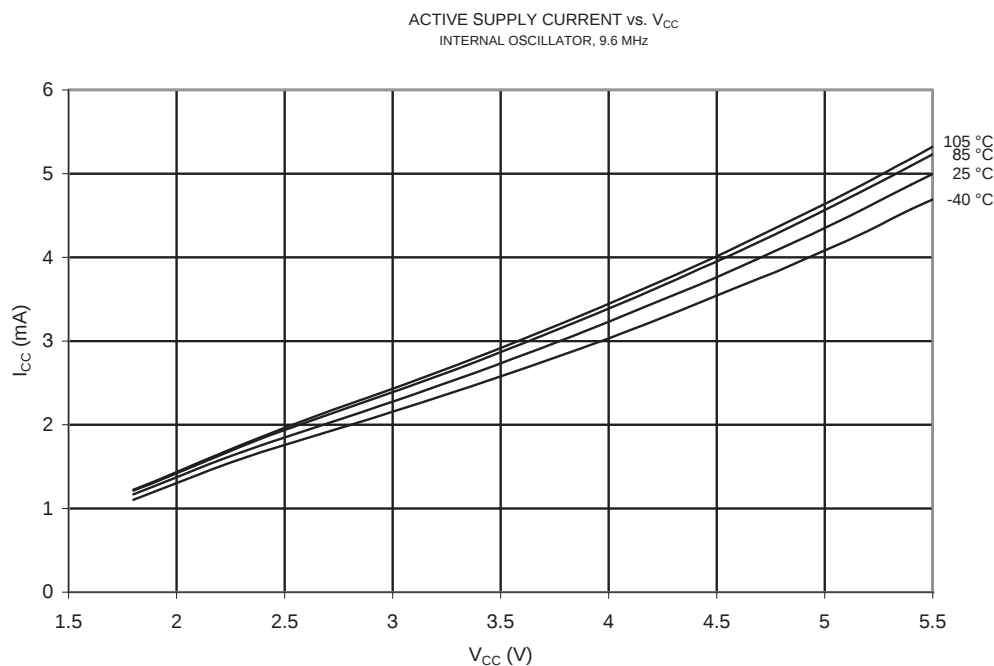


Figure 2-2. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 4.8 MHz)

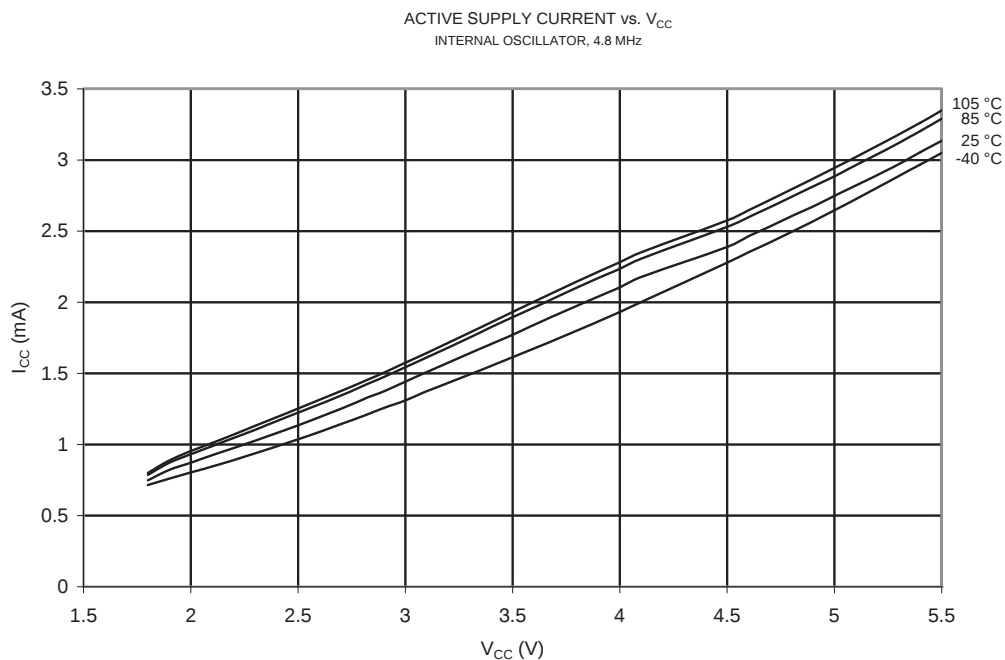


Figure 2-3. Active Supply Current vs. V_{CC} (Internal WDT Oscillator, 128 kHz)

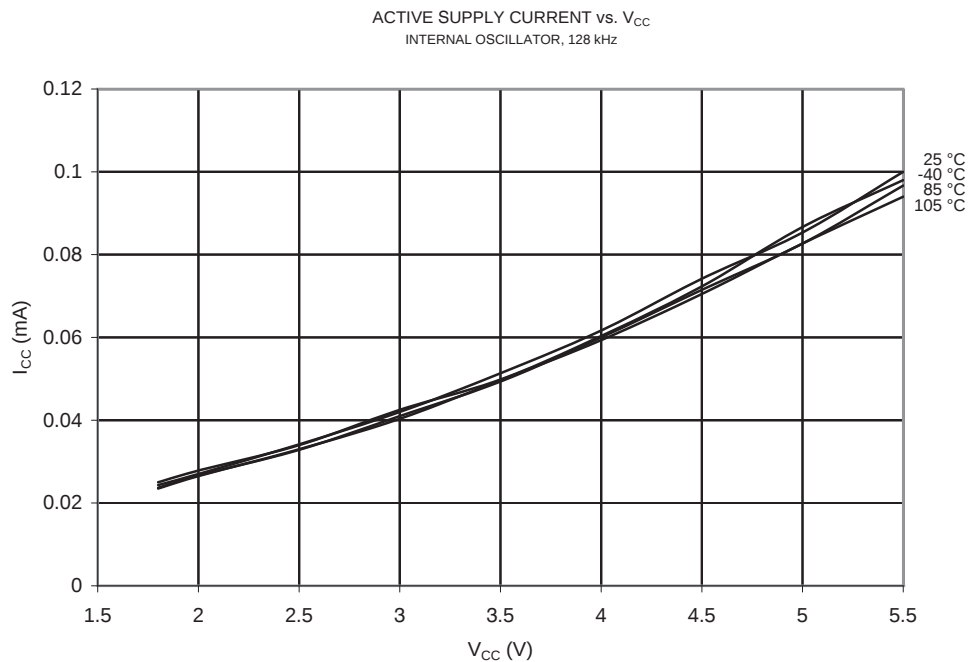
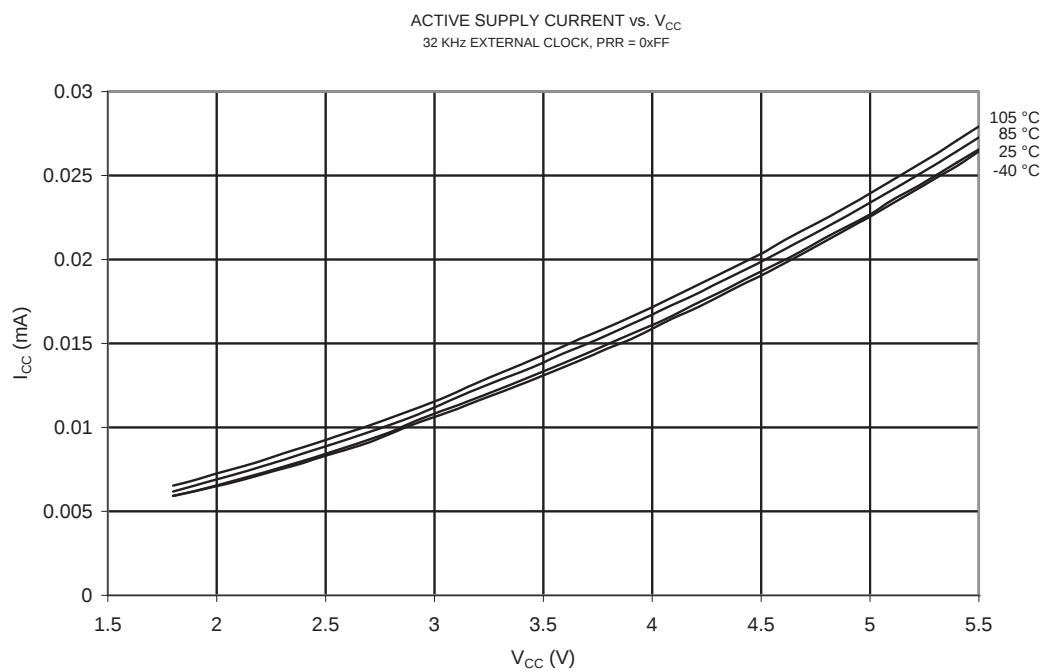


Figure 2-4. Active Supply Current vs. V_{CC} (32 kHz External Clock)



2.2 Current Consumption in Idle Mode

Figure 2-5. Idle Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 9.6 MHz)

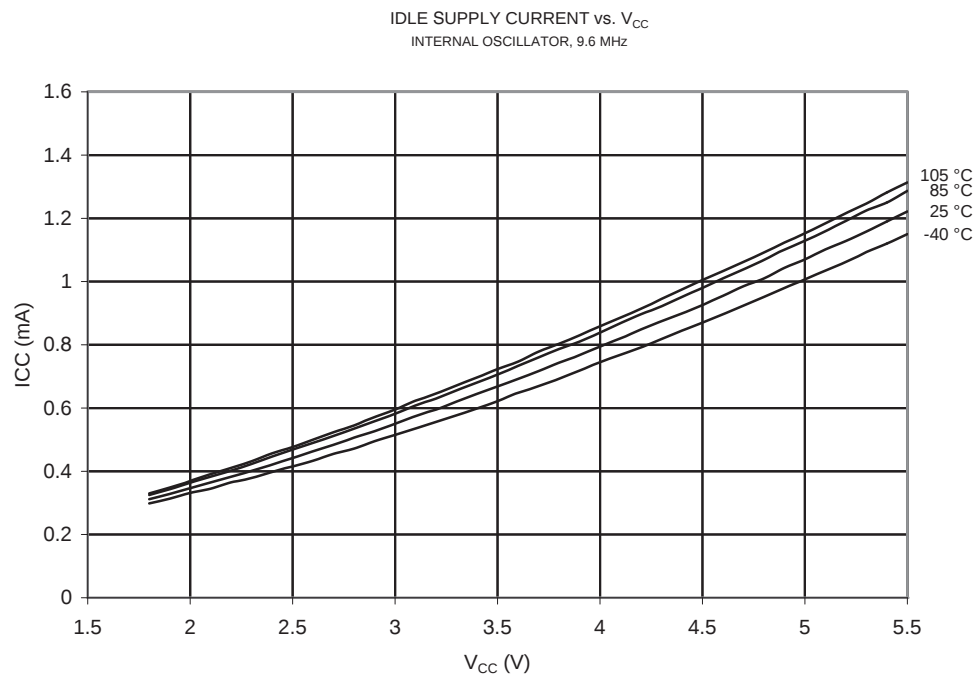


Figure 2-6. Idle Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 4.8 MHz)

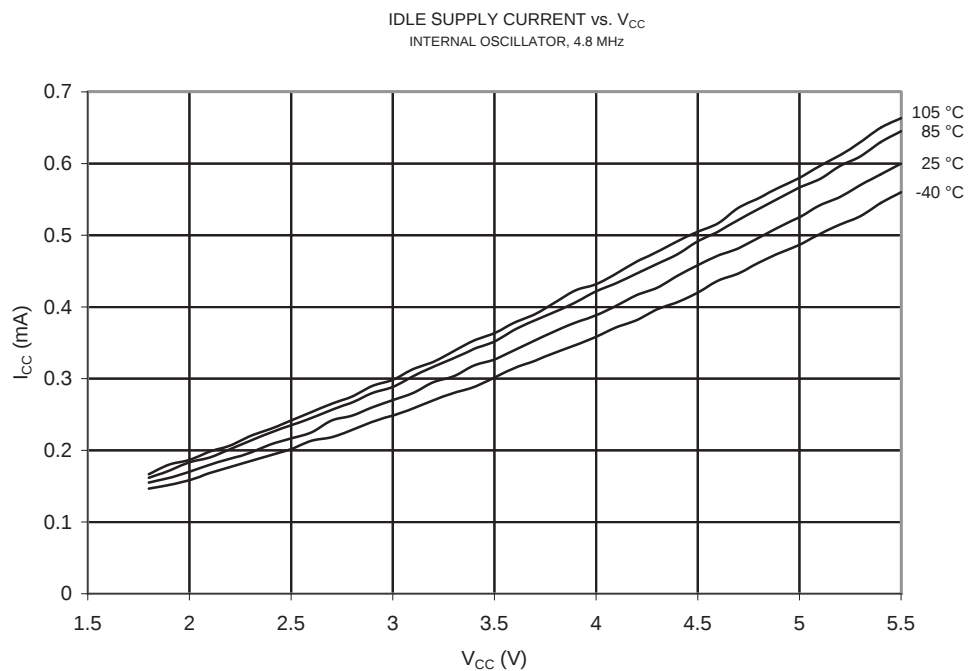


Figure 2-7. Idle Supply Current vs. V_{CC} (Internal Oscillator, 128 kHz)

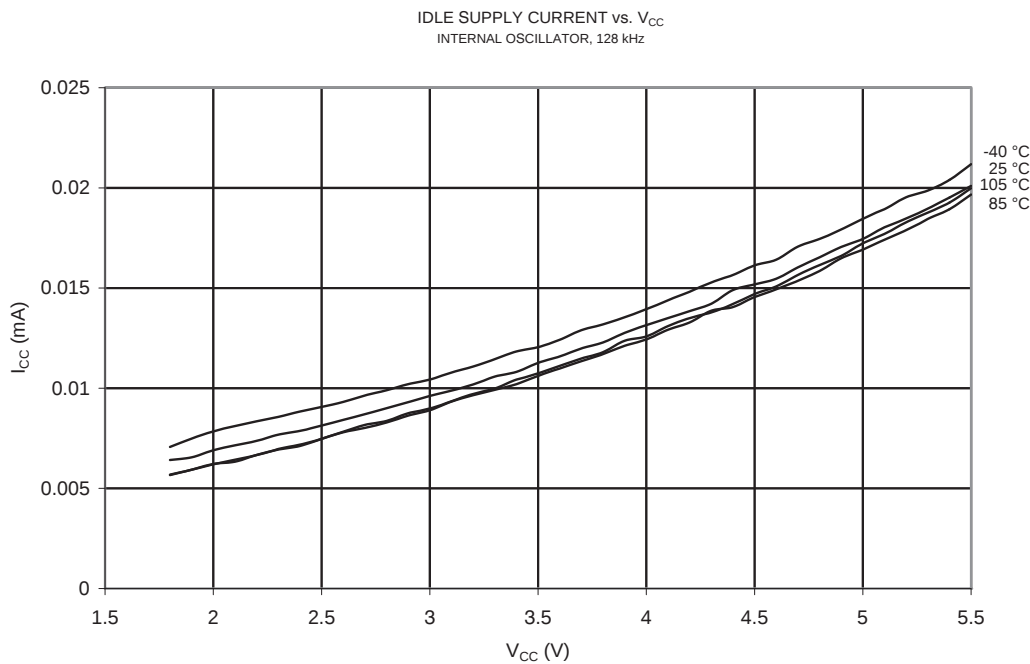
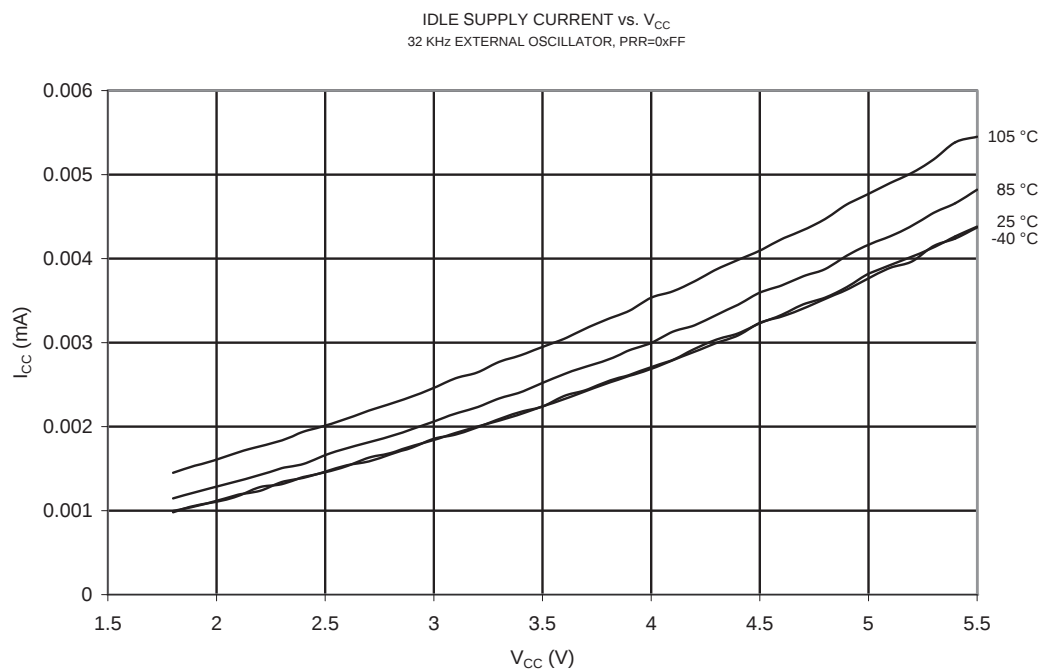


Figure 2-8. Idle Supply Current vs. V_{CC} (32 kHz External Clock)



2.3 Current Consumption in Power-Down Mode

Figure 2-9. Power-Down Supply Current vs. V_{CC} (Watchdog Timer Disabled)

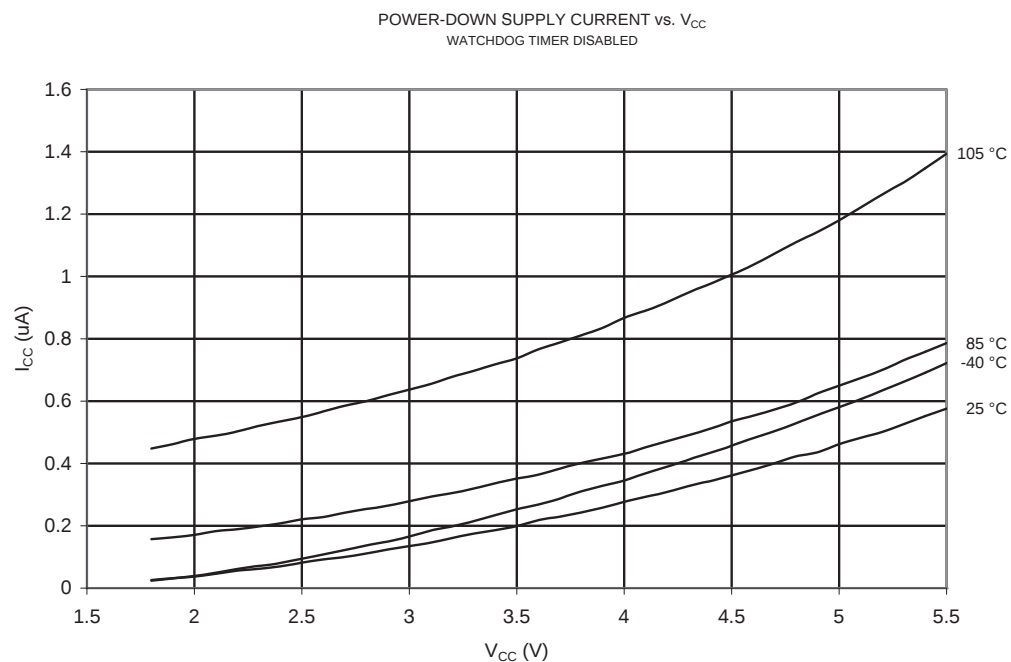
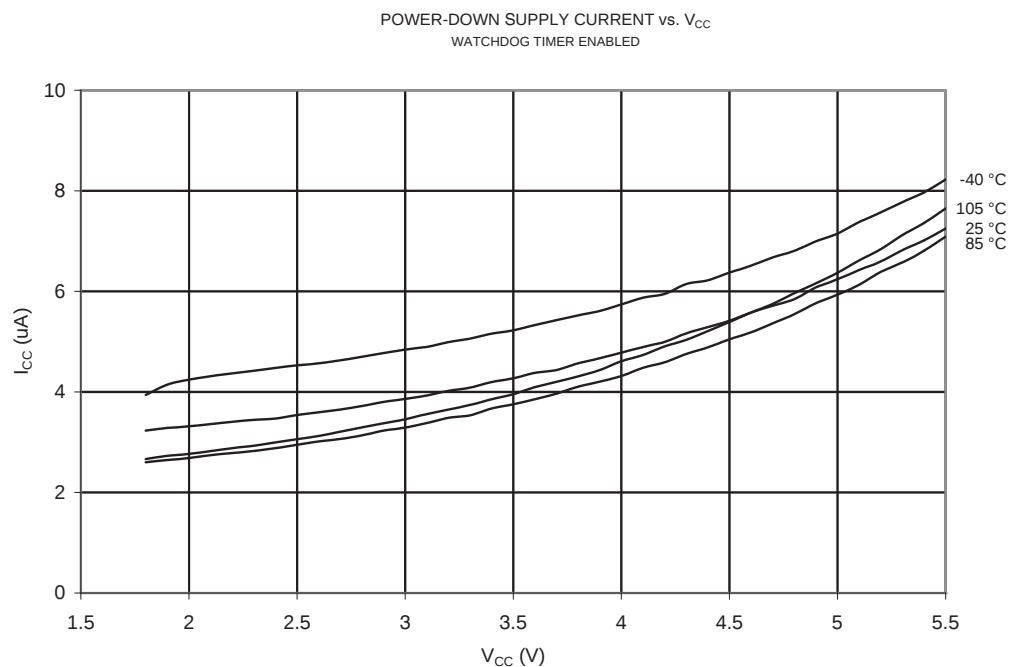


Figure 2-10. Power-Down Supply Current vs. V_{CC} (Watchdog Timer Enabled)



2.4 Current Consumption of Peripheral Units

Figure 2-11. Brownout Detector Current vs. V_{CC}

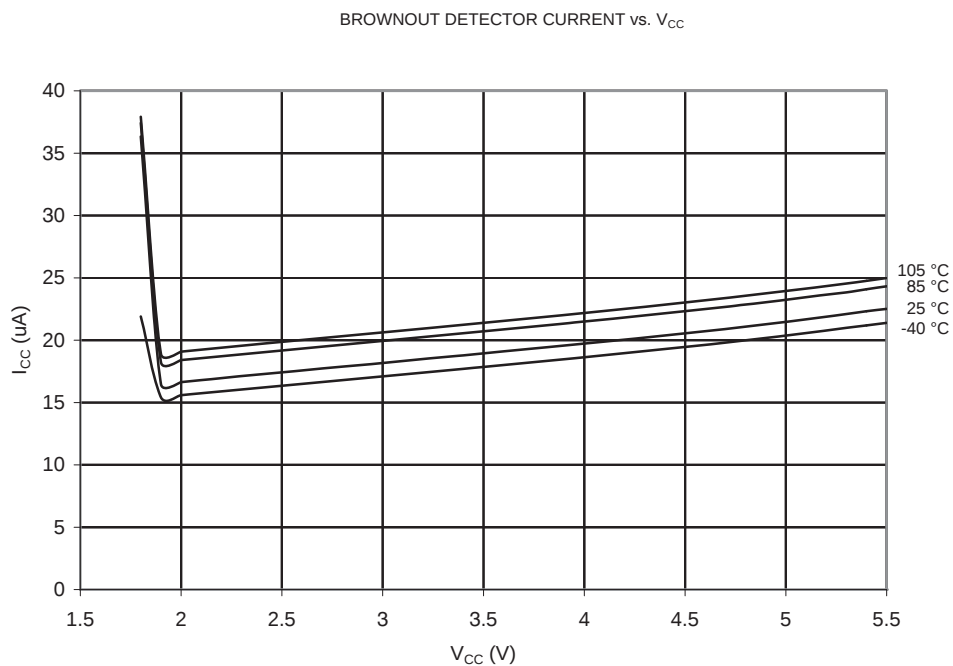


Figure 2-12. ADC Current vs. V_{CC}

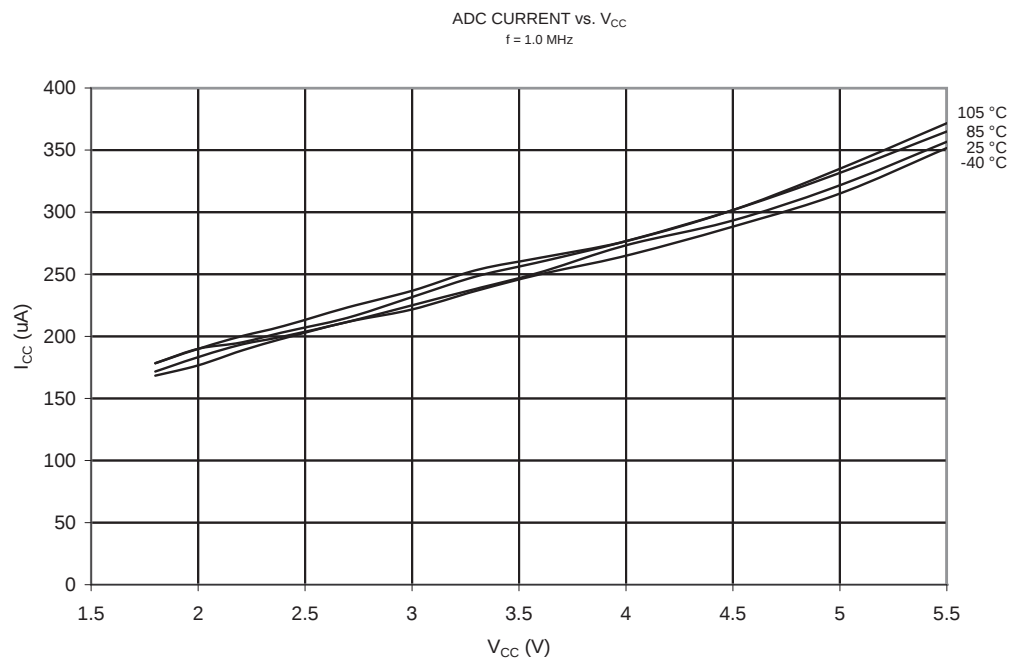


Figure 2-13. Analog Comparator Current vs. V_{CC}

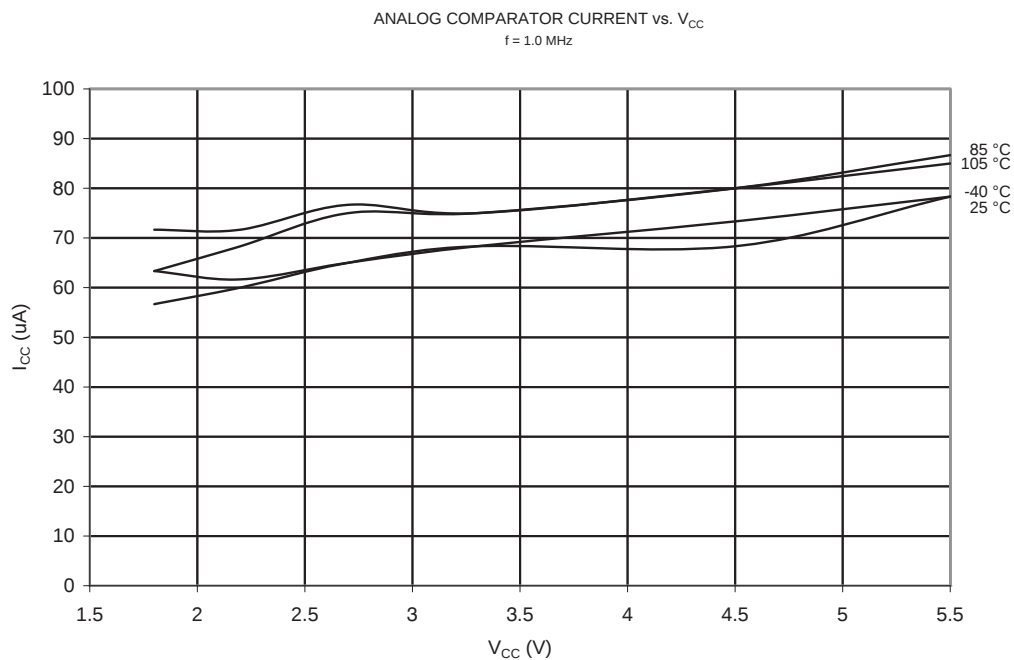
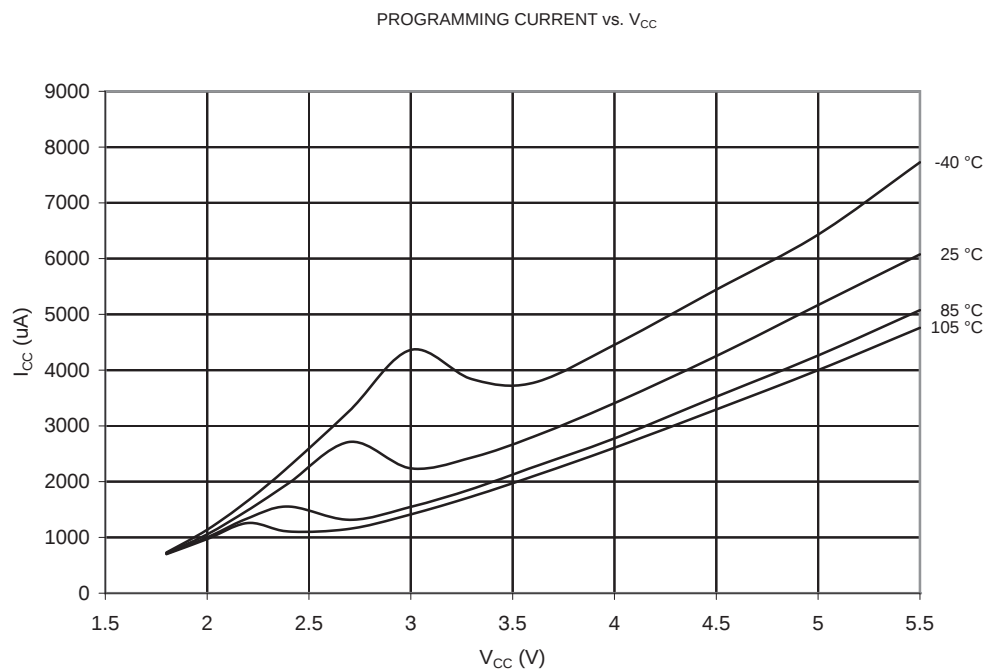


Figure 2-14. Programming Current vs. V_{CC}



2.5 Pull-up Resistors

Figure 2-15. Pull-up Resistor Current vs. Input Voltage (I/O Pin, $V_{CC} = 1.8V$)

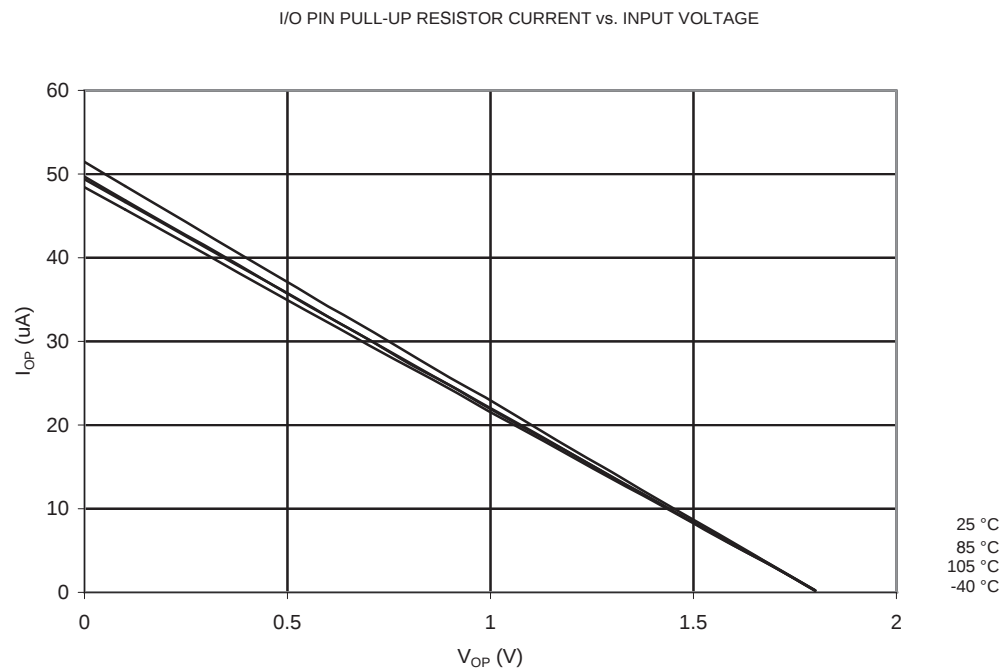


Figure 2-16. Pull-up Resistor Current vs. Input Voltage (I/O Pin, $V_{CC} = 3V$)

I/O PIN PULL-UP RESISTOR CURRENT vs. INPUT VOLTAGE
 $V_{CC} = 3V$

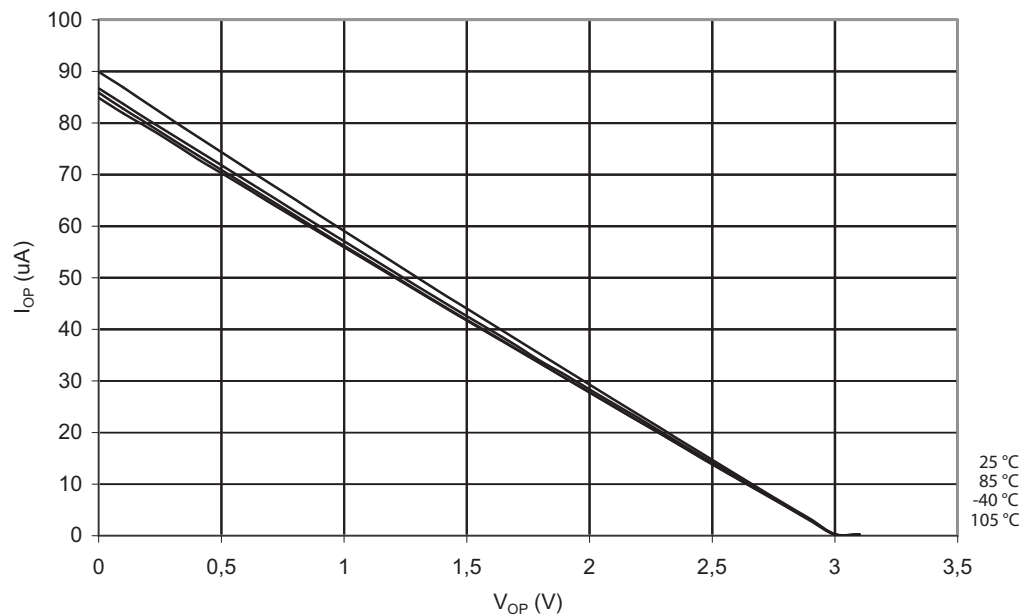


Figure 2-17. Pull-up Resistor Current vs. Input Voltage (I/O Pin, $V_{CC} = 5V$)

I/O PIN PULL-UP RESISTOR CURRENT vs. INPUT VOLTAGE

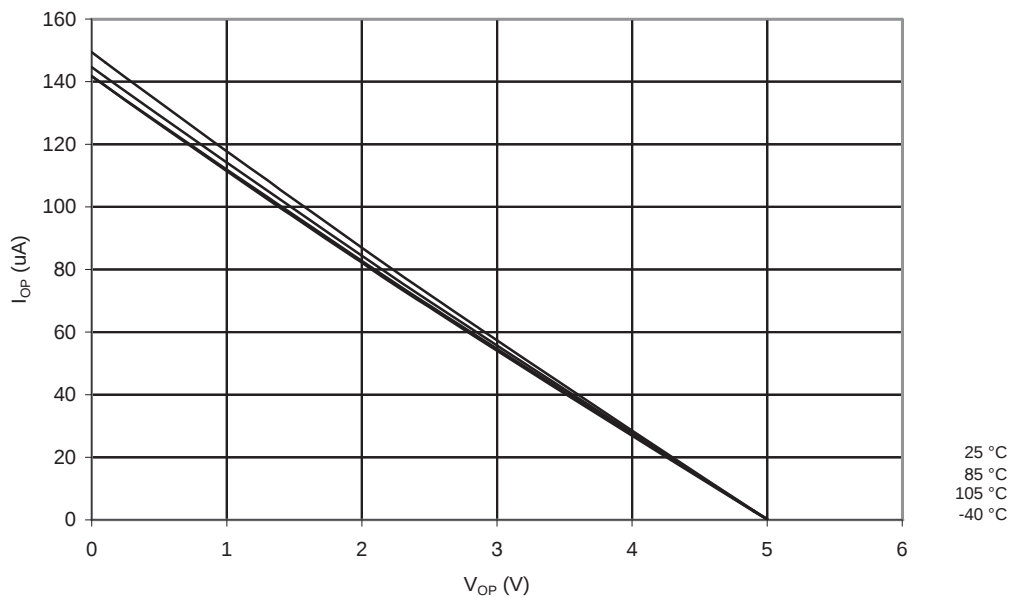


Figure 2-18. Reset Pull-up Resistor Current vs. Reset Pin Voltage ($V_{CC} = 1.8V$)

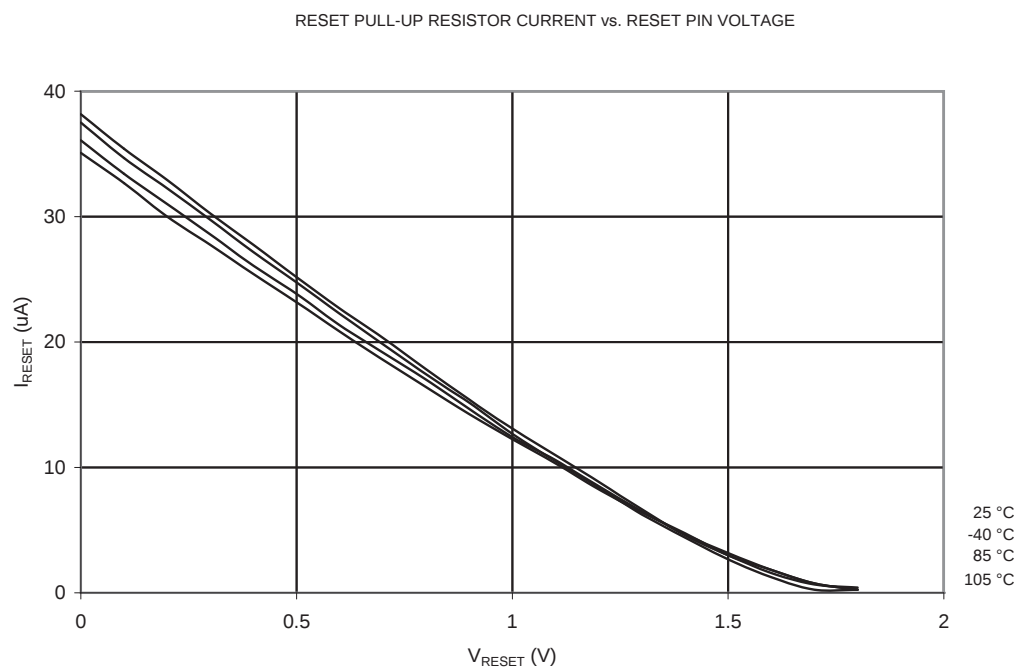


Figure 2-19. Reset Pull-up Resistor Current vs. Reset Pin Voltage ($V_{CC} = 3V$)

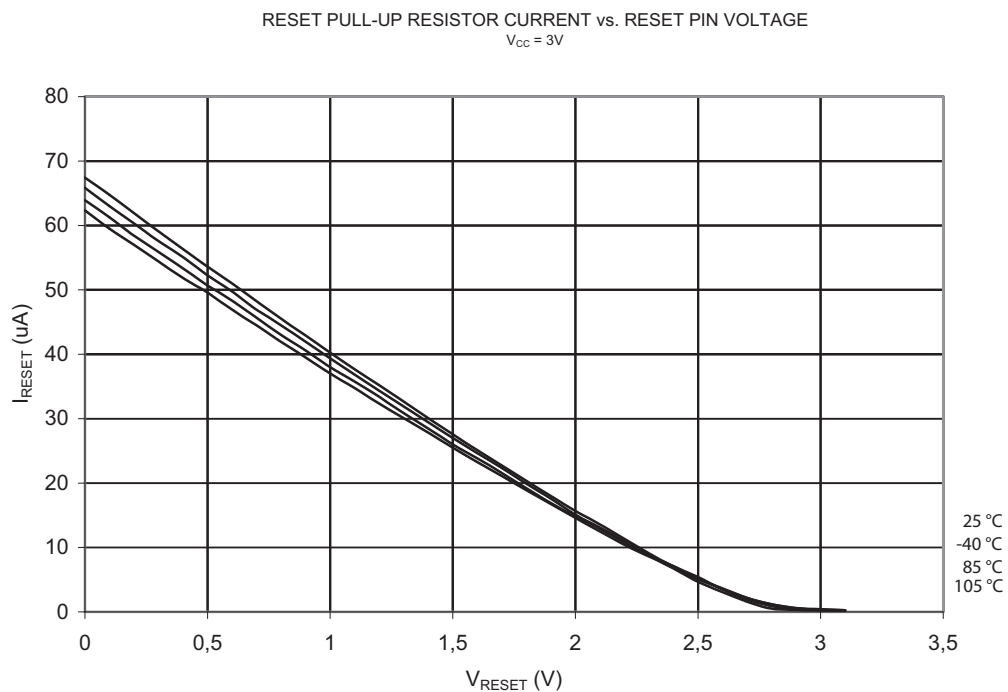
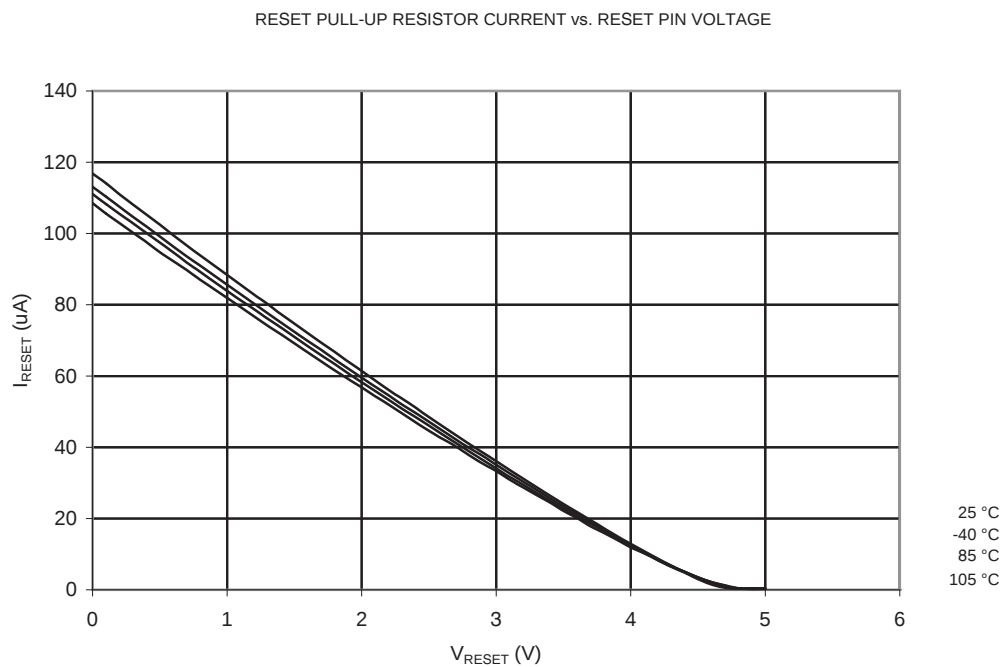


Figure 2-20. Reset Pull-up Resistor Current vs. Reset Pin Voltage ($V_{CC} = 5V$)



2.6 Output Driver Strength (Low Power Pins)

Figure 2-21. V_{OH} : I/O Pin Output Voltage vs. Source Current (Low Power Pins, $V_{CC} = 1.8V$)

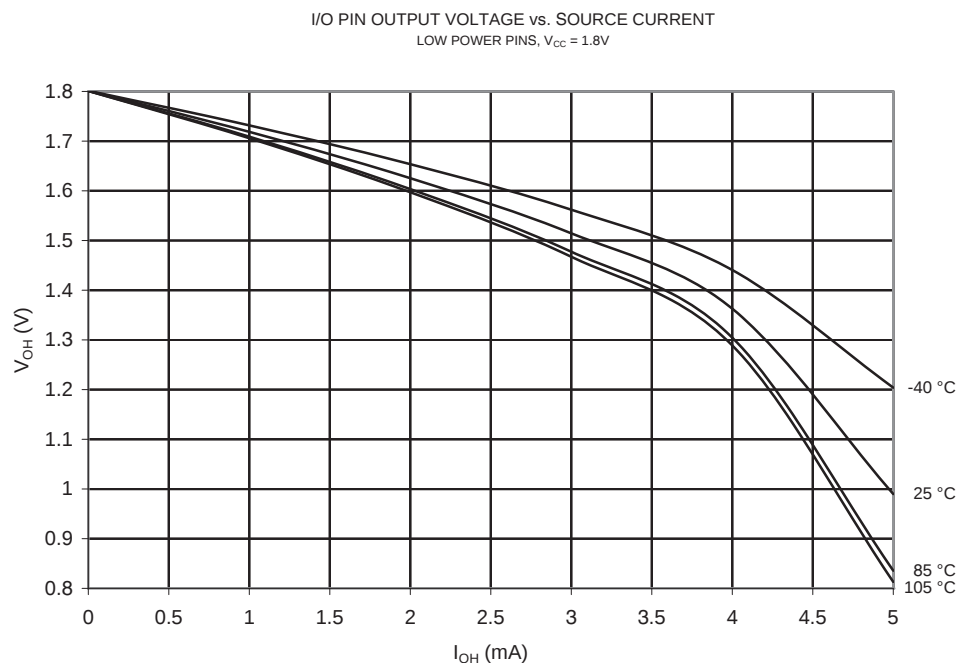


Figure 2-22. V_{OH} : I/O Pin Output Voltage vs. Source Current (Low Power Pins, $V_{CC} = 3V$)

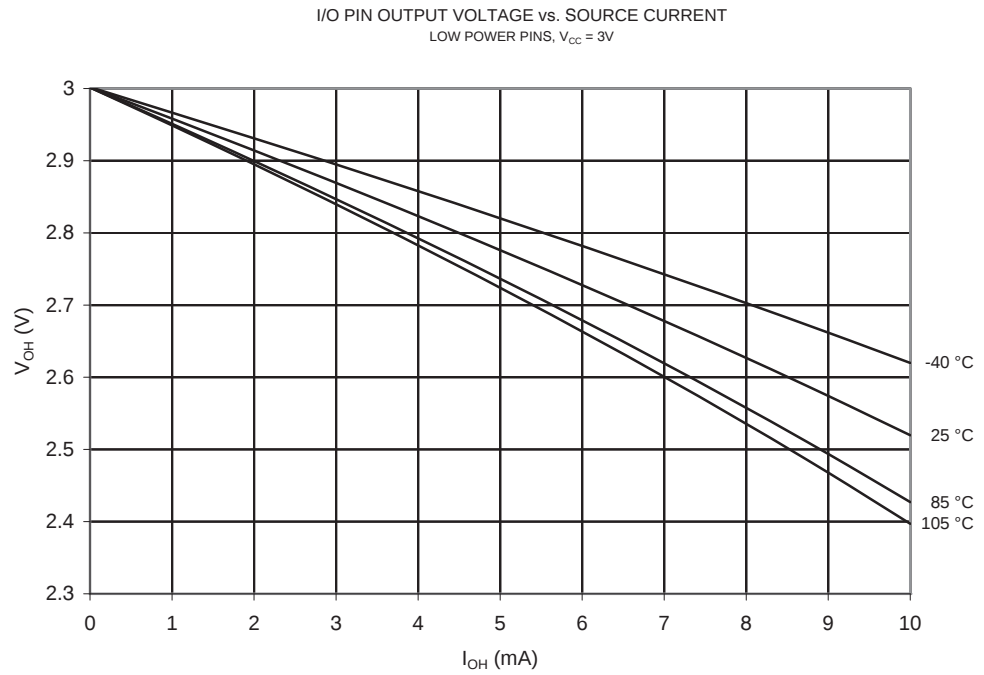


Figure 2-23. V_{OH} : I/O Pin Output Voltage vs. Source Current (Low Power Pins, $V_{CC} = 5V$)

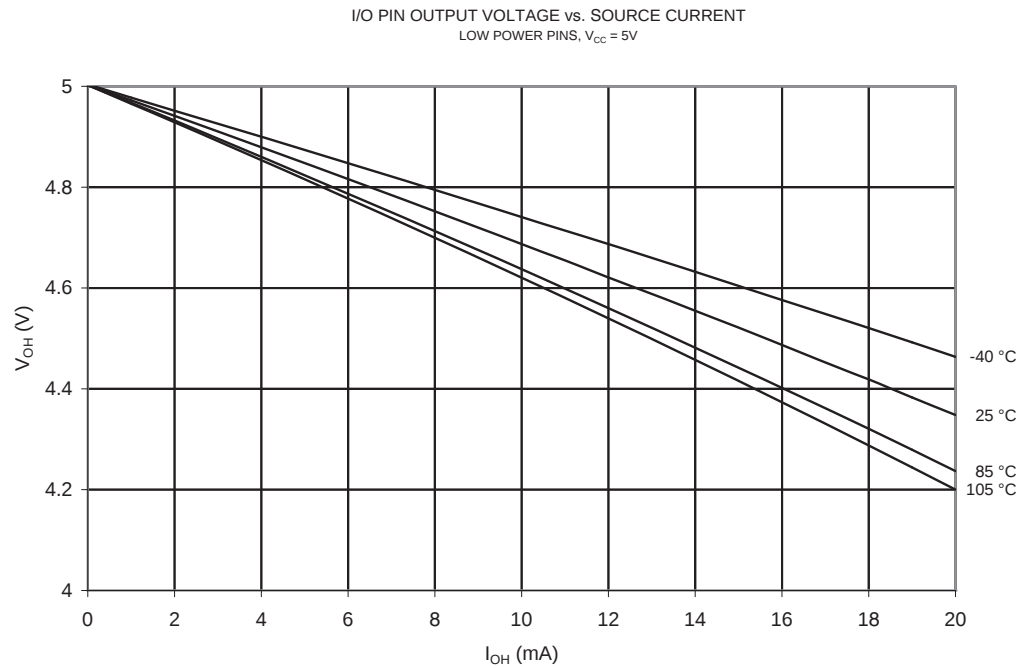


Figure 2-24. V_{OL} : I/O Pin Output Voltage vs. Sink Current (Low Power Pins, $V_{CC} = 1.8V$)

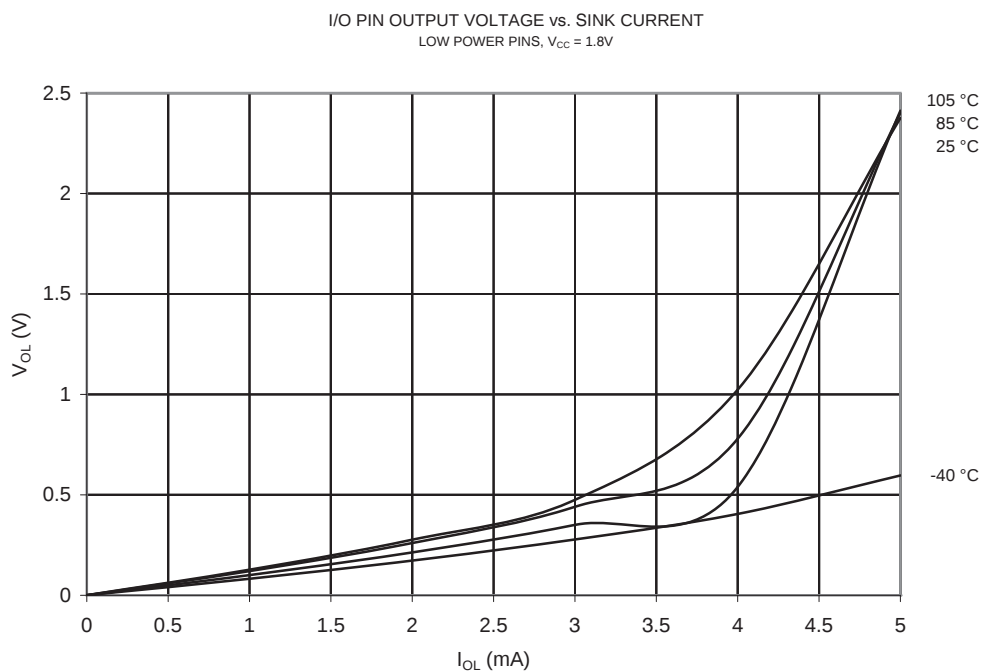


Figure 2-25. V_{OL} : I/O Pin Output Voltage vs. Sink Current (Low Power Pins, $V_{CC} = 3V$)

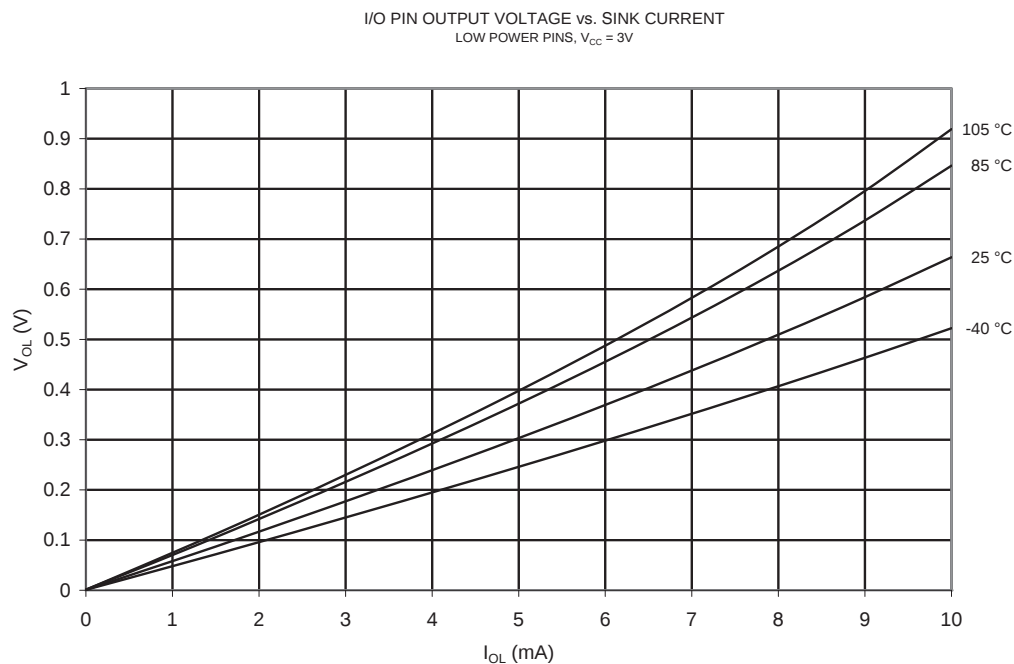
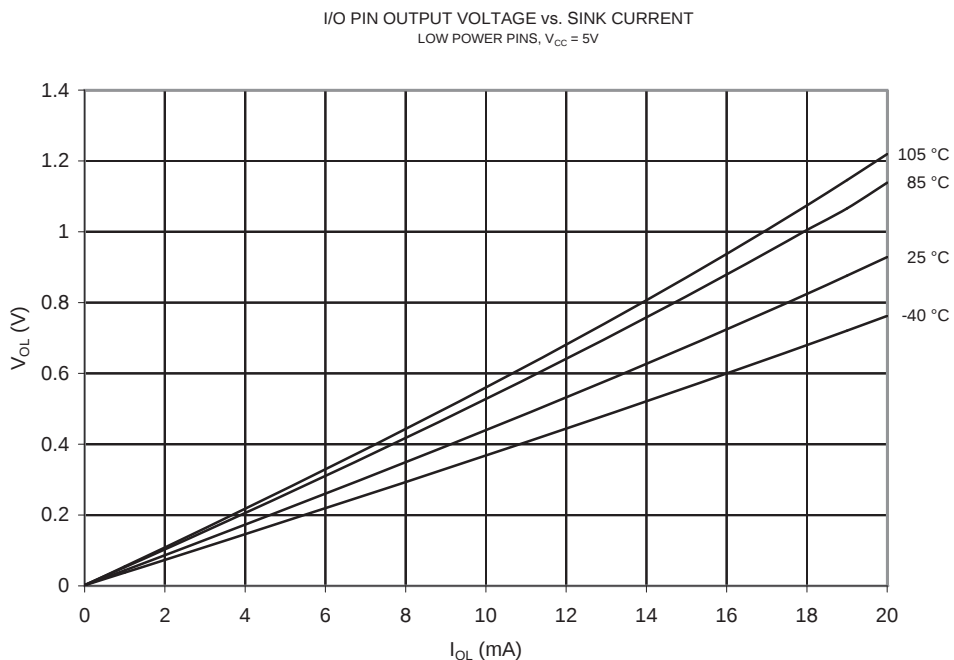


Figure 2-26. V_{OL} : I/O Pin Output Voltage vs. Sink Current (Low Power Pins, $V_{CC} = 5V$)



2.7 Output Driver Strength (Regular Pins)

Figure 2-27. V_{OH} : I/O Pin Output Voltage vs. Source Current ($V_{CC} = 1.8V$)

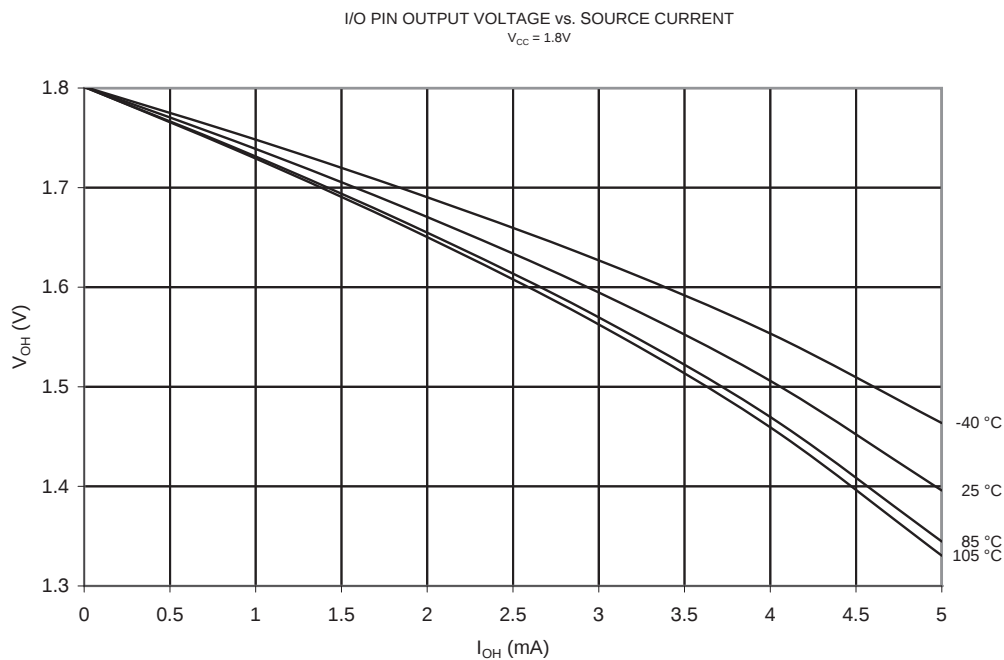


Figure 2-28. V_{OH} : I/O Pin Output Voltage vs. Source Current ($V_{CC} = 3V$)

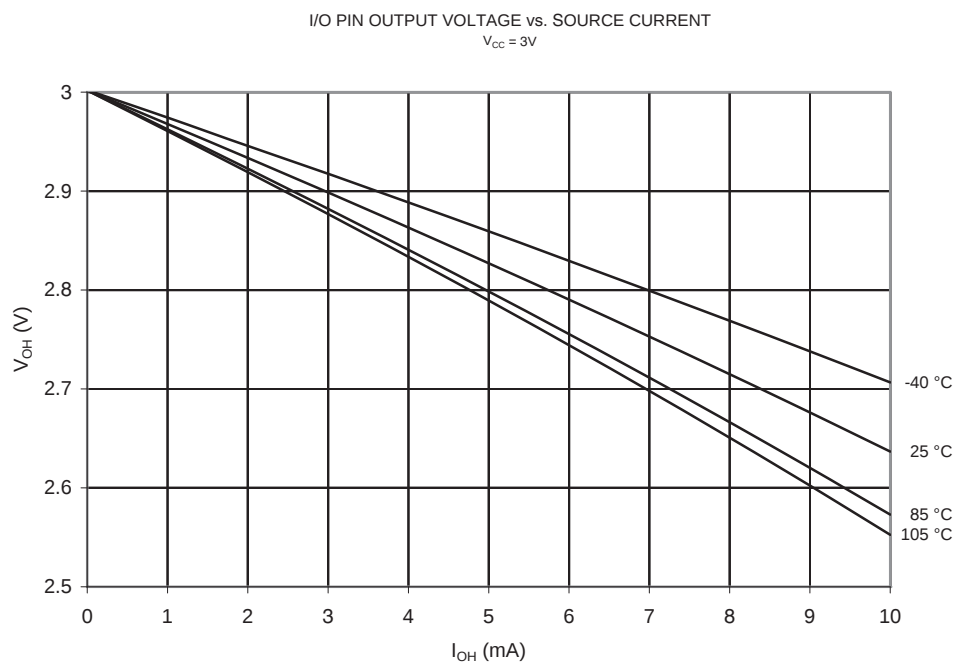


Figure 2-29. V_{OH} : I/O Pin Output Voltage vs. Source Current ($V_{CC} = 5V$)

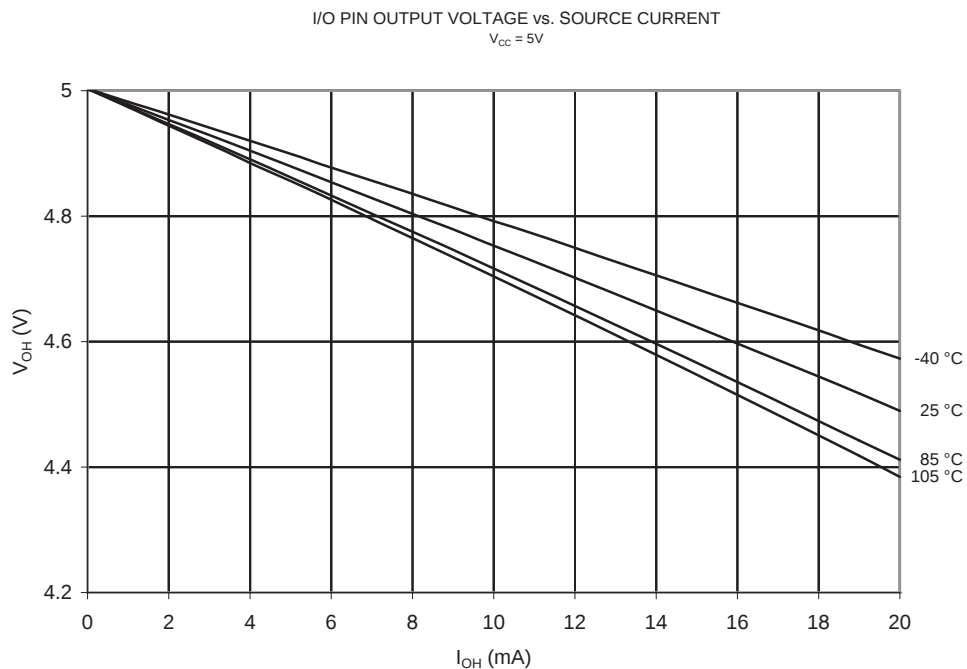


Figure 2-30. V_{OL} : I/O Pin Output Voltage vs. Sink Current ($V_{CC} = 1.8V$)

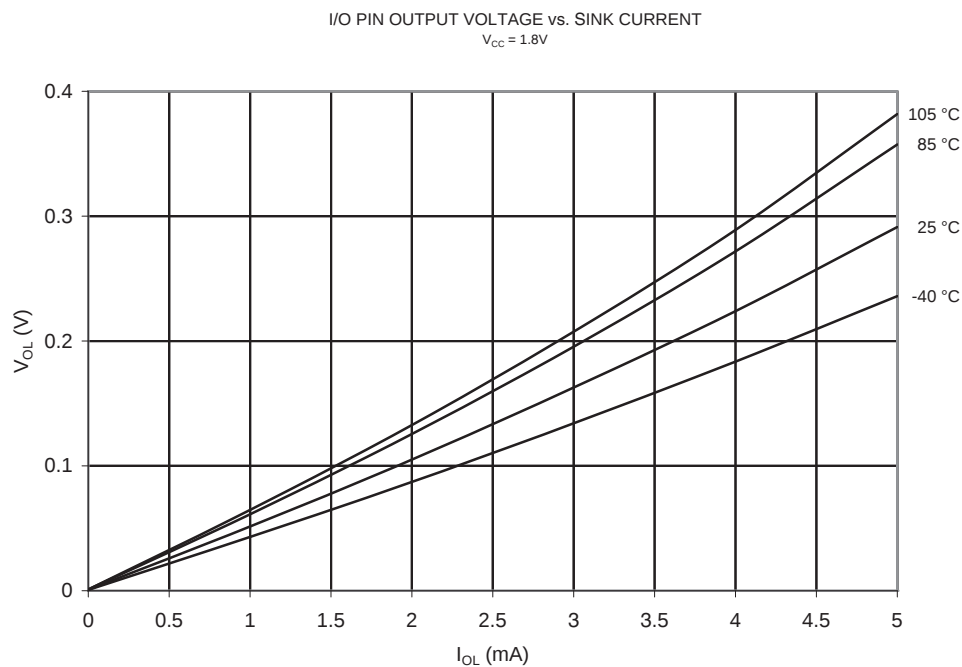


Figure 2-31. V_{OL} : I/O Pin Output Voltage vs. Sink Current ($V_{CC} = 3V$)

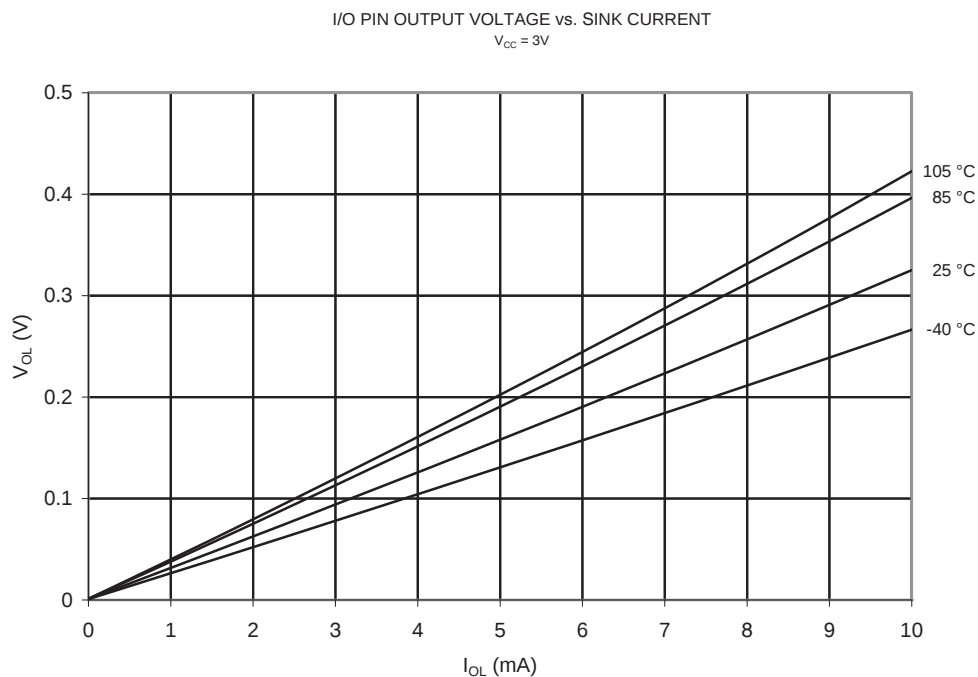


Figure 2-32. V_{OL} : I/O Pin Output Voltage vs. Sink Current ($V_{CC} = 5V$)

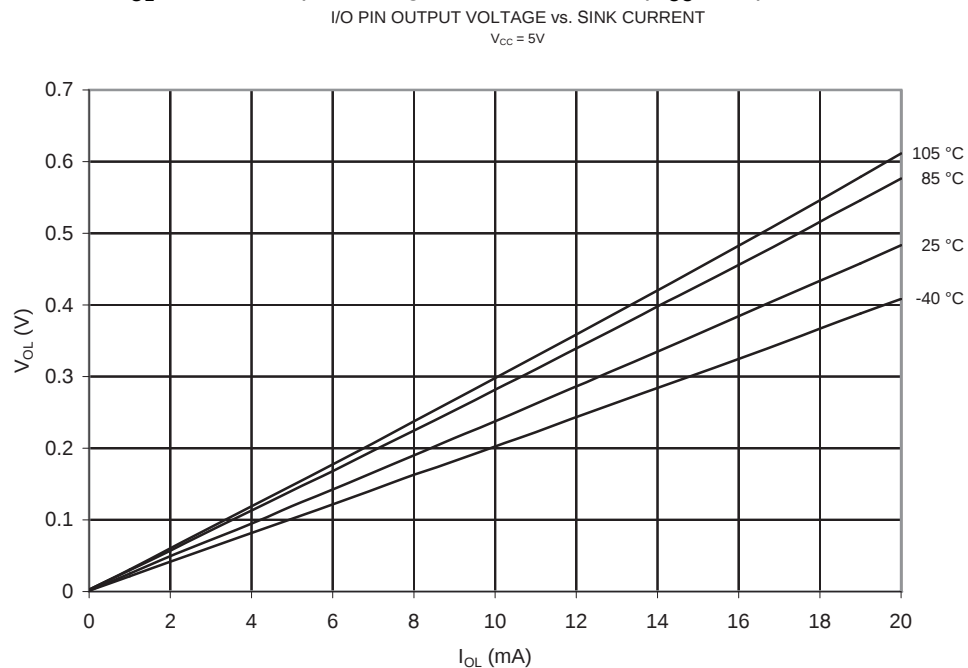


Figure 2-33. V_{OH} : Reset Pin as I/O, Output Voltage vs. Source Current ($V_{CC} = 1.8V$)

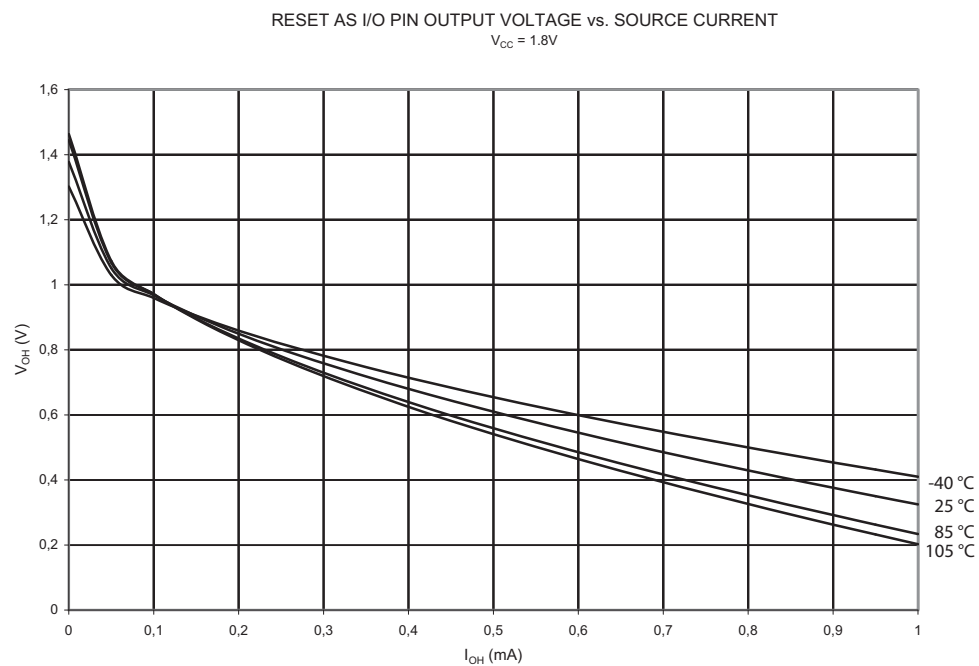


Figure 2-34. V_{OH} : Reset Pin as I/O, Output Voltage vs. Source Current ($V_{CC} = 3V$)

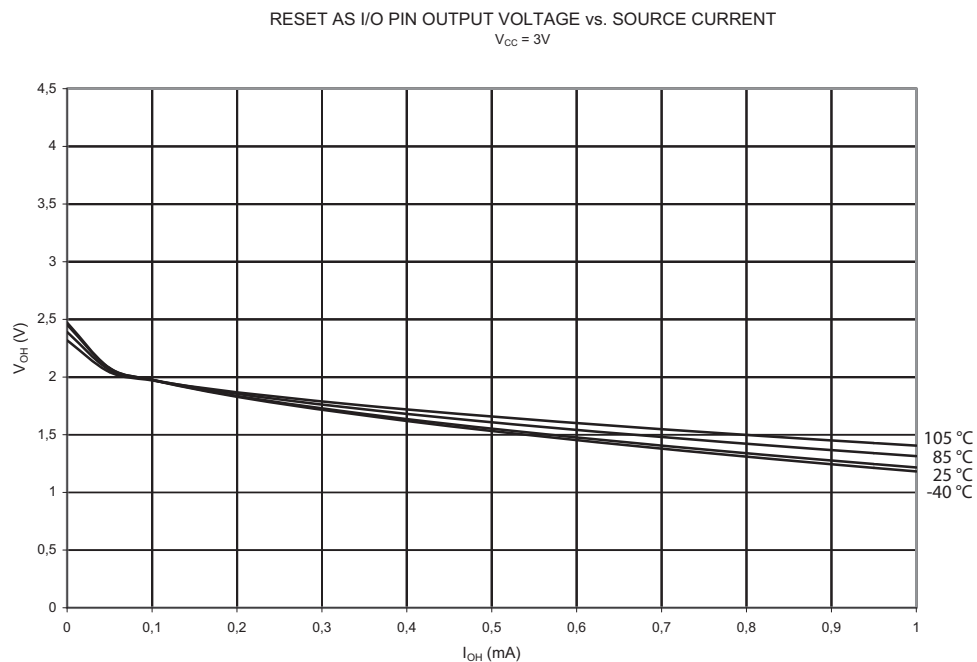


Figure 2-35. V_{OH} : Reset Pin as I/O, Output Voltage vs. Source Current ($V_{CC} = 5V$)

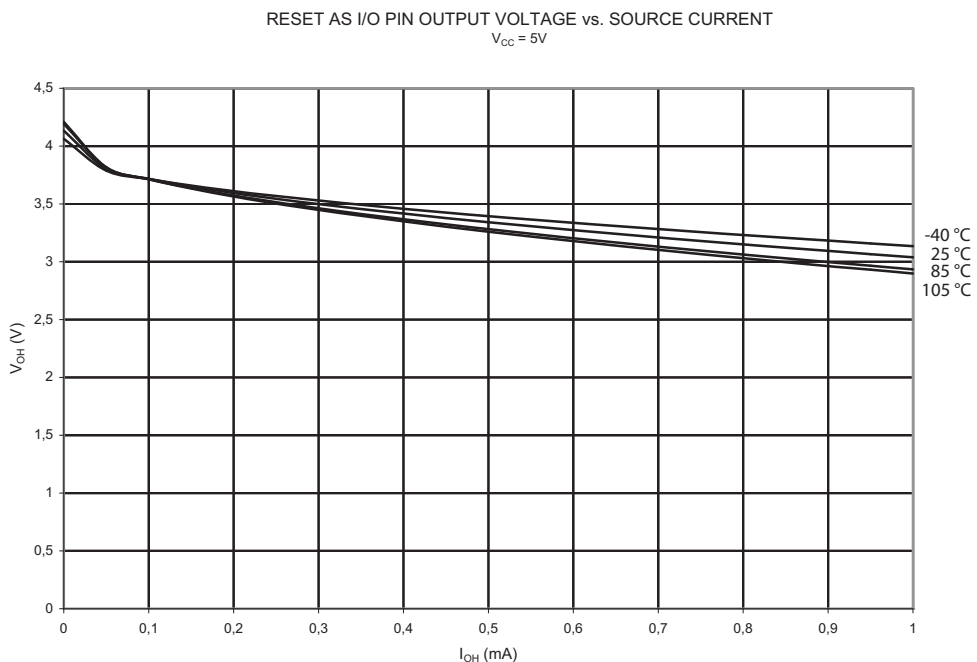


Figure 2-36. V_{OL} : Reset Pin as I/O, Output Voltage vs. Sink Current ($V_{CC} = 1.8V$)

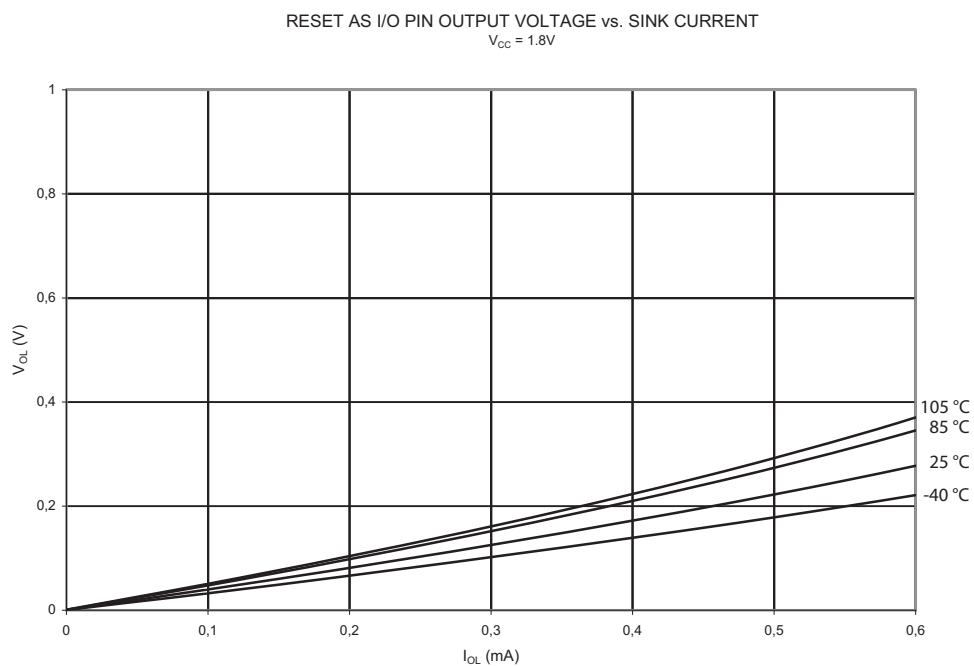


Figure 2-37. V_{OL} : Reset Pin as I/O, Output Voltage vs. Sink Current ($V_{CC} = 3V$)

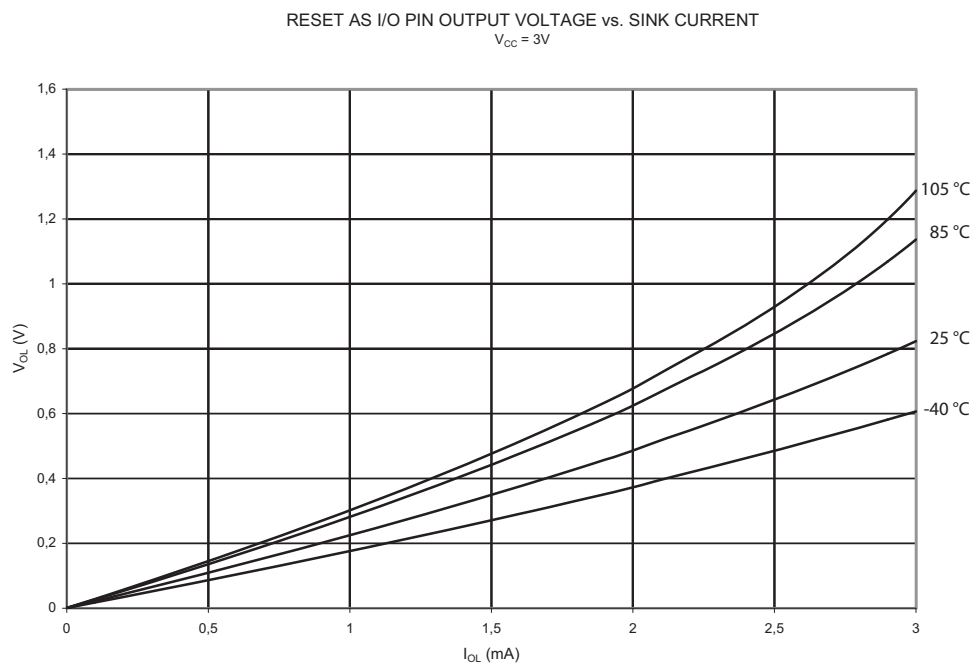
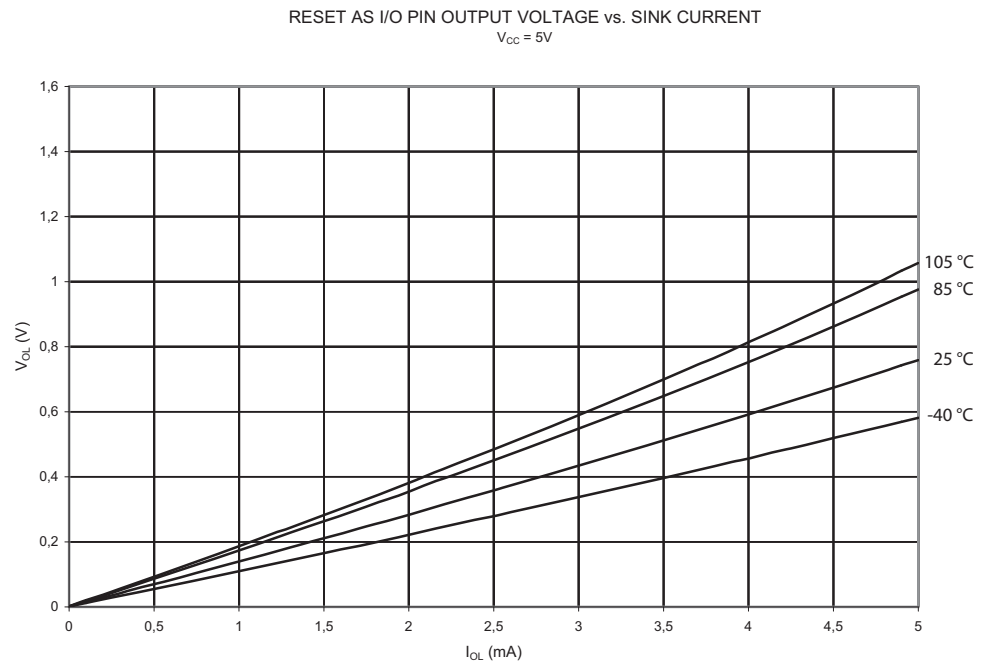


Figure 2-38. V_{OL} : Reset Pin as I/O, Output Voltage vs. Sink Current ($V_{CC} = 5V$)



2.8 Input Thresholds and Hysteresis (for I/O Ports)

Figure 2-39. V_{IH} : Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '1')

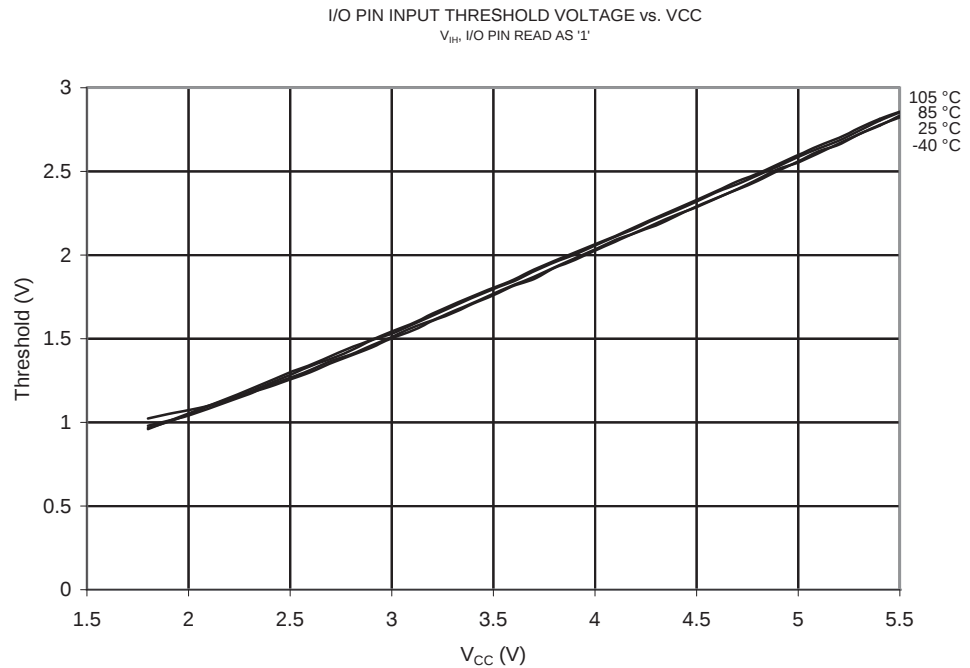


Figure 2-40. V_{IL} : Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '0')

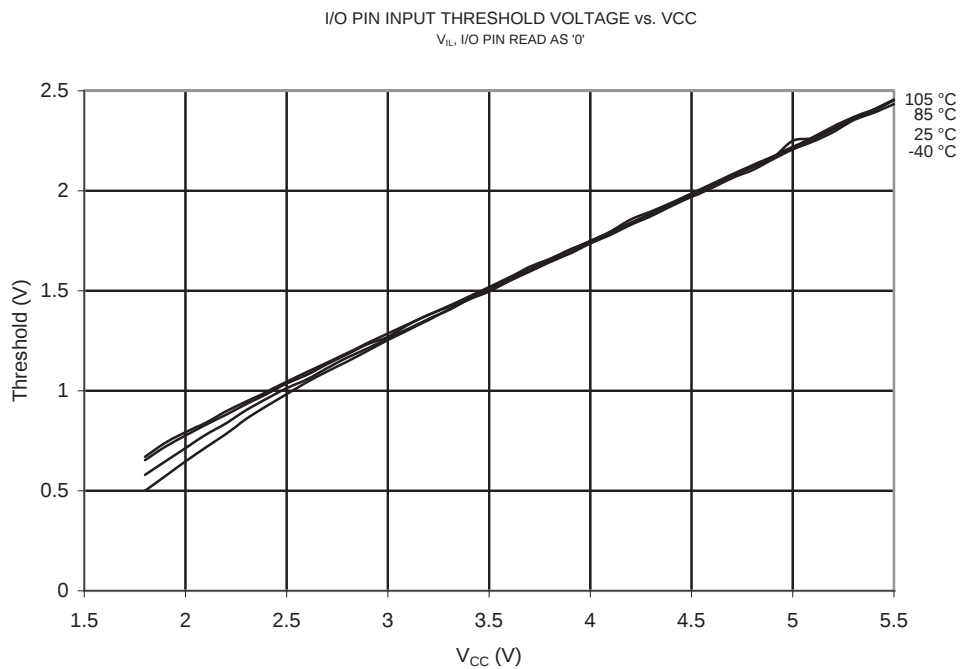


Figure 2-41. $V_{IH}-V_{IL}$: Input Hysteresis vs. V_{CC} (I/O Pin)

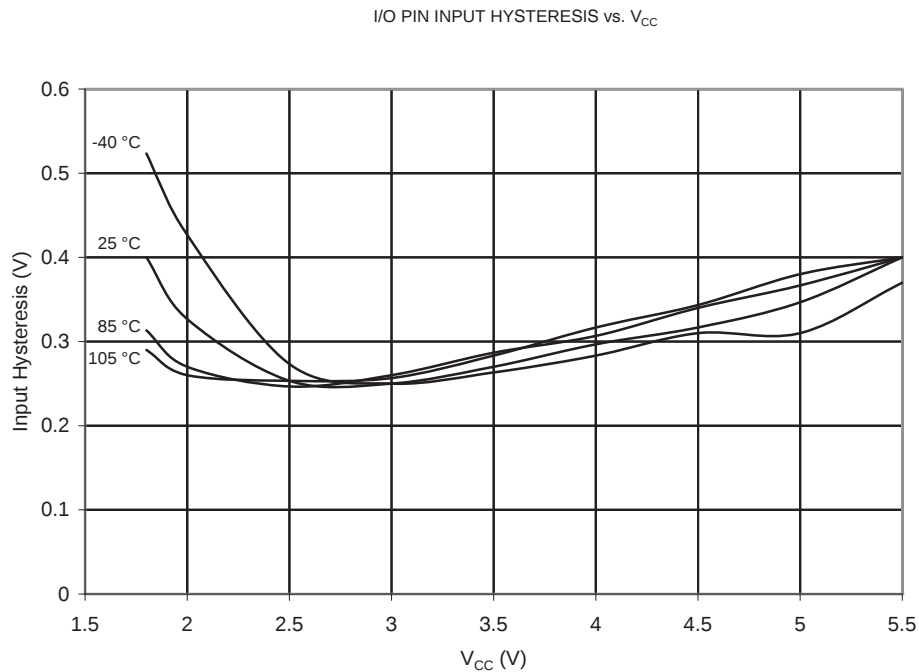


Figure 2-42. V_{IH} : Input Threshold Voltage vs. V_{CC} (Reset Pin as I/O, Read as '1')

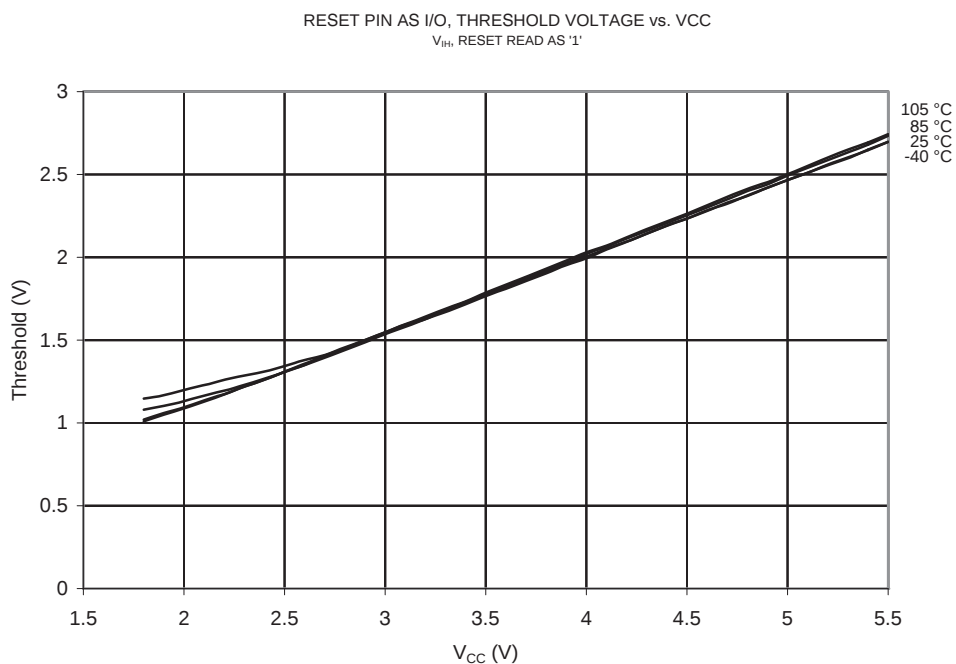


Figure 2-43. V_{IL} : Input Threshold Voltage vs. V_{CC} (Reset Pin as I/O, Read as '0')

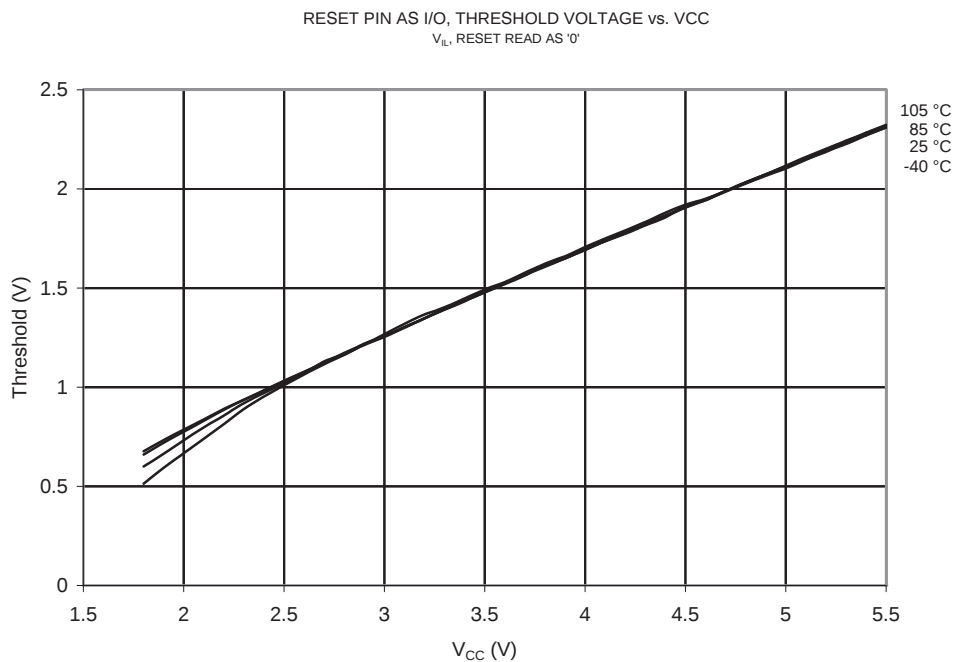
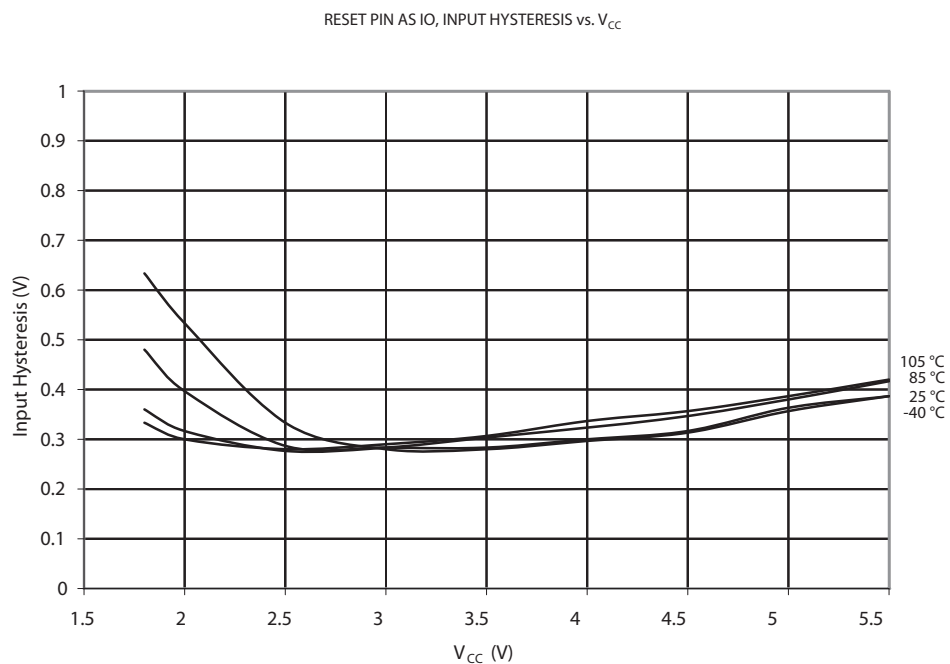


Figure 2-44. $V_{IH}-V_{IL}$: Input Hysteresis vs. V_{CC} (Reset Pin as I/O)



2.9 BOD, Bandgap and Reset

Figure 2-45. BOD Thresholds vs. Temperature (BODLEVEL is 4.3V)

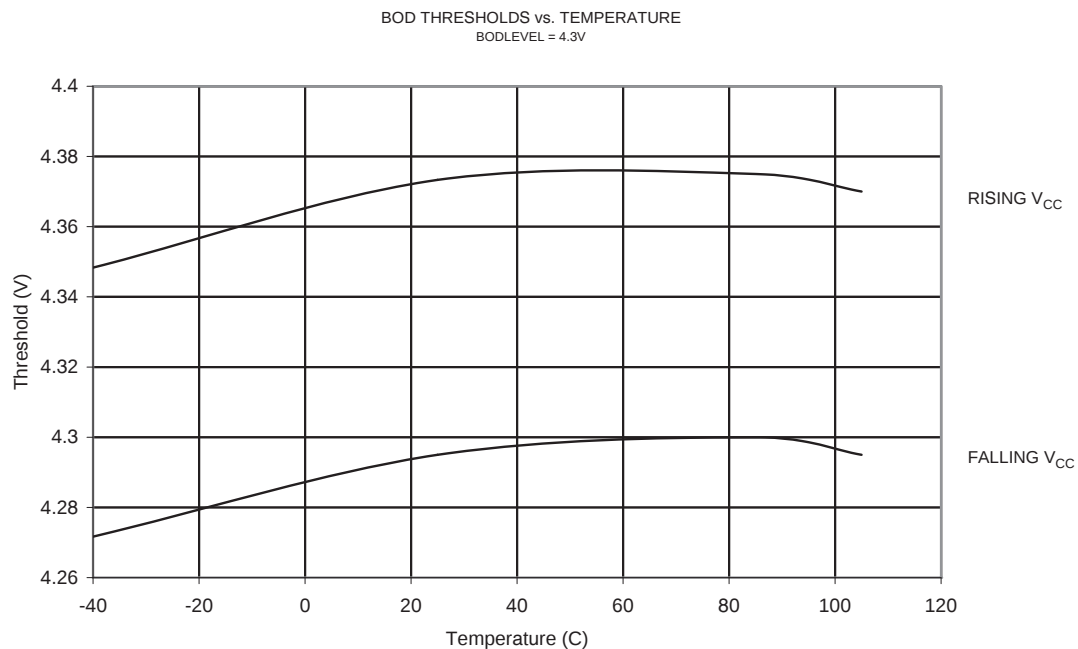


Figure 2-46. BOD Thresholds vs. Temperature (BODLEVEL is 2.7V)

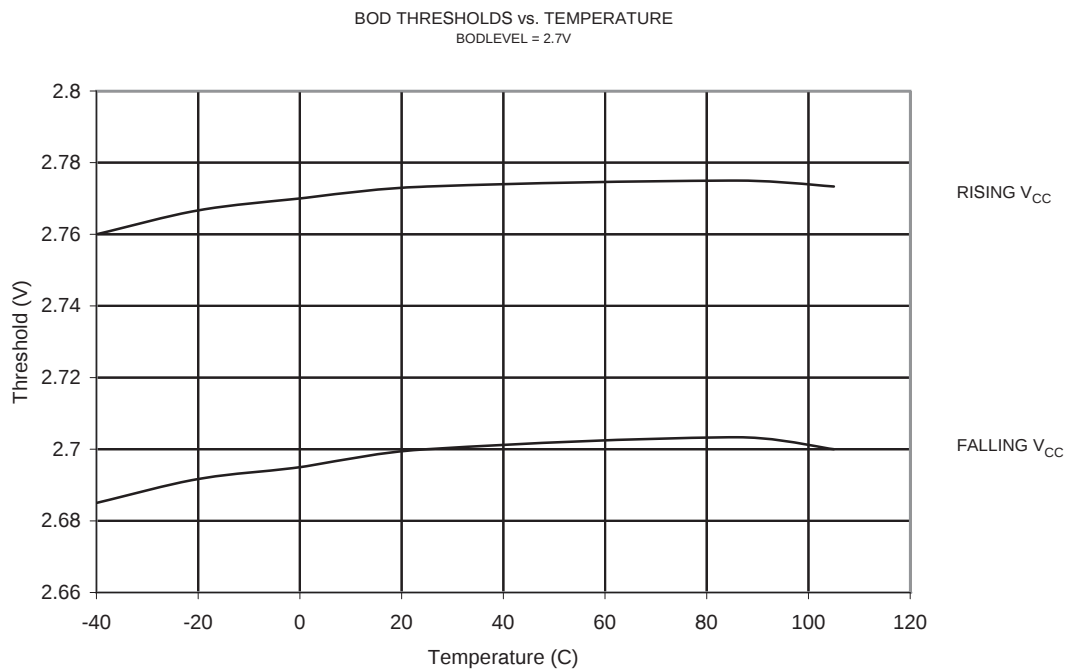


Figure 2-47. BOD Thresholds vs. Temperature (BODLEVEL is 1.8V)

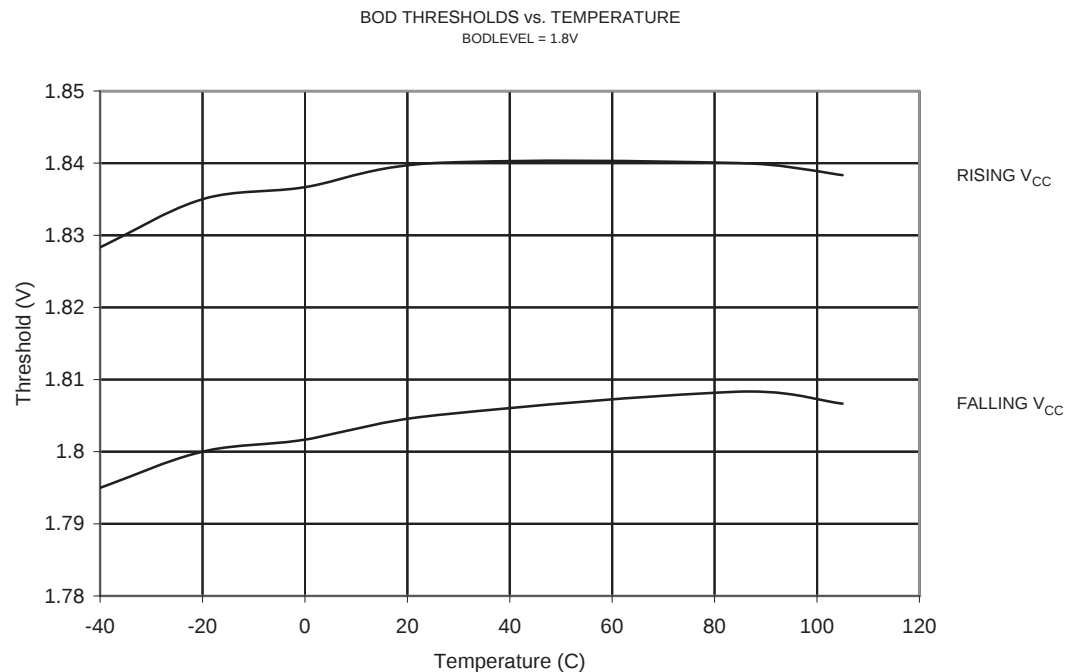


Figure 2-48. Bandgap Voltage vs. V_{CC}

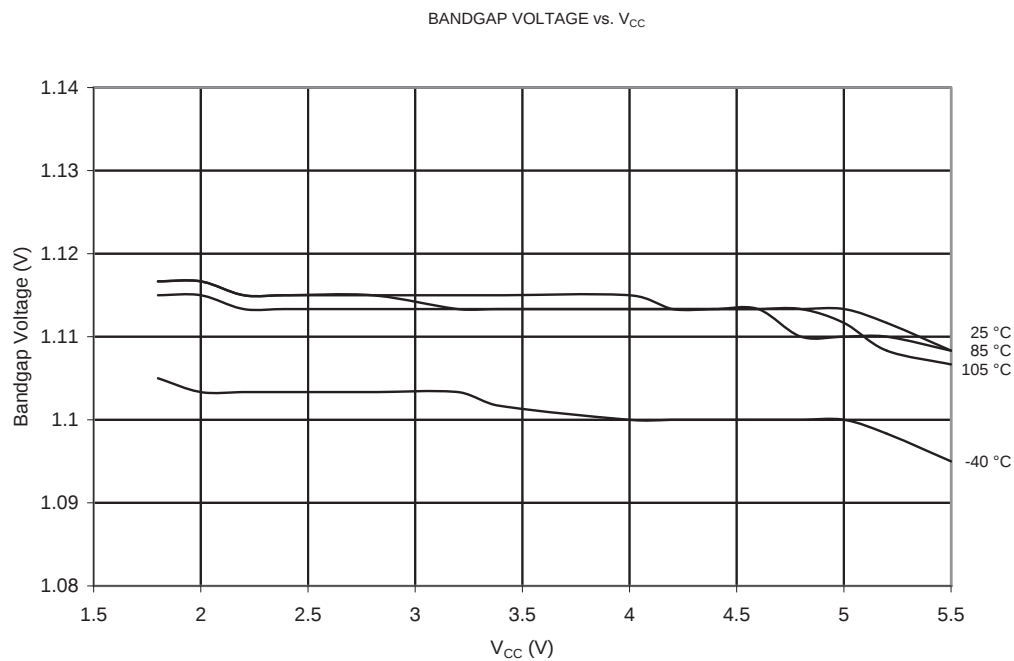


Figure 2-49. V_{IH} : Reset Input Threshold Voltage vs. V_{CC} (Reset Pin Read as '1')

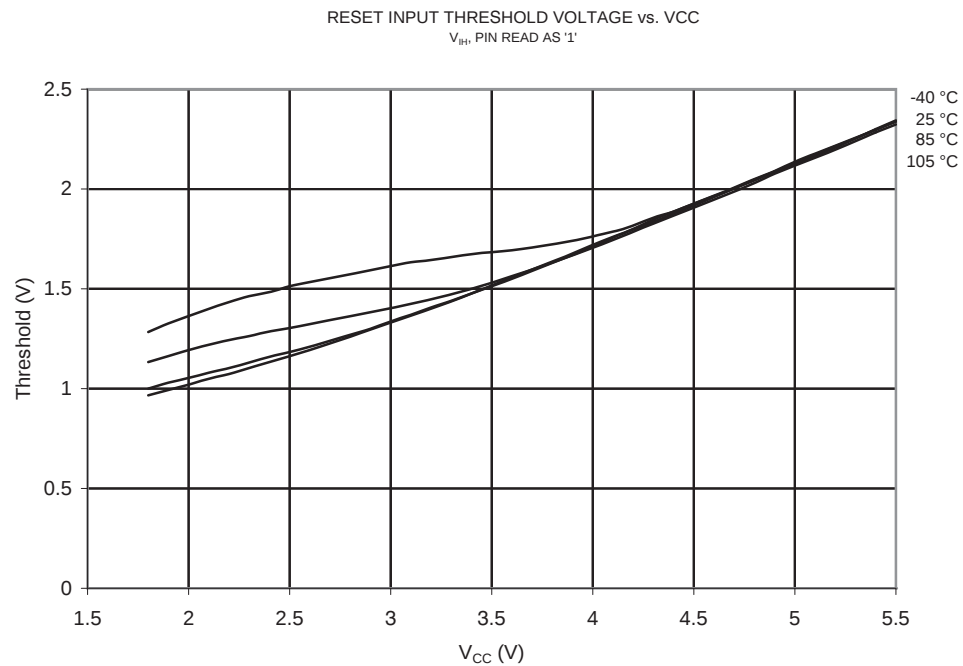


Figure 2-50. V_{IH} : Reset Input Threshold Voltage vs. V_{CC} (Reset Pin Read as '0')

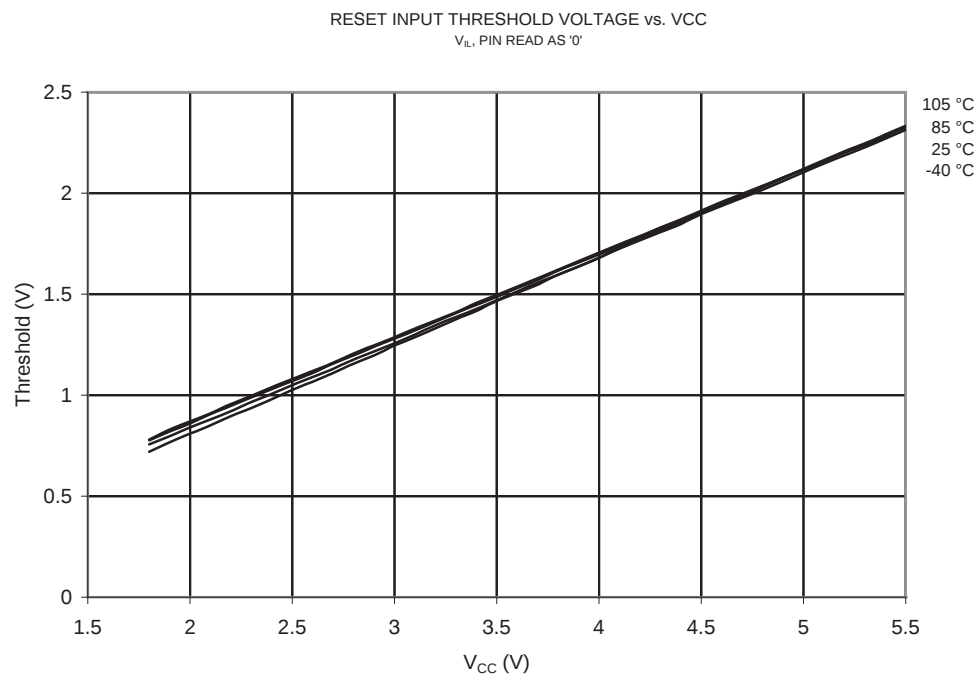


Figure 2-51. $V_{IH}-V_{IL}$: Reset Input Pin Hysteresis vs. V_{CC}

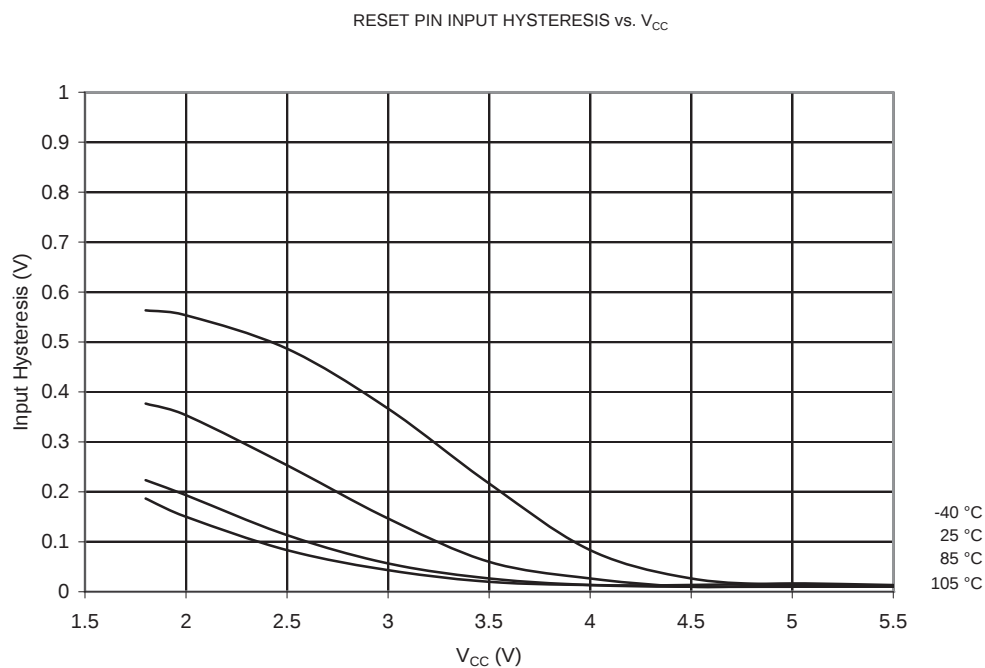
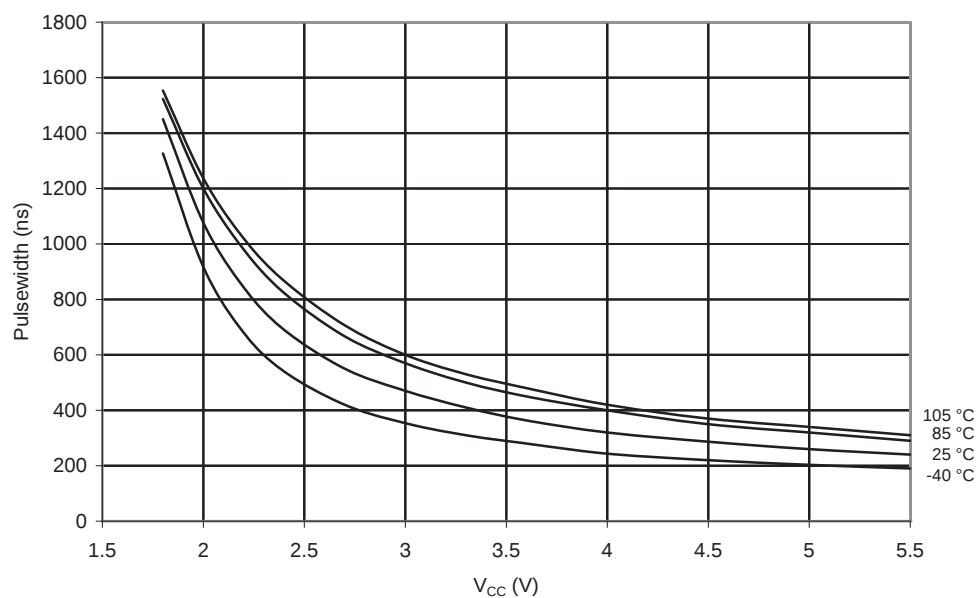


Figure 2-52. Minimum Reset Pulse Width vs. V_{CC}

MINIMUM RESET PULSE WIDTH vs. V_{CC}



2.10 Internal Oscillator Speed

Figure 2-53. Calibrated 9.6 MHz Oscillator Frequency vs. Temperature

CALIBRATED 9.6MHz OSCILLATOR FREQUENCY vs. TEMPERATURE

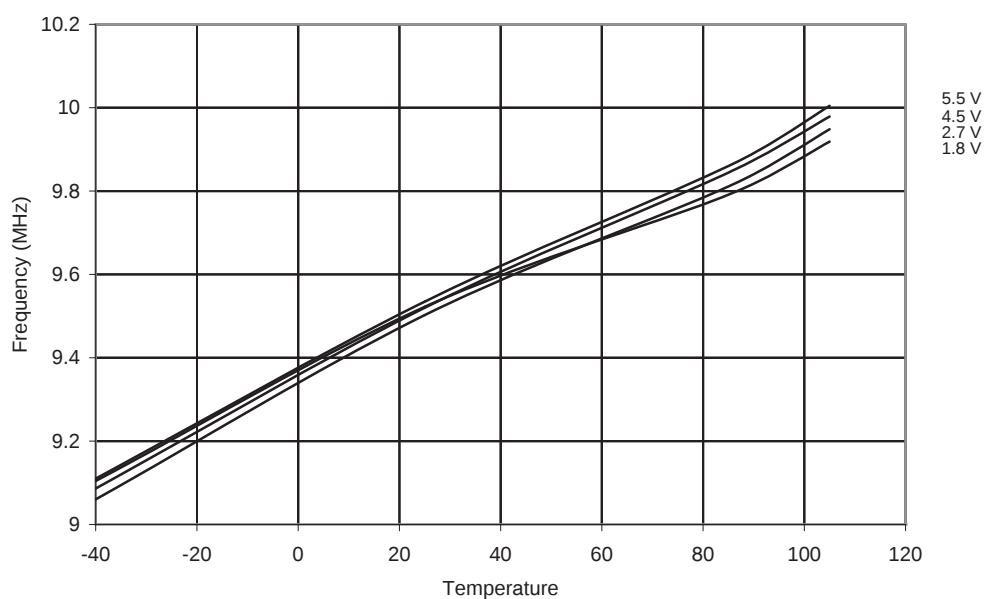


Figure 2-54. Calibrated 9.6 MHz Oscillator Frequency vs. V_{CC}

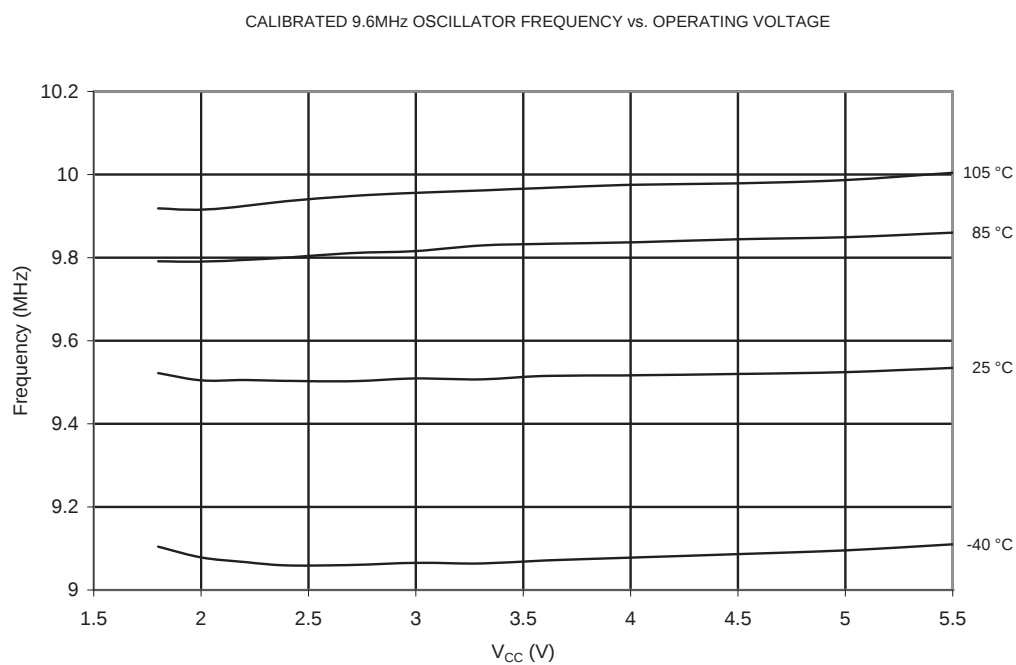


Figure 2-55. Calibrated 4.8 MHz Oscillator Frequency vs. Temperature

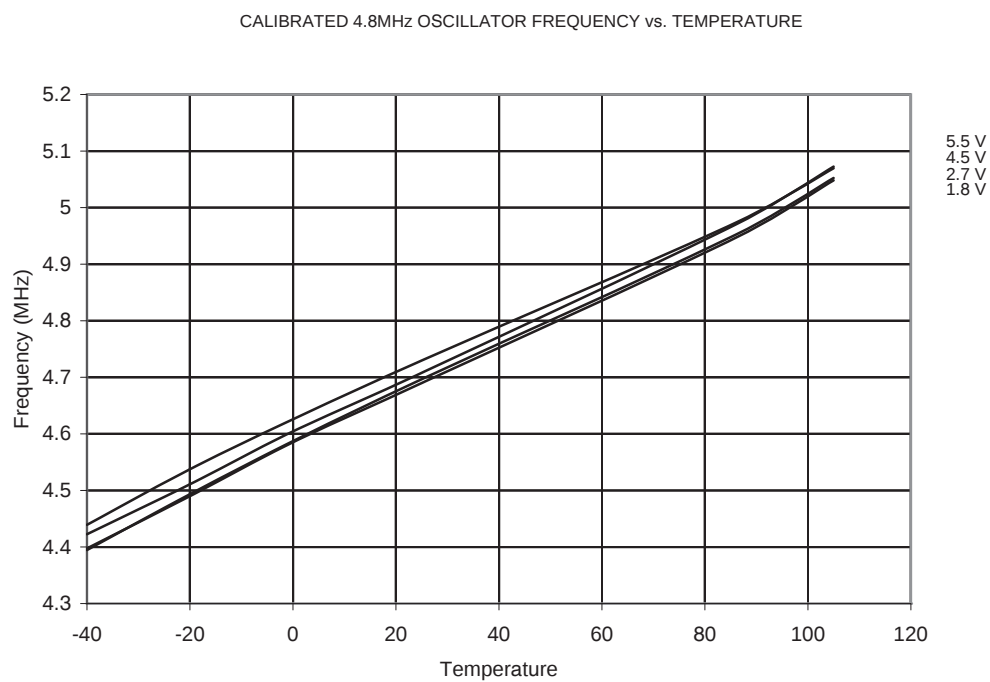


Figure 2-56. Calibrated 4.8 MHz Oscillator Frequency vs. V_{CC}

CALIBRATED 4.8MHz OSCILLATOR FREQUENCY vs. OPERATING VOLTAGE

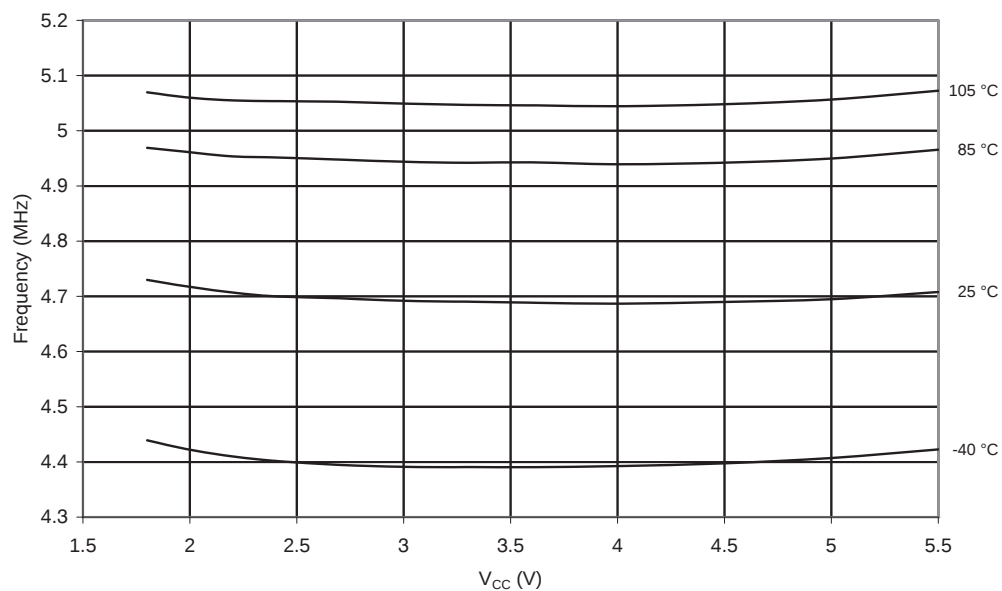


Figure 2-57. 128 kHz Watchdog Oscillator Frequency vs. Temperature

WATCHDOG OSCILLATOR FREQUENCY vs. TEMPERATURE

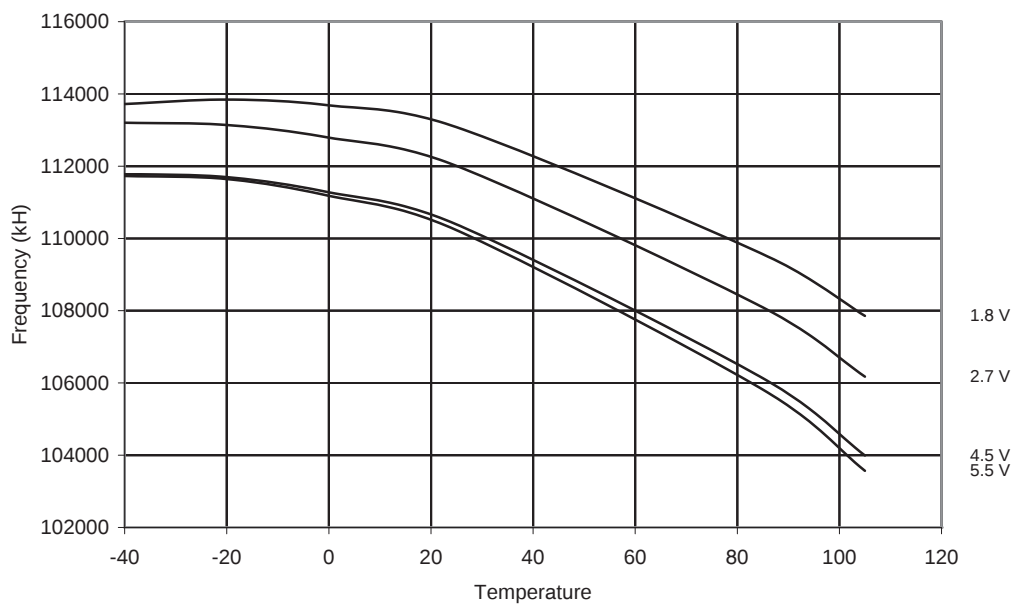
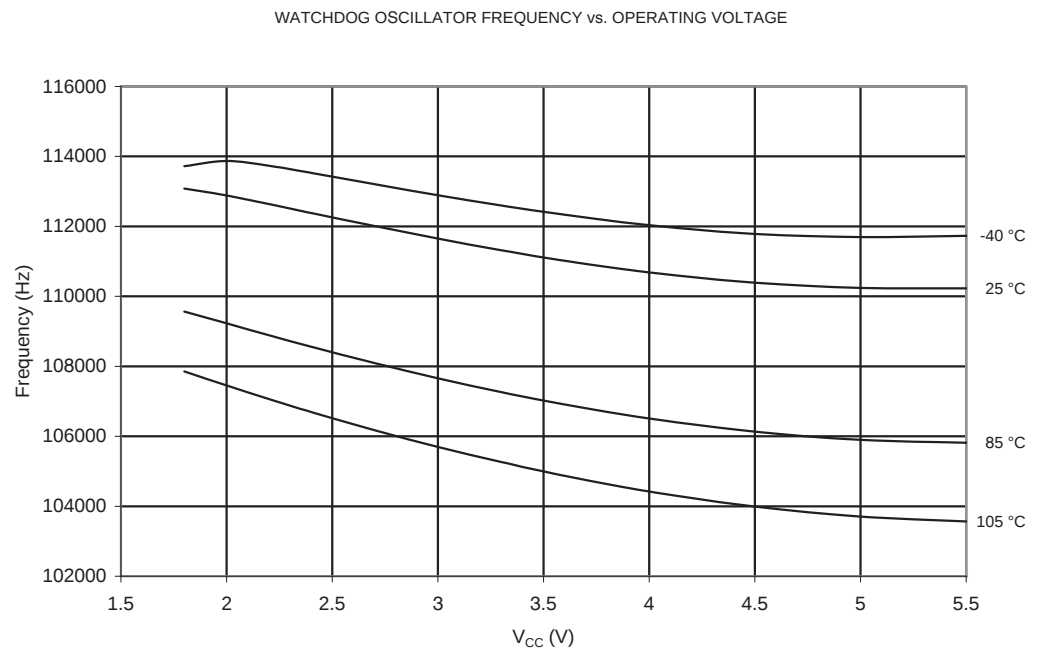


Figure 2-58. 128 kHz Watchdog Oscillator Frequency vs. V_{CC}





3. Ordering Information

Speed (MHz)	Power Supply (V)	Ordering Code ⁽¹⁾	Package ⁽²⁾	Operation Range
20	1.8 - 5.5	ATtiny13A-SN ATtiny13A-SNR ATtiny13A-SS7 ATtiny13A-SS7R	8S2 8S2 8S1 8S1	Industrial (-40°C to +105°C)

Notes: 1. Code indicators:

- 7: NiPdAu lead finish
- N: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).

Package Type	
8S2	8-lead, 0.209" Wide, Plastic Small Outline Package (EIAJ SOIC)
8S1	8-lead, 0.150" Wide, Plastic Gull-Wing Small Outline (JEDEC SOIC)

4. Revision History

Revision No.	History
8126A-Appendix A-AVR-07/10	Initial revision
8126E-Appendix A-AVR-08/11	Removed "Preliminary" status, updated contact information



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