SMART ARM-based Microcontrollers

SAM V71 Xplained Ultra

USER GUIDE

Preface

The Atmel® | SMART SAM V71 Xplained Ultra evaluation kit is a hardware platform to evaluate the ATSAMV71Q21, and other Atmel ARM® Cortex®-M7-based microcontrollers in the SAM V70, SAM S70, and SAM E70 series.

Supported by the Atmel Studio integrated development platform, the kit provides easy access to the features of the Atmel ATSAMV71Q21 and explains how to integrate the device in a custom design.

The Xplained Ultra series evaluation kits include an on-board Embedded Debugger, and no external tools are necessary to program or debug the ATSAMV71Q21.

The Xplained Pro extension kits offers additional peripherals to extend the features of the board and ease the development of custom designs.

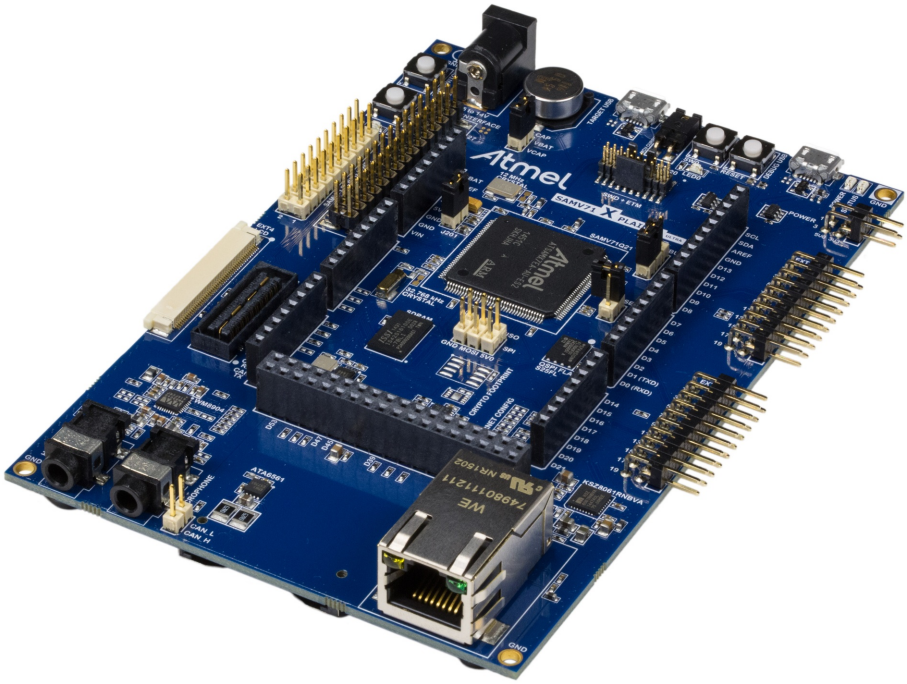


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1. Introduction

1.1. Features

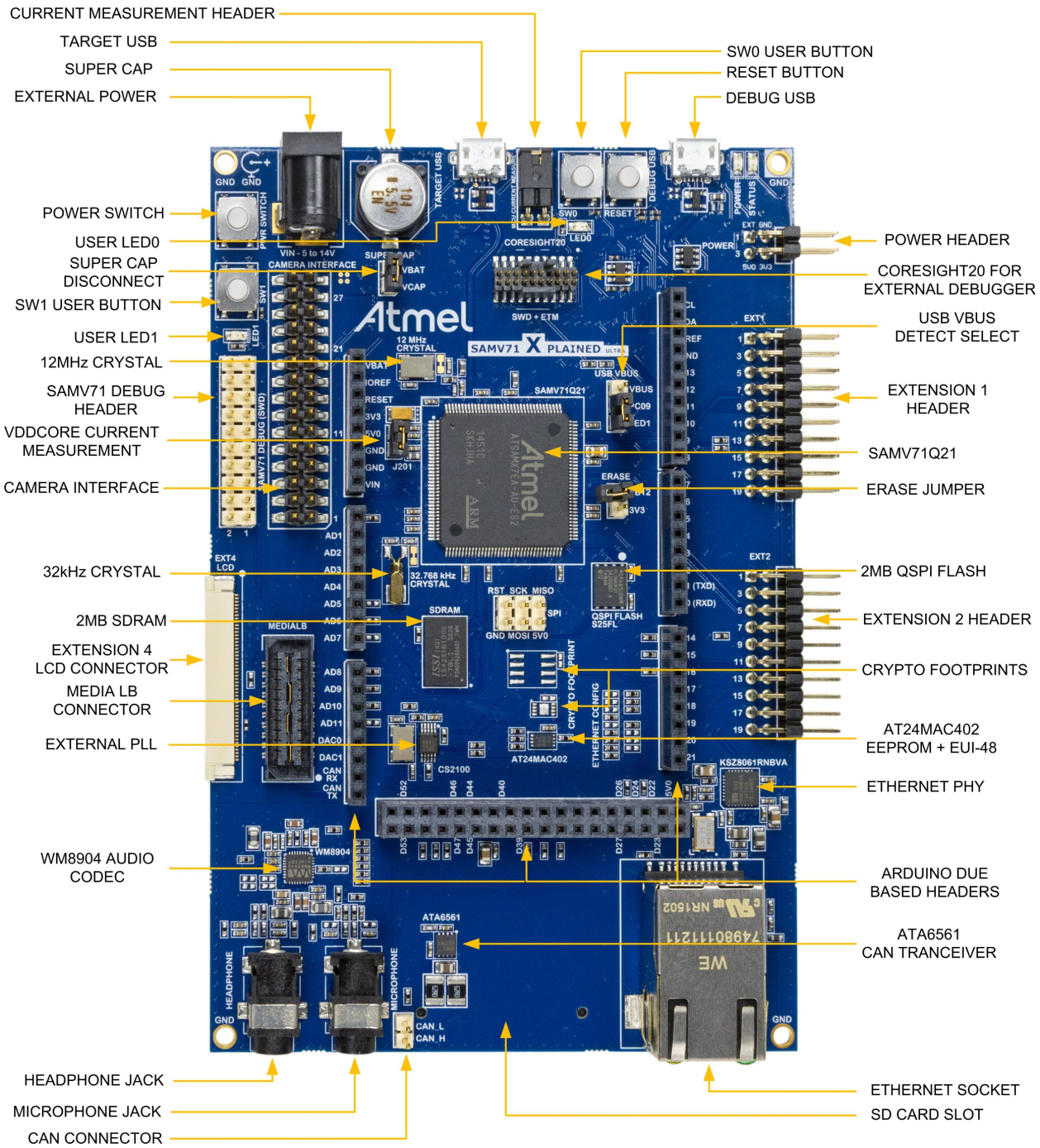
- ATSAMV71Q21 microcontroller
- One mechanical reset button
- One power switch button
- Two mechanical user pushbuttons
- Two yellow user LEDs
- Supercap backup
- 12.0MHz crystal
- 32.768kHz crystal
- 2MB SDRAM
- 2MB QSPI Flash
- Built in Ethernet MAC with external IEEE 802.3az 10Base-T/100Base-TX Ethernet RMII PHY
- AT24MAC402 256KB EEPROM with EUI-48 address
- WM8904 low power stereo audio codec
  - External PLL for precise clock generation
  - Microphone jack
  - Headphone jack
- ATA6561 CAN Transceiver
- SD Card connector with SDIO support
- Camera interface connector
- MediaLB connector
- Two Xplained Pro extension headers
- One Xplained Pro LCD header
- CoreSight 20 connector for 4-bit ETM
- Arduino Due based shield connectors
- External debugger connector
- USB interface, device and host mode
- Embedded Debugger
  - Auto-ID for board identification in Atmel Studio
  - One yellow status LED
  - One green board power LED
  - Symbolic debug of complex data types including scope information
  - Programming and debugging
  - Data Gateway Interface: SPI, I^2C, four GPIOs
  - Virtual COM port (CDC)
- External power input (5-14V)
- USB powered

1.2. Kit Overview

The Atmel SAM V71 Xplained Ultra evaluation kit is a hardware platform to evaluate the Atmel ATSAMV71Q21.

The kit offers a set of features that enables the ATSAMV71Q21 user to get started with the SAM V70 and SAM V71 peripherals right away and to get an understanding of how to integrate the device in their own design.

Figure 1-1 SAM V71 Xplained Ultra Evaluation Kit Overview



2. Getting Started

2.1. SAM V71 Xplained Ultra Quick Start

Three steps to start exploring the Atmel SAM V71 Xplained Ultra:

1. Download Atmel Studio.
2. Launch Atmel Studio.
3. Connect a USB cable (Standard-A to Micro-B or Micro-AB) between the PC and the DEBUG USB port on the kit.

When the Atmel SAM V71 Xplained Ultra is connected to your computer for the first time, the operating system will do a driver software installation. The driver file supports both 32-bit and 64-bit versions of Microsoft® Windows® XP, Windows Vista®, Windows 7, and Windows 8.

Once the kit is powered the green power LED will be lit and Atmel Studio will auto detect the kit and which Xplained Pro extension board(s) are connected. Atmel Studio will present relevant information like datasheets and kit documentation. The SAM V71 device is programmed and debugged by the on-board Embedded Debugger and therefore no external programmer or debugger tool is needed.

2.2. Design Documentation and Relevant Links

The following list contains links to the most relevant documents and software for the SAM V71 Xplained Ultra.

- **Xplained Pro products** - Atmel Xplained Pro is a series of small-sized and easy-to-use evaluation kits for Atmel microcontrollers and other Atmel products. It consists of a series of low cost MCU boards for evaluation and demonstration of features and capabilities of different MCU families.
- **Atmel Studio** - Free Atmel IDE for development of C/C++ and assembler code for Atmel microcontrollers.
- **Atmel sample store** - Atmel sample store where you can order samples of devices.
- **EDBG User Guide** - User guide containing more information about the on-board Embedded Debugger.
- **Atmel Data Visualizer** - Atmel Data Visualizer is a program used for processing and visualizing data. Data Visualizer can receive data from various sources such as the Embedded Debugger Data Gateway Interface found on Xplained Pro boards, and COM ports.
- **IAR Embedded Workbench® for ARM** - This is a commercial C/C++ compiler that is available for ARM. There is a 30 day evaluation version as well as a code size limited kick-start version available from their website. The code size limit is 16KB for devices with M0, M0+, and M1 cores and 32KB for devices with other cores.
- **Keil MDK-ARM Microcontroller Development Kit** - The MDK-ARM is a complete software development environment for Cortex-M, Cortex-R4, ARM7™, and ARM9™ processor-based devices. MDK-ARM is specifically designed for microcontroller applications, it is easy to learn and use, yet powerful enough for the most demanding embedded applications.
- **Design Documentation** - Package containing schematics, BOM, assembly drawings, 3D plots, layer plots etc.
- **Hardware Users Guide in PDF format** - PDF version of this User Guide.

3. Xplained Pro

SAM V71 Xplained Ultra implements several Xplained Pro standards like extension headers and connectors, this chapter documents these standards.

Xplained Pro is an evaluation platform that provides the full Atmel microcontroller experience. The platform consists of a series of Microcontroller (MCU) boards and extension boards that are integrated with Atmel Studio, support data streaming and more. Xplained Pro MCU boards support a wide range of Xplained Pro extension boards that are connected through a set of standardized headers and connectors. Each extension board has an identification (ID) chip to uniquely identify which boards are connected to a Xplained Pro MCU board. This information is used to present relevant user guides, application notes, datasheets, and example code through Atmel Studio.

3.1. Embedded Debugger

The SAM V71 Xplained Ultra contains the Atmel Embedded Debugger (EDBG) for on-board debugging. The EDBG is a composite USB device of three interfaces; a debugger, Virtual COM Port, and a Data Gateway Interface (DGI).

Together with Atmel Studio, the EDBG debugger interface can program and debug the ATSAMV71Q21. On SAM V71 Xplained Ultra, the SWD interface is connected between the EDBG and the ATSAMV71Q21.

The Virtual COM Port is connected to a UART on the ATSAMV71Q21 and provides an easy way to communicate with the target application through terminal software. It offers variable baud rate, parity, and stop bit settings. Note that the settings on the ATSAMV71Q21 must match the settings given in the terminal software.

Note: If not set automatically, data terminal ready (DTR) must be set in the terminal software.

The DGI consists of several physical interfaces for communication with the host computer. Communication over the interfaces is bidirectional. It can be used to send events and values from the ATSAMV71Q21 or as a generic printf-style data channel. Traffic over the interfaces can be timestamped on the EDBG for more accurate tracing of events. Note that timestamping imposes an overhead that reduces maximal throughput. Atmel Data Visualizer is used to send and receive data through DGI.

The EDBG controls two LEDs on SAM V71 Xplained Ultra; a power LED and a status LED. Table 3-1 EDBG LED Control on page 7 shows how the LEDs are controlled in different operation modes.

Table 3-1 EDBG LED Control

Operation Mode	Power LED	Status LED
Normal operation	Power LED is lit when power is applied to the board.	Activity indicator, LED flashes when any communication happens to the EDBG.
Bootloader mode (idle)	The power LED and the status LED blinks simultaneously.	
Bootloader mode (firmware upgrade)	The power LED and the status LED blinks in an alternating pattern.	

For further documentation on the EDBG, see the EDBG User Guide.

3.2. Hardware Identification System

All Xplained Pro compatible extension boards have an Atmel ATSHA204 CryptoAuthentication™ chip mounted. This chip contains information that identifies the extension with its name and some extra data. When an Xplained Pro extension is connected to an Xplained Pro MCU board the information is read and sent to Atmel Studio. The Atmel Kits extension, installed with Atmel Studio, will give relevant information, code examples, and links to relevant documents. Table 3-2 Xplained Pro ID Chip Content on page 8 shows the data fields stored in the ID chip with example content.

Table 3-2 Xplained Pro ID Chip Content

Data field	Data type	Example content
Manufacturer	ASCII string	Atmel'\0'
Product Name	ASCII string	Segment LCD1 Xplained Pro'\0'
Product Revision	ASCII string	02'\0'
Product Serial Number	ASCII string	1774020200000010'\0'
Minimum Voltage [mV]	uint16_t	3000
Maximum Voltage [mV]	uint16_t	3600
Maximum Current [mA]	uint16_t	30

3.3. Power Sources

The SAM V71 Xplained Ultra kit can be powered by several power sources listed in Table 3-3 Power Sources for SAM V71 Xplained Ultra on page 8.

Table 3-3 Power Sources for SAM V71 Xplained Ultra

Power input	Voltage requirements	Current requirements	Connector marking
External power	5V ±2% (±100mV) for USB host operation. 4.3V to 5.5V if USB host operation is not required.	Recommended minimum is 1A to be able to provide enough current for connected USB devices and the board itself. Recommended maximum is 2A due to the input protection maximum current specification.	PWR
Embedded debugger USB	4.4V to 5.25V (according to USB spec.)	500mA (according to USB spec.)	DEBUG USB
Target USB	4.4V to 5.25V (according to USB spec.)	500mA (according to USB spec.)	TARGET USB
External jack input	Kit specific	Kit specific	VIN

The kit will automatically detect which power sources are available and choose which one to use according to the following priority:

1. External jack input.
2. External power.
3. Embedded Debugger USB.
4. Target USB.

Info: External power is required when 500mA from a USB connector is not enough to power the board with possible extension boards. A connected USB device in a USB host application might easily exceed this limit.

3.4. Xplained Pro Headers and Connectors

3.4.1. Xplained Pro Standard Extension Header

All Xplained Pro kits have one or more dual row, 20-pin, 100mil extension header. Xplained Pro MCU boards have male headers, while Xplained Pro extensions have their female counterparts. Note that all pins are not always connected. All connected pins follow the defined pin-out description in Table 3-4 Xplained Pro Standard Extension Header on page 9.

The extension headers can be used to connect a variety of Xplained Pro extensions to Xplained Pro MCU boards or to access the pins of the target MCU on Xplained Pro MCU boards directly.

Table 3-4 Xplained Pro Standard Extension Header

Pin number	Name	Description
1	ID	Communication line to the ID chip on an extension board
2	GND	Ground
3	ADC(+)	Analog to digital converter, alternatively positive part of differential ADC
4	ADC(-)	Analog to digital converter, alternatively negative part of differential ADC
5	GPIO1	General purpose I/O
6	GPIO2	General purpose I/O
7	PWM(+)	Pulse width modulation, alternatively positive part of differential PWM
8	PWM(-)	Pulse width modulation, alternatively negative part of differential PWM
9	IRQ/GPIO	Interrupt request line and/or general purpose I/O
10	SPI_SS_B/ GPIO	Slave select for SPI and/or general purpose I/O
11	I^2C_SDA	Data line for I^2C interface. Always implemented, bus type.

Pin number	Name	Description
12	I^2C_SCL	Clock line for I^2C interface. Always implemented, bus type.
13	UART_RX	Receiver line of target device UART
14	UART_TX	Transmitter line of target device UART
15	SPI_SS_A	Slave select for SPI. Should preferably be unique.
16	SPI_MOSI	Master out slave in line of serial peripheral interface. Always implemented, bus type.
17	SPI_MISO	Master in slave out line of serial peripheral interface. Always implemented, bus type.
18	SPI_SCK	Clock for serial peripheral interface. Always implemented, bus type.
19	GND	Ground
20	VCC	Power for extension board

3.4.2. Xplained Pro LCD Extension Connector

The LCD connector provides the ability to connect to display extensions that have a parallel interface. The connector implements signals for a MCU parallel bus interface and a LCD controller interface as well as signals for a touch controller. The connector pin-out definition is shown in Table 3-5 Xplained Pro LCD Connector on page 10. Note that usually only one display interface is implemented, either the LCD controller or the MCU bus interface.

A FPC/FFC connector with 50 pins and 0.5mm pitch is used for the LCD connector. The connector XF2M-5015-1A from Omron is used on several Xplained Pro designs and can be used as a reference.

Table 3-5 Xplained Pro LCD Connector

Pin number	Name	RGB interface description	MCU interface description
1	ID	Communication line to the ID chip on an extension board	
2	GND	Ground	
3	D0	Data line	
4	D1	Data line	
5	D2	Data line	
6	D3	Data line	
7	GND	Ground	
8	D4	Data line	
9	D5	Data line	
10	D6	Data line	
11	D7	Data line	
12	GND	Ground	
13	D8	Data line	
14	D9	Data line	

Pin number	Name	RGB interface description	MCU interface description
15	D10	Data line	
16	D11	Data line	
17	GND	Ground	
18	D12	Data line	
19	D13	Data line	
20	D14	Data line	
21	D15	Data line	
22	GND	Ground	
23	D16	Data line	
24	D17	Data line	
25	D18	Data line	
26	D19	Data line	
27	GND	Ground	
28	D20	Data line	
29	D21	Data line	
30	D22	Data line	
31	D23	Data line	
32	GND	Ground	
33	PCLK / CMD DATA SEL	Pixel clock	Display RAM select. One address line of the MCU for displays where it is possible to select either register or data interface.
34	VSYNC / CS	Vertical Synchronization	Chip select
35	HSYNC / WE	Horizontal Synchronization	Write enable signal
36	DATA ENABLE / RE	Data enable signal	Read enable signal
37	SPI SCK	Clock for serial peripheral interface	
38	SPI MOSI	Master out slave in of serial peripheral interface	
39	SPI MISO	Master in slave out of serial peripheral interface	
40	SPI SS	Slave select for serial peripheral interface. Preferably a dedicated pin.	
41	ENABLE	Display enable	
42	I^2C SDA	I^2C data	
43	I^2C SCL	I^2C clock	

Pin number	Name	RGB interface description	MCU interface description
44	IRQ1	Interrupt 1	
45	IRQ2	Interrupt 2	
46	PWM	Backlight control	
47	RESET	Extension reset	
48	VCC	3.3V power supply for extension board	
49	VCC	3.3V power supply for extension board	
50	GND	Ground	

3.4.3. Xplained Pro Power Header

The power header can be used to connect external power to the SAM V71 Xplained Ultra kit. The kit will automatically detect and switch to any external power if supplied. The power header can also be used as supply for external peripherals or extension boards. Care must be taken not to exceed the total current limitation of the on-board regulator when using the 3.3V pin.

Table 3-6 Xplained Pro Power Header

Pin number	Pin name	Description
1	VEXT_P5V0	External 5V input
2	GND	Ground
3	VCC_P5V0	Unregulated 5V (output, derived from one of the input sources)
4	VCC_P3V3	Regulated 3.3V (output, used as main power supply for the kit)

4. Hardware Users Guide

4.1. Power Distribution

SAM V71 Xplained Ultra has four power sources as described in Power Sources on page 8. Figure 4-1 Power Supply Block Diagram on page 13 shows a block diagram of the power supply circuitry, the related I/O pins are described in Table 4-1 Power Distribution Signals on page 14.

The kit can be powered from the EDBG USB, Target USB, external 5.0V, and/or a 5-14V DC jack input. The kit will automatically select a source to draw power from.

An on board supercap (100mF) is charged to 3.6V from the kits 5V net. When all external power is removed from the board or the 3.3V regulator is disabled by the application running on the ATSAMV71Q21 the power switch will supply the ATSAMV71Q21 from the supercap. It is intended that the supercap can supply the ATSAMV71Q21 in its low power backup mode.

Info: When the on-board regulator is turned off by the target application in the ATSAMV71Q21, all ICs on the kit are unpowered except the ATSAMV71Q21. Care must be taken to not supply and stray power these ICs through the ATSAMV71Q21s I/O pins.

Figure 4-1 Power Supply Block Diagram

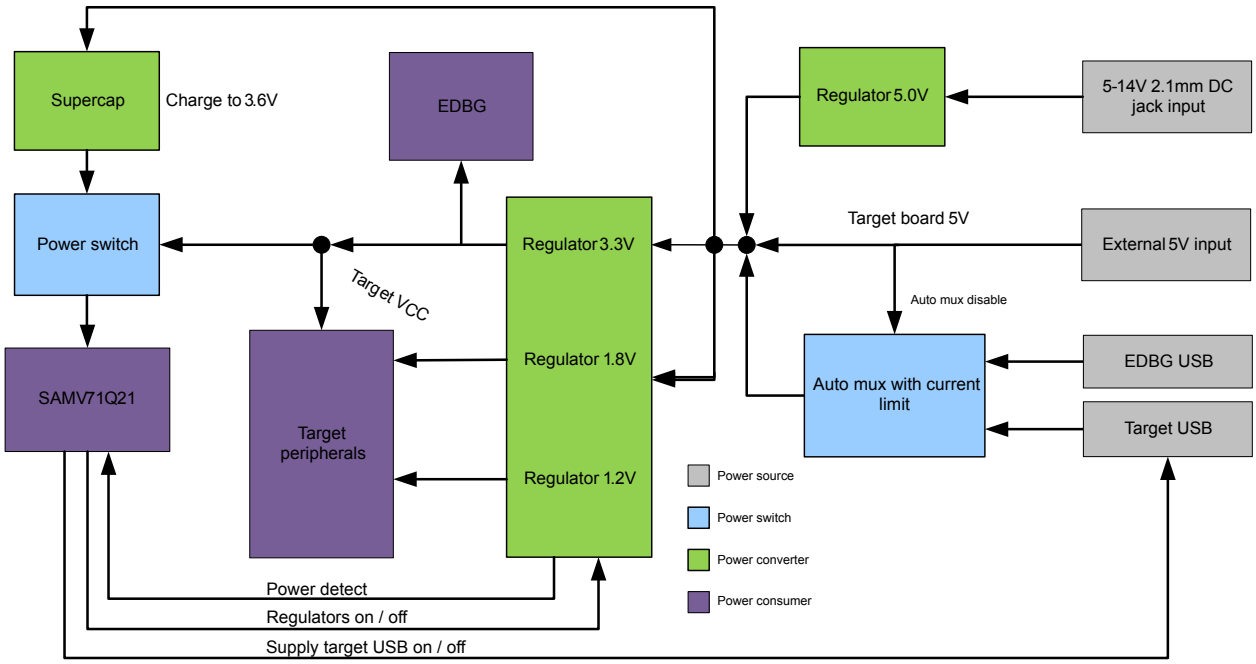


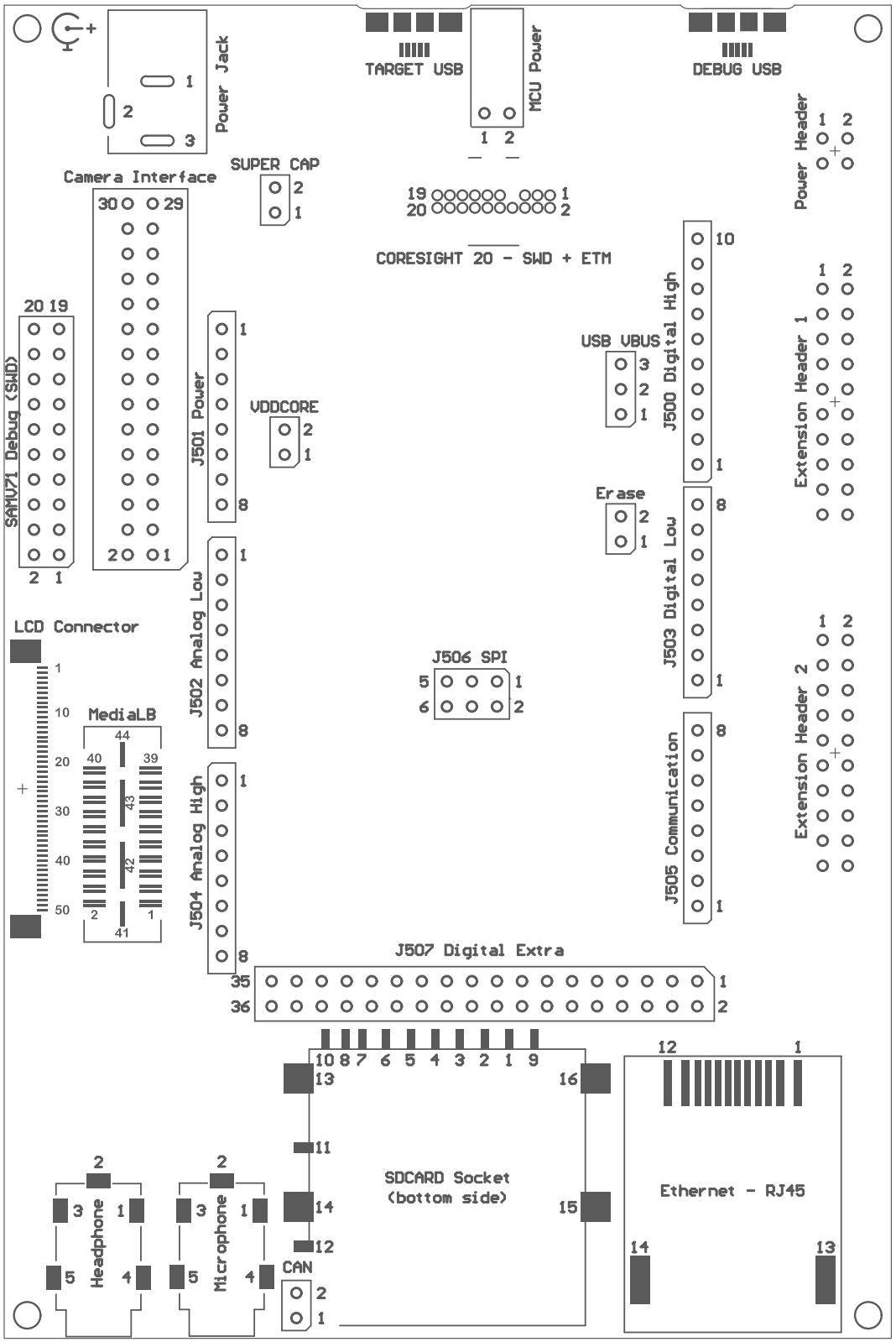
Table 4-1 Power Distribution Signals

SAM V71 pin	Function	Description
PC17	GPIO	Power Enable, drive low to disable the on-board voltage regulator
PA01	WKUP1	Regulator Power Detect, pulled high when the regulator output is good
PC16	GPIO	Drive low to enable the kit to supply the target USB

4.2. Connectors

These sections describes the implementation of the relevant connectors and headers on SAM V71 Xplained Ultra and their connection to the ATSAMV71Q21. The tables of connections in these sections also describes which signals are shared between the headers and on-board functionality. Figure 4-2 SAM V71 Xplained Ultra Connector Overview on page 15 shows all available connectors and jumpers on SAM V71 Xplained Ultra.

Figure 4-2 SAM V71 Xplained Ultra Connector Overview



4.2.1. Extension Headers

The Xplained Pro headers EXT1 and EXT2 on SAM V71 Xplained Ultra offers access to the I/O of the microcontroller in order to expand the board e.g. by connecting extensions to the board. The headers have a pitch of 2.54mm.

Table 4-2 Extension Header EXT1

EXT1 pin	SAM V71 pin	Function	Shared functionality
1 [ID]	-	-	Communication line to the ID chip on an extension board
2 [GND]	-	-	Ground
3 [ADC(+)]	PC31	AFE1_AD6	Shield
4 [ADC(-)]	PA19	AFE0_AD8	Ethernet and Shield
5 [GPIO1]	PB03	GPIO/RTS0	Camera, MediaLB, and Shield(2)
6 [GPIO2]	PB02	GPIO/CTS0	MediaLB and Shield(2)
7 [PWM(+)]	PA00	PWMH0	Shield
8 [PWM(-)]	PC30	TIOB5	LCD
9 [IRQ/GPIO]	PD28	WKUP5	EDBG GPIO, Camera, LCD, and Shield(2)
10 [SPI_SS_B/GPIO]	PA05	GPIO	Camera and Shield
11 [TWI_SDA]	PA03	TWID0	EXT2, EDBG I^2C, LCD, Camera, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield
12 [TWI_SCL]	PA04	TWICK0	EXT2, EDBG I^2C, LCD, Camera, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield
13 [USART_RX]	PB00	RXD0	Audio and Shield(2)
14 [USART_TX]	PB01	TXD0	Audio and Shield(2)
15 [SPI_SS_A]	PD25	SPI0_NPCS1	Camera and Shield
16 [SPI_MOSI]	PD21	SPI0_MOSI	EXT2, EDBG SPI, Audio, Camera, and Shield(2)
17 [SPI_MISO]	PD20	SPI0_MISO	EXT2, EDBG SPI, and Shield(2)
18 [SPI_SCK]	PD22	SPI0_SPCK	EXT2, EDBG SPI, Camera, and Shield(2)
19 [GND]	-	-	Ground
20 [VCC]	-	-	Power for extension board

Table 4-3 Extension Header EXT2

EXT2 pin	SAM V71 pin	Function	Shared functionality
1 [ID]	-	-	Communication line to the ID chip on an extension board
2 [GND]	-	-	Ground
3 [ADC(+)]	PD30	AFE0_AD0	Camera and Shield(2)
4 [ADC(-)]	PC13	AFE1_AD1	LCD and Shield
5 [GPIO1]	PA06	GPIO	Camera, MediaLB, and Shield
6 [GPIO2]	PD11	GPIO	Camera, Audio, and Shield
7 [PWM(+)]	PC19	PWMC0_PWMH2	Camera and Shield
8 [PWM(-)]	PD26	PWMC0_PWML2	Audio and Shield
9 [IRQ/GPIO]	PA02	WKUP2/GPIO	EDBG GPIO, LCD and Shield
10 [SPI_SS_B/GPIO]	PA24	GPIO	Camera and Shield
11 [TWI_SDA]	PA03	TWCK1	EXT1, EDBG I^2C, LCD, Camera, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield
12 [TWI_SCL]	PA04	TWCK0	EXT1, EDBG I^2C, LCD, Camera, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield
13 [USART_RX]	PA21	RXD1	EDBG CDC and Shield
14 [USART_TX]	PB04	TXD1	EDBG CDC, MediaLB and Shield
15 [SPI_SS_A]	PD27	SPI0_NPCS3	Camera and Shield(2)
16 [SPI_MOSI]	PD21	SPI0_MOSI	EXT1, EDBG SPI, Audio, Camera, and Shield(2)
17 [SPI_MISO]	PD20	SPI0_MISO	EXT1, EDBG SPI, and Shield(2)
18 [SPI_SCK]	PD22	SPI0_SPCK	EXT1, EDBG SPI, Camera, and Shield(2)

EXT2 pin	SAM V71 pin	Function	Shared functionality
19 [GND]	-	-	Ground
20 [VCC]	-	-	Power for extension board

4.2.2. LCD Extension Connector

Extension connector EXT4 is a special connector for LCD displays. The physical connector is a TE Connectivity 5-1734839-0 FPC connector.



Info:
Plugging a cable into the LCD connector creates routing stubs for the on-board SDRAM which creates ringing. The ringing will reduce the maximum SDRAM communication frequency. See EBI Signal Integrity on page 43 for more information.

Table 4-4 Xplained Pro LCD Connector EXT4

Pin on EXT4	SAM V71 pin	Function	Shared Functionality
1 [ID]	-	Communication line to ID chip on extension board	-
2 [GND]	-	GND	
3 [D0]	PC00	D0	SDRAM
4 [D1]	PC01	D1	SDRAM
5 [D2]	PC02	D2	SDRAM
6 [D3]	PC03	D3	SDRAM
7 [GND]	-	GND	
8 [D4]	PC04	D4	SDRAM
9 [D5]	PC05	D5	SDRAM
10 [D6]	PC06	D6	SDRAM
11 [D7]	PC07	D7	SDRAM
12 [GND]	-	GND	
13 [D8]	PE00	D8	SDRAM and Shield
14 [D9]	PE01	D9	SDRAM
15 [D10]	PE02	D10	SDRAM
16 [D11]	PE03	D11	SDRAM and Shield
17 [GND]	-	GND	
18 [D12]	PE04	D12	SDRAM and Shield
19 [D13]	PE05	D13	SDRAM and Shield
20 [D14]	PA15	D14	SDRAM
21 [D15]	PA16	D15	SDRAM
22 [GND]	-	GND	
23 [D16]	-	-	
24 [D17]	-	-	
25 [D18]	-	-	
26 [D19]	-	-	
27 [GND]	-	GND	
28 [D20]	-	-	
29 [D21]	-	-	
30 [D22]	-	-	
31 [D23]	-	-	
32 [GND]	-	GND	
33 [PCLK / CMD_DAT A_SEL]	PC30	GPIO	EXT1
34 [VSYNC / CS]	PD19	NCS3	Shield

Pin on EXT4	SAM V71 pin	Function	Shared Functionality
35 [HSYNC / WE]	PC08	NWE	
36 [DAT A ENABLE / RE]	PC11	NRD	
37 [SPI SCK]	-		
38 [SPI MOSI]	-		
39 [SPI MISO]	-		
40 [SPI SS]	-		
41 [DISP ENABLE]	-	100K resistor to VCC_TARGET_P3V3	
42 [TWI SDA]	PA03	TWD0	EXT1, EXT2, EDBG I2C, Camera, Audio, MediaLB, and Shield
43 [TWI SCL]	PA04	TWCK0	EXT1, EXT2, EDBG I2C, Camera, Audio, MediaLB, and Shield
44 [IRQ1]	PD28	WKUP5	EXT1, Camera, and Shield
45 [IRQ2]	PA02	WKUP2	EXT2, EDBG GPIO3, and Shield
46 [PWM]	PC09	TIOB7	LED1 and Shield
47 [RESET]	PC13	GPIO	EXT2 and Shield
48 [VCC]	-	VCC_TARGET_P3V3	
49 [VCC]	-	VCC_TARGET_P3V3	
50 [GND]	-	GND	

4.2.3. Arduino Connectors

SAM V71 Xplained Ultra implements extended Arduino shield connectors based on the Arduino Due. All references to Arduino pin names and pin numbers are taken from the official Arduino pin out list of the Arduino Due.

Caution: Like the Arduino Due, SAM V71 Xplained Ultra runs at 3.3V and the maximum voltage that the I/O pins can tolerate is 3.3V, providing higher voltages like 5V to an I/O pin could damage the board.

Info: Note that all pins on the shield connectors aren't populated, each shield should be checked for compatibility before it is connected.

Table 4-5 J501 - Power

Pin on J501	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	-	RFU	-	VBAT	
2	-	IOREF	-	VCC_TARGET_P3V3	
3	NRST	RESET	-	TARGET_RESET	
4	-	3.3V	-	VCC_TARGET_P3V3	
5	-	5V	-	VCC_P5V0	
6	-	GND	-	GND	
7	-	GND	-	GND	
8	-	VIN	-	VCC_EXT_P5V0_P14V0	

Table 4-6 J502 - Analog Low

Pin on J502	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	PD26	A0	54	TD	Audio and EXT2
2	PC31	A1	55	AFE1_AD6	EXT1
3	PA19	A2	56	AFE0_AD8	Ethernet and EXT1
4	PD30	A3	57	AFE0_AD0	Camera, EXT2, and Shield
5	PC13	A4	58	AFE1_AD1	LCD and EXT2
6	PE00	A5	59	AFE1_AD11	SDRAM and LCD
7	PE03	A6	60	AFE1_AD10	SDRAM and LCD
8	PE04	A7	61	AFE0_AD4	SDRAM and LCD

Table 4-7 J504 - Analog High

Pin on J504	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	PD24	A8	62	RF	Audio and Camera
2	PA10	A9	63	RD	Audio
3	PA22	A10	64	RK	Audio
4	PE05	A11	65	AFE0_AD3	SDRAM and LCD
5	PB13	DAC0	66	DAC0	Camera
6	PD00	DAC1	67	DAC1	Ethernet
7	PB03	CANRX	68	CANRX0 / AFE0_AD2	Camera, MediaLB, EXT1, and Shield
8	PB02	CANTX	69	CANTX0 / AFE0_AD5	MediaLB, EXT1, and Shield

Table 4-8 J503 - Digital Low

Pin on J503	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	PD28	RX0	0	URXD3	Camera, LCD, EXT1, Shield, and EDBG GPIO
2	PD30	TX0	1	UTXD3	Camera, EXT2, and Shield
3	PA00	D2	2	PWMC0_PWMH0	EXT1
4	PA06	D3	3	GPIO	Camera, MediaLB, and EXT2
5	PD27	D4	4	PWMC0_PWML3	Camera, EXT2, and Shield
6	PD11	D5	5	PWMC0_PWMH0	Audio, Camera, and EXT2

Pin on J503	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
7	PC19	D6	6	PWMC0_PWMH2	Camera and EXT2
8	PA02	D7	7	PWMC0_PWMH1	MediaLB, LCD, EXT2, and EDBG GPIO

Table 4-9 J500 - Digital High

Pin on J500	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	PA05	D8	8	PWMC1_PWML3	Camera and EXT1
2	PC09	D9	9	TIOB7	LED1 and LCD
3	PD25	D10	10	PWMC0_PWML1 / SPI0_NPCS1	Camera and EXT1
4	PD21	D11	11	PWMC0_PWMH1 / SPI0_MOSI	PLL, Camera, EXT1, EXT2, Shield, and EDBG SPI
5	PD20	D12	12	PWMC0_PWMH0 / SPI0_MISO	EXT1, EXT2, Shield, and EDBG SPI
6	PD22	D13	13	PWMC0_PWMG2 / SPI0_SPCK	Camera, EXT1, EXT2, Shield, and EDBG SPI
7	-	GND	-	-	-
8	ADVREF	AREF	-	ADVREFP	-
9	PA03	SDA1	70	TWD0	PLL, Audio, Camera, LCD, EXT1, EXT2, Crypto, and EDBG I^2C
10	PA04	SCL1	71	TWCK0	PLL, Audio, Camera, LCD, EXT1, EXT2, Crypto, and EDBG I^2C

Table 4-10 J506 - SPI

Pin on J506	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	PD20	MISO	74	SPI0_MISO	EXT1, EXT2, Shield, and EDBG SPI
2	-	5V	-	VCC_P5V0	-
3	PD22	SCLK	76	SPI0_SPCK	Camera, EXT1, EXT2, Shield, and EDBG SPI
4	PD21	MOSI	75	SPI0_MOSI	PLL, Camera, EXT1, EXT2, Shield, and EDBG SPI

Pin on J506	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
5	NRST	RESET	-	RESET	Trace and EDBG Debug
6	-	GND	-	GND	-

Table 4-11 J505 - Communication

Pin on J505	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	PD28	SCL	21	TWCK2	Camera, LCD, EXT1, Shield, and EDBG GPIO
2	PD27	SDA	20	TWD2	Camera, EXT2, and Shield
3	PD18	RX1	19	URXD4	SD Card and Shield
4	PD19	TX1	18	UTXD4	LCD and Shield
5	PD15	RX2	17	RXD2	SDRAM
6	PD16	TX2	16	TXD2	SDRAM
7	PB00	RX3	15	RXD0	Audio, EXT1, and Shield
8	PB01	TX3	14	TXD0	Audio, EXT1, and Shield

Table 4-12 J507 - Digital Extra

Pin on J507	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
1	-	5V	-	VCC_P5V0	-
2	-	5V	-	VCC_P5V0	-
3	PA18	D22	22	PCK2	Audio
4	PB01	D23	23	TK	Audio, EXT1, and Shield
5	PB00	D24	24	TF	Audio, EXT1, and Shield
6	-	D25	25	-	-
7	PD19	D26	26	CTS2	LCD and Shield
8	PD18	D27	27	RTS2	SD Card and Shield
9	-	D28	28	-	-
10	-	D29	29	-	-
11	-	D30	30	-	-
12	-	D31	31	-	-
13	-	D32	32	-	-
14	-	D33	33	-	-
15	-	D34	34	-	-

Pin on J507	SAM V71 pin	Arduino pin name	Arduino pin number	Function	Shared functionality
16	-	D35	35	-	-
17	-	D36	36	-	-
18	-	D37	37	-	-
19	-	D38	38	-	-
20	PB02	D39	39	CTS0	MediaLB and EXT1
21	PB03	D40	40	RTS0	Camera, MediaLB, and EXT1
22	-	D41	41	-	-
23	-	D42	42	-	-
24	-	D43	43	-	-
25	PA25	D44	44	CTS1	SD Card
26	PA24	D45	45	RTS1	Camera and EXT2
27	PA21	D46	46	RXD1	EXT2 and EDBG CDC
28	PB04	D47	47	TXD1	MediaLB, EXT2, and EDBG CDC
29	-	D48	48	-	-
30	-	D49	49	-	-
31	-	D50	50	-	-
32	-	D51	51	-	-
33	PC12	D52	52	CANRX1	CAN
34	PC14	D53	53	CANTX1	CAN
35	-	GND	-	GND	-
36	-	GND	-	GND	-

4.2.4. MediaLB Connector

Media Local Bus (MediaLB) is an on-PCB or inter-chip communications bus, specifically designed to standardize a common hardware interface and software API library. This standardization allows an application or multiple applications to access the MOST® (Media Oriented Systems Transport) Network data, or to communicate with other applications, with minimum effort.

On SAM V71 Xplained Ultra the MLB module of the ATSAMV71Q21 is connected to a MediaLB connector implemented with a 40 pin SAMTEC *QSH-020-01-L-D-DP-A*. This connector is intended to interface with a board that includes the MOST INIC and the MOST-50 physical layer connector (such as a Physical+ Interface Board OS81092 ePhy) or with other MOST tools. Table 4-13 MediaLB Connector on page 23 shows all connections between the ATSAMV71Q21 and the connector.

Info: To use the MediaLB connector with an external kit that requires 12V, a 12V supply must be connected to the power jack.

Table 4-13 MediaLB Connector

Pin number	SAM V71 Pin	Function	Shared functionality
1 [RESERVED]	-	-	
2 [MLB CLK]	PB04	MLBCLK	EXT2, Shield, and EDBG CDC
3 [RESERVED]	-	-	
4 [MLB_ID0]	-	-	
5 [MLB_ID4]	-	-	
6 [MLBSIG]	PD10	MLBSIG	
7 [MLB_ID3]	-	-	
8 [MLB_ID1]	-	-	
9 [SCK]	-	-	
10 [MLBDAT]	PB05	MLBDAT	EDBG Debug
11 [FSY]	-	-	
12 [MLB_ID2]	-	-	
13 [RESERVED]	-	-	
14 [SX0]	-	-	
15 [RESERVED]	-	-	
16 [RMCK]	PA02	RMCK	LCD, EXT2, Shield, and EDBG GPIO3
17 [RESERVED]	-	-	
18 [SR0]	-	-	
19 [RESERVED]	-	-	
20 [RESERVED]	-	-	
21 [PS0]	-	-	
22 [PS1]	-	-	
23 [STATUS]	-	-	
24 [PWROFF]	-	-	
25 [RESET_N]	PA06	GPIO	Camera, EXT2, and Shield
26 [RSOUT]	-	-	

Pin number	SAM V71 Pin	Function	Shared functionality
27 [ERR/BOOT]	PB03	GPIO	Camera, EXT1, and Shield (2)
28 [MCK_IN]	-	-	
29 [TCK/DSCL]	-	-	
30 [TMS]	-	-	
31 [TDO/DINT]	-	-	
32 [TDI/DSDA]	-	-	
33 [I2C_SCL]	PA04	TWCK0	EXT1, EXT2, EDBG I2C, LCD, Audio, PLL, Camera, EEPROM, Crypto, and Shield
34 [MLB_INT]	PB02	GPIO	EXT1, Shield (2)
35 [I2C_SDA]	PA03	TWD0	EXT1, EXT2, EDBG I2C, LCD, Audio, PLL, Camera, EEPROM, Crypto, and Shield
36 [RESERVED]	-	-	
37 [3V3_SWITCHED]	-	-	
38 [3V3_CONTINOUS]	-	-	
39 [3V3_SWITCHED]	-	-	
40 [12V0_CONTINOUS]	-	-	

4.2.5. Camera Connector

A 2x15, 100mil pin-header camera connector is implemented to give access to the SAM V71's parallel Image Sensor Interface (ISI).

Table 4-14 Camera Connector

Pin number	SAM V71 pin	Function	Shared functionality
1 [VCC]	-	VCC_TARGET_P3V3	
2 [GND]	-	GND	
3 [VCC]	-	VCC_TARGET_P3V3	
4 [GND]	-	GND	
5 [RESET]	PB13	GPIO	Shield
6 [PWD]	PC19	ISI_PWD	EXT2 and Shield
7 [I2C_SCK]	PA04	TWCK0	EXT1, EXT2, EDBG I2C, LCD, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield

Pin number	SAM V71 pin	Function	Shared functionality
8 [I2C_SDA]	PA03	TWD0	EXT1, EXT2, EDBG I²C, LCD, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield
9 [GND]	-	GND	
10 [MCK]	PA06	PCK0	EXT2, MediaLB, and Shield
11 [GND]	-	GND	
12 [VSYNC]	PD25	ISI_VSYNC	EXT1 and Shield
13 [GND]	-	GND	
14 [HSYNC]	PD24	ISI_HSYNC	Audio and Shield
15 [GND]	-	GND	
16 [PCK]	PA24	ISI_PCK	EXT2 and Shield
17 [GND]	-	GND	
18 [D0]	PD22	ISI_D0	EXT1, EXT2, EDBG SPI, and Shield (2)
19 [D1]	PD21	ISI_D1	EXT1, EXT2, EDBG SPI, Audio, and Shield (2)
20 [D2]	PB03	ISI_D2	EXT1, MediaLB, and Shield (2)
21 [D3]	PA09	ISI_D3	EDBG GPIO and SW0
22 [D4]	PA05	ISI_D4	EXT1 and Shield
23 [D5]	PD11	ISI_D5	EXT2, Audio, and Shield
24 [D6]	PD12	ISI_D6	EDBG SPI
25 [D7]	PA27	ISI_D7	SD Card
26 [D8]	PD27	ISI_D8	EXT2 and Shield (2)
27 [D9]	PD28	ISI_D9	EXT1, EDBG GPIO, LCD, and Shield (2)
28 [D10]	PD30	ISI_D10	EXT2 and Shield (2)
29 [D11]	PD31	ISI_D11	QSPI Flash
30 [GND]	-	GND	

4.2.6. USB

The SAM V71 Xplained Ultra has a Micro-USB connector for use with the SAM V71 USB module labeled as TARGET USB on the kit. In USB host mode VBUS voltage is provided by the kit and has to be enabled by setting the "VBUS Host Enable" pin low.

Table 4-15 USB Connections

Pin on SAM V71	USB function
PC16	VBUS Host Enable (Active low)
HSDM	USB D-
HSDP	USB D+

There is a 1x3, 100mil pin-header marked VBUS on the kit. PC09 on the SAM V71 can be connected to either LED1 or to the target USB VBUS DETECT signal by placing a jumper between pin 1 and 2, or pin 2 and 3 respectively on this pin-header.

USB VBUS DETECT is the target USB voltage divided by 1.64, when connected to the PC09 pin the signal can be used to detect power on the target USB connector.

Table 4-16 USB VBUS Selection

Pin	Function
1	LED1
2	PC09
3	USB VBUS DETECT

4.2.7. Super Capacitor

There is a 1x2, 100mil pin-header on the kit that can be used to connect/disconnect the super capacitor from the voltage backup system marked "SUPER CAP". The capacitor is connected by default with the jumper that is mounted on this pin-header. To disconnect the super capacitor remove the jumper.

Table 4-17 Super Capacitor

Pin	Function	Description
1	V_SUPERCAP	Connected directly to the positive pin of the capacitor
2	VBAT	VBAT input to the power switch

4.2.8. Current Measurement Header

An angled 1x2, 100mil pin-header marked with MCU current measurement is located at the upper edge of the SAM V71 Xplained Ultra. All power to the ATSAMV71Q21 is routed through this header. To measure the power consumption of the device remove the jumper and replace it with an ammeter.



Caution: Removing the jumper from the pin-header while the kit is powered may cause the ATSAMV71Q21 to be powered through its I/O pins. This may cause permanent damage to the device.

4.2.9. VDDCORE Current Measurement

A 1x2, 100mil pin-header marked with J201 is located at the center of the SAM V71 Xplained Ultra. All power to VCCDORE of the ATSAMV71Q21 is routed through this header. To measure the power consumption of VDDCORE remove the jumper and replace it with an ampere meter.

Caution: Removing the jumper from the pin-header while the kit is powered will power all power pins on the ATSAMV71Q21 except VDDCORE. This may cause permanent damage to the device.

4.2.10. Chip Erase Header

There is a 1x2 pin-header that is connected to the SAM V71 chip erase pin, PB12, and 3V3 marked ERASE. This header can be used to chip erase the SAM V71 by placing jumper on the header and toggle power to the board. After the power is toggled the jumper should be removed. Using the chip erase jumper may be the only way to erase a chip with the security bit set, and applications that immediately sets invalid clock options or goes into deep sleep without any wake-up sources enabled.

4.2.11. Trace Connector

ATSAMV71Q21 supports 4-bit parallel trace. SAM V71 Xplained Ultra implements a CoreSight 20 20-pin, 50-mil keyed connector (pin seven is removed).

To use the trace functionality an external debugger with trace support and CoreSight 20 pin out has to be used. Table 4-18 CoreSight 20 Trace Connector on page 27 shows the connections on the kit.

Info: Several of the trace signals are shared with Ethernet signals, this means that there is no trace support if Ethernet is used in an application.

Table 4-18 CoreSight 20 Trace Connector

Pin number	SAM V71 pin	Function	Shared functionality
1 [VTREF]	-	VCC_TARGET_P3V3	
2 [TMS/SWDIO]	PB06	SWDIO	EDBG SWD
3 [GND]	-	Ground	
4 [TCK/SWCLK]	PB07	SWCLK	EDBG SWD
5 [GND]	-	Ground	
6 [TDO/SWO]	PB05	TRACESWO	MediaLB and EDBG SWD
7 [KEY]	-	-	
8 [TDI]	-	-	
9 [GND]	-	Ground	
10 [nSRST]	NRST	NRST	Shield and EDBG
11 [NC]	-	-	
12 [RTCK/TRACECLK]	PD08	TRACECLK	Ethernet
13 [NC]	-	-	
14 [SWO/D0]	PD04	TRACED0	Ethernet
15 [GND]	-	Ground	

Pin number	SAM V71 pin	Function	Shared functionality
16 [ntRST/D1]	PD05	TRACED1	Ethernet
17 [GND]	-	Ground	
18 [DBGRQ/D2]	PD06	TRACED2	Ethernet
19 [GND]	-	Ground	
20 [DBGACK/D3]	PD07	TRACED3	Ethernet

4.3. Peripherals

4.3.1. Crystals

The SAM V71 Xplained Ultra kit contains two crystals that can be used as clock sources for the SAM V71 device. The crystals have cut-straps next to them that can be used to measure the oscillator safety factor. This is done by cutting the strap and adding a resistor across the strap. Information about oscillator allowance and safety factor can be found in the Atmel application note AVR4100, information about clock calibration and compensation can be found in the Atmel application note AT03155.

Table 4-19 External 32.768kHz Crystal

SAM V71 pin	Function
PA07	XIN32
PA08	XOUT32

Table 4-20 External 12MHz Crystal

SAM V71 pin	Function
PB09	XIN
PB08	XOUT

Info: The 12MHz crystal selected for the SAM V71 Xplained Ultra evaluation kit has a load capacitance outside the specification from the ATSAMV71Q21 datasheet, see the errata section for more information.

Related Links

12MHz Crystal Selection on page 44

4.3.2. Mechanical Buttons

SAM V71 Xplained Ultra contains three mechanical buttons. One button is the RESET button connected to the SAM V71 reset line and the others are generic user configurable buttons. When a button is pressed it will drive the I/O line to GND.

Info: There are no pull-up resistors connected to the generic user buttons, remember to enable the internal pull-up in the SAM V71 to use the button.

Info: PB12 is set up as a system flash ERASE pin when the firmware boots. To use the SW1, PB12 has to be configured as a normal regular I/O pin in the MATRIX module. For more information, see the SAM V71 datasheet.

Table 4-21 Mechanical Buttons

SAM V71 pin	Function	Shared functionality
RESET	RESET	Trace, Shield, and EDBG
PA09	SW0	EDBG GPIO and Camera
PB12	SW1	EDBG SWD and Chip Erase

4.3.3. LEDs

There are two yellow LEDs available on the SAM V71 Xplained Ultra board that can be turned on and off. The LEDs can be activated by driving the connected I/O line to GND.

Table 4-22 LED Connection

SAM V71 pin	Function	Shared functionality
PA23	Yellow LED0	EDBG GPIO
PC09	Yellow LED1	LCD and Shield

4.3.4. SDRAM

SAM V71 Xplained Ultra features one external IS42S16100E-7BLI, 512Kx16x2, 144MHz, SDRAM. The SDRAM is connected to chip select NCS1. SDRAM access can be configured in the SDRAM Controller in the SAM V71. Table 4-23 SDRAM Connections on page 29 lists all I/O-lines connected to the SDRAM.

Info:
Due to the maximum communication speed of 144MHz in the on-board SDRAM and stubs created by the routing to the LCD connector (EXT4), the SDRAM is accessible up to 133MHz with the GPIO configured in low-drive mode. With GPIO configured as high drive or with a cable connected to the LCD connector the maximum communication speed is lowered further. See EBI Signal Integrity on page 43 for more information.

Table 4-23 SDRAM Connections

SAM V71 pin	Function	SDRAM function	Shared functionality
PC00	D0	Data line 0	LCD
PC01	D1	Data line 1	LCD
PC02	D2	Data line 2	LCD
PC03	D3	Data line 3	LCD
PC04	D4	Data line 4	LCD
PC05	D5	Data line 5	LCD
PC06	D6	Data line 6	LCD

SAM V71 pin	Function	SDRAM function	Shared functionality
PC07	D7	Data line 7	LCD
PE00	D8	Data line 8	LCD and Shield
PE01	D9	Data line 9	LCD
PE02	D10	Data line 10	LCD
PE03	D11	Data line 11	LCD and Shield
PE04	D12	Data line 12	LCD and Shield
PE05	D13	Data line 13	LCD and Shield
PA15	D14	Data line 14	LCD
PA16	D15	Data line 15	LCD
PC20	A2	Address line 0	
PC21	A3	Address line 1	
PC22	A4	Address line 2	
PC23	A5	Address line 3	
PC24	A6	Address line 4	
PC25	A7	Address line 5	
PC26	A8	Address line 6	
PC27	A9	Address line 7	
PC28	A10	Address line 8	
PC29	A11	Address line 9	
PD13	SDA10	Address line 10	
PA20	BA0	Bank select line 0	
PD23	SDCK	Clock	
PD14	SDCKE	Clock Enable	
PC15	SDCS	Chip Select	
PD16	RAS	RAS	Shield
PD17	CAS	CAS	
PD29	SDWE	Write Enable	
PC18	A0/NBS0	LDQM	
PD15	NWR1/ NBS1	UDQM	Shield

4.3.5. QSPI Flash

The SAM V71 Xplained Ultra features one external SPANSION, S25FL116K, 2MB, QSPI Flash. QSPI Slash access can be configured in the QSPI module in the SAM V71. Table 4-24 QSPI Flash Connections on page 31 lists all I/O-lines connected to the QSPI Flash.

Table 4-24 QSPI Flash Connections

SAM V71 pin	Function	QSPI Flash function	Shared functionality
PA13	QIO0	Slave In/IO0	
PA12	QIO1	Slave Out/IO1	
PA17	QIO2	Write Protect/IO2	
PD31	QIO3	Hold/IO3	Camera
PA14	QSCK	Clock	
PA11	QCS	Chip Select	

4.3.6. SD Card

The SAM V71 Xplained Ultra has one standard SD card connector which is connected to High Speed Multimedia Card Interface (HSMCI) of the SAM V71. Table 4-25 SD Card Connection on page 31 lists all I/O-lines connected to the SD card connector.

Table 4-25 SD Card Connection

SAM V71 pin	Function	Shared functionality
PA30	MCDA0 (DAT0)	
PA31	MCDA1 (DAT1)	
PA26	MCDA2 (DAT2)	
PA27	MCDA3 (DAT3)	Camera
PA25	MCCK (CLK)	Shield
PA28	MCCDA (CMD)	
PD18	Card Detect (C/D)	Shield, (2)

4.3.7. Ethernet

ATSAMV71Q21 has a built in 10/100Mbps Ethernet IEEE® 802.3 compatible MAC with RMII and MII interface. The MAC also supports energy efficient Ethernet (IEEE 802.3az) and Ethernet Audio Video Bridging (AVB) including IEEE 802.1AS and IEEE802.1Qav. SAM V71 Xplained Ultra connects the MAC to a Micrel *KSZ8061RNBVA* RMII physical-layer transceiver (PHY), with IEEE 802.3az support, which is connected to one RJ45 Ethernet connector.

A unique EUI-48 address is available on every SAM V71 Xplained Ultra through the on-board AT24MAC402, the EUI-48 address can be used as a MAC address for the *KSZ8061RNBVA*. The address is also programmed into the on board EDBG. For more information, see Kit Specific Data on page 42.

Table 4-26 KSZ8061RNBVA Connections on page 32 lists all pins connected from the ATSAMV71Q21 to the Ethernet PHY.

Info: Several of the Ethernet signals are shared with the trace connector, this means that there is no Ethernet support if trace is used in an application.

Table 4-26 KSZ8061RNBVA Connections

SAM V71 pin	Function	Ethernet function	Shared functionality
PD00	GTXCK	REF_CLK	Shield
PD01	GTXEN	TXEN	
PD02	GTX0	TXD0	
PD03	GTX1	TXD1	
PD04	GRXDV	CRS_DV	Trace
PD05	GRX0	RXD0	Trace
PD06	GRX1	RXD1	Trace
PD07	GRXER	RXER	Trace
PD08	GMDC	MDC	Trace
PD09	GMDIO	MDIO	
PA19	GPIO	INTERRUPT	EXT1, Shield
PA29	GPIO	SIGDET	
PC10	GPIO	RESET	

The *KSZ8061RNBVA* also has a set of parameters that are latched in during reset based on I/O pin levels, these configuration options have a default mode on the kit done by external pull-up and pull-down resistors. For detailed information about the configuration see the *KSZ8061RNBVA* datasheet.

Table 4-27 KSZ8061RNBVA kit configuration

Configuration name	Default value on kit	Default configuration
PHYAD	001	The PHYs address is 001
CONFIG	111	RMII mode with MDI/MDI-X enabled
AUTONEG	0	Auto negotiation of link speed enabled
NAND_TREE	1	NAND TREE test mode disabled
QWF	0	Quiet-WIRE filtering enabled

4.3.8. AT24MAC402

The SAM V71 Xplained Ultra features one external AT24MAC402 serial EEPROM with a EIA-48 MAC address connected to the SAM V71 through I^2C. This device contain a MAC address for use with the Ethernet interface. Table 4-28 AT24MAC402 Connections on page 33 lists all I/O-lines connected to the ATMAC402 device.

Table 4-28 AT24MAC402 Connections

SAM V71 pin	Function	QSPI Flash function	Shared functionality
PA03	TWID0	SDA	EXT1, EXT2, EDBG I²C, LCD, Camera, Audio, MediaLB, and Shield
PA04	TWICK0	SCL	EXT1, EXT2, EDBG I²C, LCD, Camera, Audio, MediaLB, and Shield

4.3.9. CAN

SAM V71 Xplained Ultra has two MCAN modules that performs communication according to ISO11898-1 (Bosch CAN specification 2.0 part A,B) and Bosch CAN FD specification V1.0.

MCAN1 is connected to an on-board ATA6561 CAN physical-layer transceiver, Table 4-29 ATA6561 Connections on page 33 shows connections between the ATSAMV71Q21 and the ATA6561.

Table 4-29 ATA6561 Connections

SAM V71 pin	Function	ATA6561 function	Shared functionality
PC14	CANTX1	TXD	Shield
PC12	CANRX1	RXD	Shield

4.3.10. Audio and External PLL

SAM V71 Xplained Ultra includes a WOLFSON *WM8904* Audio CODEC for input and output of digital sound, the kit has two 3.5mm stereo jacks for microphone input and headphone output. There is also an (optional) external PLL, Cirrus Logic *CS2100CP*, that can be used to generate a reference clock to the *WM8904*. In an Ethernet AVB application, the *CS2100CP* PLL can be used to accurately reconstruct a media clock that is generated at a remote network node.

The *WM8904* is configured through I²C while audio data is transferred via the SSC module in the SAM V71. The CS2100CP PLL is also configured through I²C, and the input clock reference is from PD21 which is internally connected to the timer unit of the Ethernet MAC in the ATSAMV71Q21.

Table 4-30 *WM8904* Connections

SAM V71 pin	Function	Audio function	Shared functionality
PA03	TWD0	I²C control interface, data line	EXT1, EXT2, EDBG I²C, LCD, Camera, PLL, MediaLB, EEPROM, Crypto, and Shield
PA04	TWCK0	I²C control interface, clock line	EXT1, EXT2, EDBG I²C, LCD, Camera, PLL, MediaLB, EEPROM, Crypto, and Shield
PA10	RD, receiver data	ADCDAT, digital audio output (microphone)	Shield
PA18	PCK2	MCLK, master clock	Shield

SAM V71 pin	Function	Audio function	Shared functionality
PB00	TF, transmitter frame synchronization	LRCLK left/right data alignment clock	EXT1 and Shield (2)
PB01	TK, transmitter clock	BCLK, bit clock, for synchronization	EXT1 and Shield (2)
PD11	GPIO	Interrupt from Audio CODEC	Camera, EXT2, and Shield
PD24	RF, receiver frame synchronization	LRCLK, left/right data alignment clock	Audio, Camera, and Shield
PD26	TD, transmitter data	DACDAT, digital audio input (headphone)	EXT2 and Shield

Table 4-31 *CS2100CP* Connections

SAM V71 pin	Function	Audio function	Shared functionality
PA03	TWD0	I^2C control interface, data line	EXT1, EXT2, EDBG I^2C, LCD, Camera, Audio, MediaLB, EEPROM, Crypto, and Shield
PA04	TWCK0	I^2C control interface, data line	EXT1, EXT2, EDBG I^2C, LCD, Camera, Audio, MediaLB, EEPROM, Crypto, and Shield
PD21	TIOA11	REFCLK, PLL input	Camera, EXT1, EXT2, EDBG SPI, and Shield (2)
PA22	RK, receiver clock	PLL output	Shield

4.3.11. Crypto Footprint

Several of Atmels security devices, including CryptoAuthentication devices like the ATSAH204A, only requires I^2C to interface and they share the same packages and pinouts. SAM V71 Xplained Ultra has implemented SOIC8 and UDFN8 footprints for these devices so the user may solder them on themselves. Table 4-32 Crypto Footprints on page 34 shows all connections between the footprint and the ATSAMV71Q21.

Table 4-32 Crypto Footprints

Pin on footprint	SAM V71 pin	Function	Shared functionality
1	-	NC	
2	-	NC	
3	-	NC	
4	-	GND	

Pin on footprint	SAM V71 pin	Function	Shared functionality
5	PA03 [TWD0]	I²C data line	EXT1, EXT2, EDBG I²C, LCD, Camera, Audio, PLL, MediaLB, EEPROM, and Shield
6	PA04 [TWCK0]	I²C clock line	EXT1, EXT2, EDBG I²C, LCD, Camera, Audio, PLL, MediaLB, EEPROM, and Shield
7	-	NC	
8	-	VCC_TARGET_P3V3	
PADDLE	-	GND	

4.4. Zero Ohm Resistors

SAM V71 Xplained Ultra has several zero ohm resistors that can be used to disconnect I/O pins of the ATSAMV71Q21 from connectors and on-board ICs and to disconnect power signals. All Arduino pin numbers are listed in Arduino Connectors on page 18. Table 4-33 Zero Ohm Resistors on page 35 lists all zero ohm resistors on the kit. Figure 4-3 Zero Ohm Resistors Top on page 38 and Figure 4-4 Zero Ohm Resistors Bottom on page 39 shows where they are located.

Info: Note from Table 4-33 Zero Ohm Resistors on page 35 that there are some zero ohm resistors that aren't mounted by default on the kit.

Table 4-33 Zero Ohm Resistors

Designator	Mounted	From	To	Comment
R100	Yes	VCC_P3V3	VCC_TARGET_P3V3	
R109	Yes	V_SUPERCAP	U101_8	Supercap voltage to U101
R112	**No**	U101_8	Arduino VBAT pin	Power, J501 pin 1
R200	Yes	PD11	Audio IRQ	
R201	Yes	PB00	EXT1 pin 13	
R202	Yes	PB01	EXT1 pin 14	
R203	Yes	PD28	LCD connector pin 44	IRQ1
R207	Yes	PB01	Arduino pin 14	Communication, J505
R208	Yes	PB00	Arduino pin 15	Communication, J505

Designator	Mounted	From	To	Comment
R209	Yes	PD26	EXT2 pin 8	
R211	Yes	PB01	Arduino pin 23	Digital Extra, J507
R213	Yes	PB00	Arduino pin 24	Digital Extra, J507
R215	Yes	PD26	Arduino pin 54	Analog low, J502
R216	**No**	PE00	Arduino pin 59	Analog low, J502
R217	**No**	PE03	Arduino pin 60	Analog low, J502
R218	**No**	PE04	Arduino pin 61	Analog low, J502
R219	Yes	PD24	Arduino pin 62	Analog high, J504
R220	Yes	PA10	Arduino pin 63	Analog high, J504
R221	Yes	PA22	Arduino pin 64	Analog high, J504
R222	**No**	PE05	Arduino pin 65	Analog high, J504
R223	Yes	PD24	Audio RF	
R224	Yes	PB01	Audio TK	
R225	Yes	PA22	Audio RK	
R226	Yes	PB00	Audio TF	
R228	Yes	PA10	Audio RD	
R229	Yes	PD26	Audio TD	
R230	Yes	PD21	PLL clock input	
R234	Yes	PD16	Arduino pin 16	Communication, J505
R400	Yes	PB06 (SWDIO)	ARM JTAG	
R401	Yes	PB07 (SWCLK)	ARM JTAG	
R402	Yes	RESET	ARM JTAG	
R403	Yes	PB05 (TRACESWO)	ARM JTAG	
R800	Yes	Audio	Headphone jack	
R802	Yes	Audio	Headphone jack	
R806	Yes	Microphone jack	Audio	
R811	Yes	Microphone jack	Audio	
R814	Yes	GND	Audio GND	
R815	Yes	GND	Audio GND	
R816	Yes	GND	Audio GND	
R818	Yes	GND	PLL AD0	I^2C address select

Designator	Mounted	From	To	Comment
R819	Yes	VCC_P1V8	Audio DCVDD	
R920	Yes	VCC_P3V3	VCC_EDBG_P3V3	

Figure 4-3 Zero Ohm Resistors Top

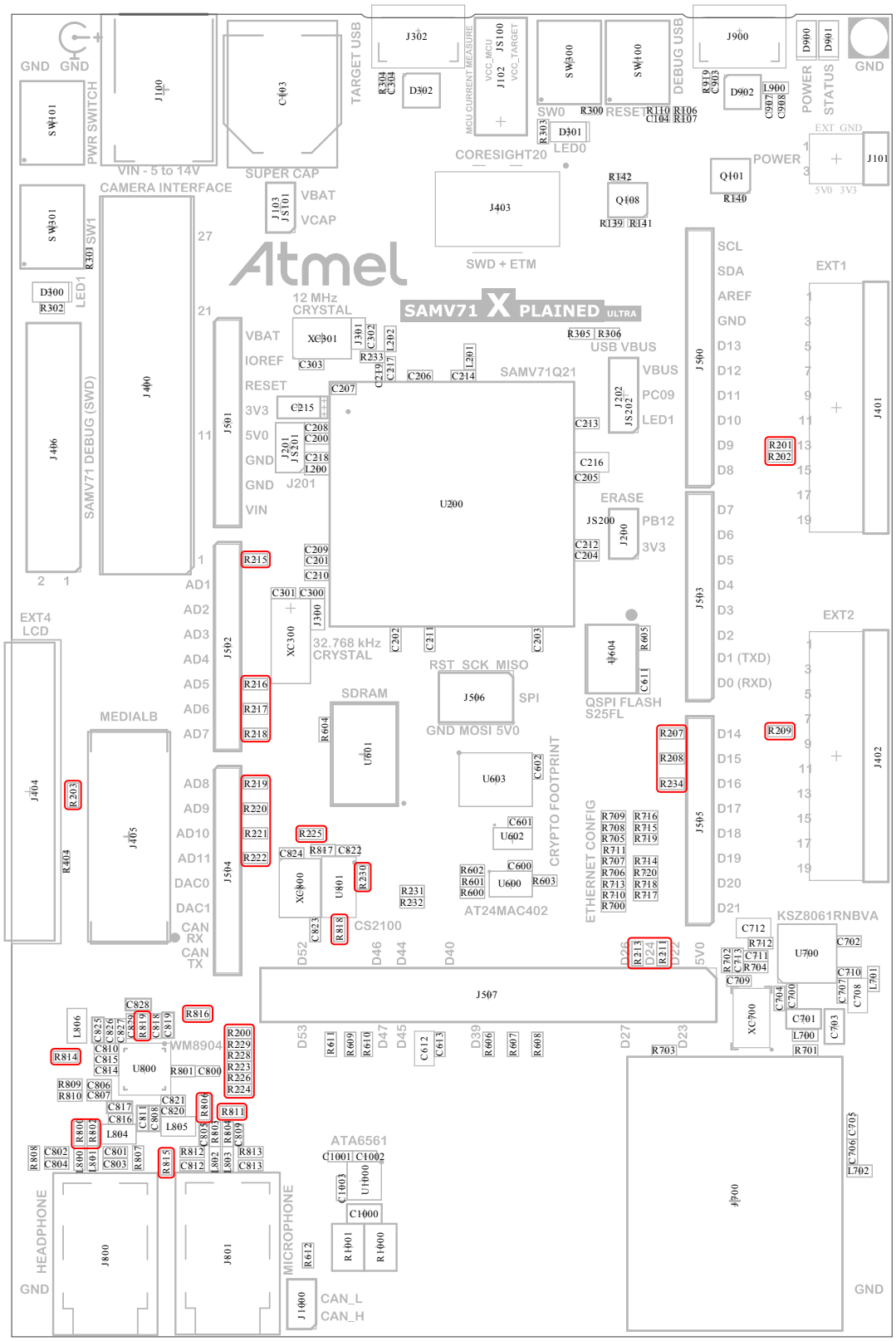
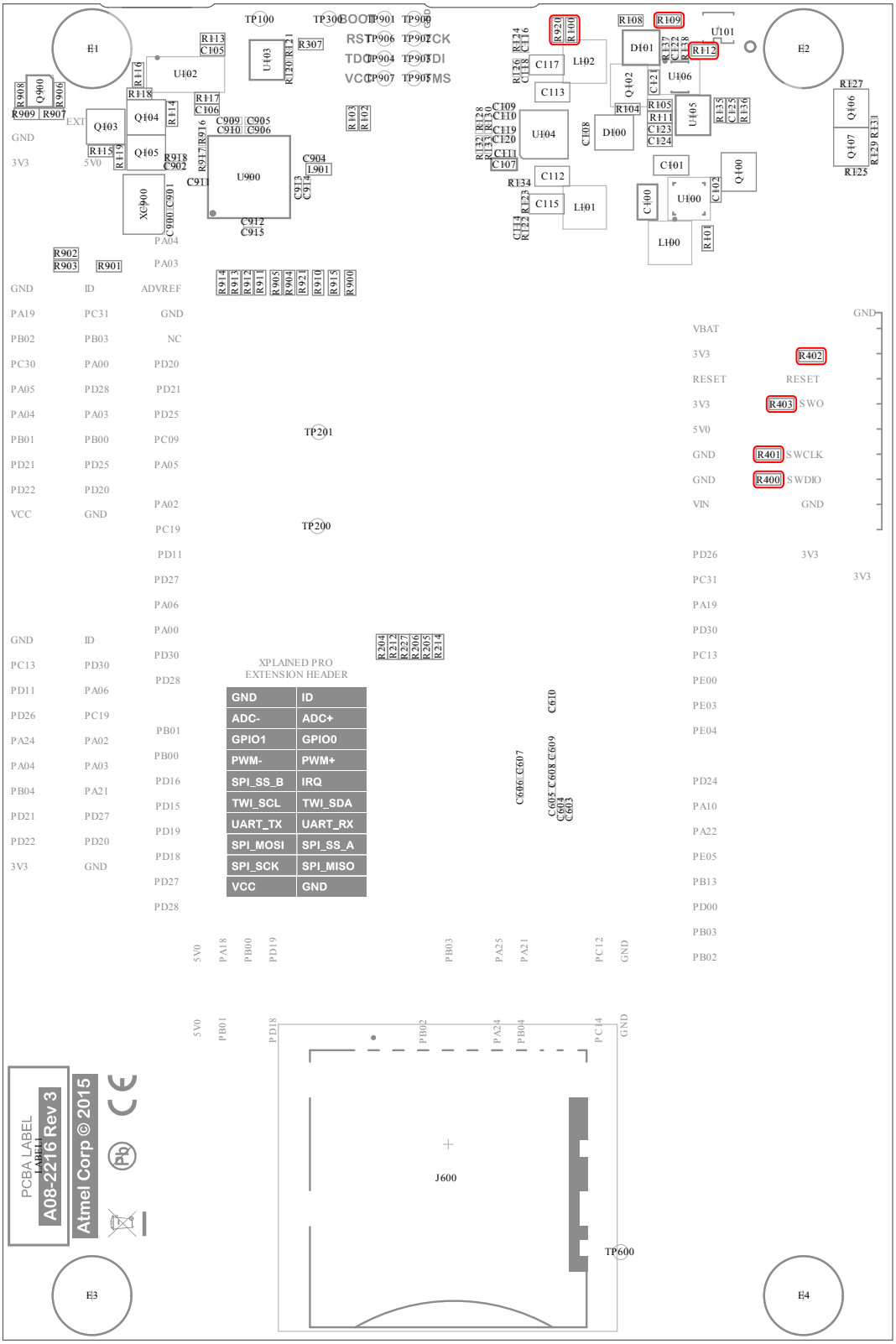


Figure 4-4 Zero Ohm Resistors Bottom



4.5. Embedded Debugger Implementation

SAM V71 Xplained Ultra contains an Embedded Debugger (EDBG) that can be used to program and debug the ATSAMV71Q21 using Serial Wire Debug (SWD). The Embedded Debugger also include a Virtual Com port interface over UART, an Atmel Data Gateway Interface over SPI, and TWI and it includes four of the SAM V71 GPIOs. Atmel Studio can be used as a front end for the Embedded Debugger.

4.5.1. Serial Wire Debug

The Serial Wire Debug (SWD) use two pins to communicate with the target. For further information on how to use the programming and debugging capabilities of the EDBG, see Embedded Debugger on page 7.

Table 4-34 SWD Connections

SAM V71 pin	Function	Shared functionality
PB07	SWD clock	Trace
PB06	SWD data	Trace
PB05	SWO Trace data	MediaLB and Trace
PB12	ERASE	SW1 and Chip Erase

4.5.2. Virtual COM Port

The Embedded Debugger acts as a Virtual Com Port gateway by using one of the ATSAMV71Q21 UARTs. For further information on how to use the Virtual COM port, see Embedded Debugger on page 7.

Table 4-35 Virtual COM Port Connections

SAM V71 pin	Function	Shared functionality
PB04	TXD1 (SAM V71 UART TX line)	EXT2, MediaLB, and Shield
PA21	RXD1 (SAM V71 UART RX line)	EXT2, MediaLB, and Shield

4.5.3. Atmel Data Gateway Interface

The Embedded Debugger features an Atmel Data Gateway Interface (DGI) by using either a SPI or I^2C port. The DGI can be used to send a variety of data from the ATSAMV71Q21 to the host PC. For further information on how to use the DGI interface, see Embedded Debugger on page 7.

Table 4-36 DGI Interface Connections when using SPI

SAM V71 pin	Function	Shared functionality
PD12	GPIO/SPI0_NPCS2 (Slave select) (SAM V71 is Master)	Camera
PD20	SPI0_MISO (Master In, Slave Out)	EXT1, EXT2, and Shield (2)
PD21	SPI0_MOSI (Master Out, Slave in)	EXT1, EXT2, Audio, Camera, and Shield (2)
PD22	SPI0_SPCK (Clock Out)	EXT1, EXT2, Camera, and Shield (2)

Table 4-37 DGI Interface Connections when using I^2C

SAM V71 pin	Function	Shared functionality
PA03	TWD0 (Data line)	EXT1, EXT2, LCD, Camera, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield
PA04	TWCK0 (Clock line)	EXT1, EXT2, LCD, Camera, Audio, PLL, MediaLB, EEPROM, Crypto, and Shield

Four GPIO lines are connected to the Embedded Debugger. The EDBG can monitor these lines and time stamp pin value changes. This makes it possible to accurately time stamp events in the SAM V71 application code. For further information on how to configure and use the GPIO monitoring features, see Embedded Debugger on page 7.

Table 4-38 GPIO Lines Connected to the EDBG

SAM V71 pin	Function	Shared functionality
PA09	GPIO0	Camera and SW0
PA23	GPIO1	LED0
PD28	GPIO2	EXT1, Camera, LCD, and Shield (2)
PA02	GPIO3	EXT2, LCD, and Shield

5. Kit Specific Data

One of the flash user pages in the EDBG is programmed with data specific to SAM V71 Xplained Ultra. The data can be read through the I^2C interface connected to the EDBG from the target application. For detailed information, see the EDBG User Guide. All data is stored as little endian. Table 5-1 MAC48Register, Offset: 0x00 on page 42 shows the memory map for the flash user page.

Table 5-1 MAC48Register, Offset: 0x00

Name	Description	Size [bits]
MAC48	Unique address assigned to the kit, value taken from the on board AT24MAC402.	48

6. Hardware Revision History and Known Issues

6.1. Identifying Product ID and Revision

The revision and product identifier of Xplained Pro boards can be found in two ways; either through Atmel Studio or by looking at the sticker on the bottom side of the PCB.

By connecting an Xplained Pro MCU board to a computer with Atmel Studio running, an information window will pop up. The first six digits of the serial number, which is listed under kit details, contain the product identifier and revision. Information about connected Xplained Pro extension boards will also appear in the Atmel Kit's window.

The same information can be found on the sticker on the bottom side of the PCB. Most kits will print the identifier and revision in plain text as A09-nnnn\rr, where nnnn is the identifier and rr is the revision. Boards with limited space have a sticker with only a QR-code, which contains a serial number string.

The serial number string has the following format:

"nnnnrrssssssssss"

n = product identifier

r = revision

s = serial number

The product identifier for SAM V71 Xplained Ultra is A09-2241.

6.2. EBI Signal Integrity

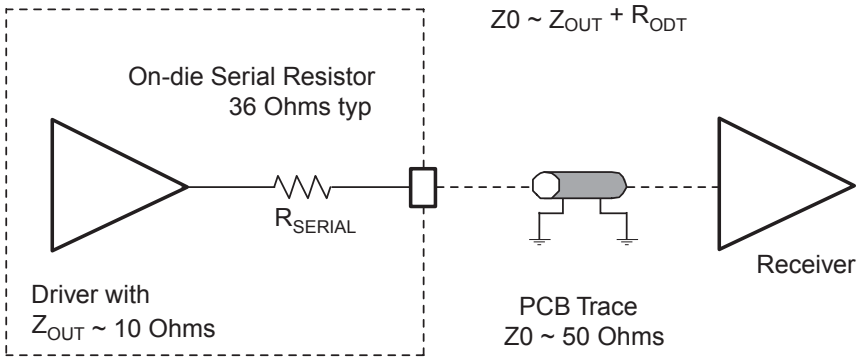
The ATSAMV71Q21 has on-die series termination on every I/O pin as shown in Figure 6-1 On-Die Termination on page 44.

Some of the pins that belong to the External Bus Interface (EBI) are connected to the on-board SDRAM and the Xplained Pro LCD connector (EXT4). When a cable is plugged into the LCD connector long stubs are created on the signal lines, the stubs create ringing that reduces the maximum clock speed, which can be used when communicating with the SDRAM.

For more detailed information about termination strategies, see application note AT91-AN02: Signal Integrity and AT91 Products.

All designs should be simulated using an IBIS file for the ATSAMV71Q21 and the target peripherals to check that the signals are within the limits of the devices.

Figure 6-1 On-Die Termination



6.3. 12MHz Crystal Selection

The selected 12MHz crystal *FQ5032B-12-C-C-C-200-1* has a load of 20pF, this is outside the recommended range of 12.5pF to 17.5pF in the ATSAMV71Q21 datasheet. Using a crystal with loads outside the recommended range can cause instability when operating the device close to maximum/ minimum parameters for supply voltage and temperature.

Fix/Workaround: None, any new design should select a crystal within the limits specified in the datasheet.

Related Links

Crystals on page 28

6.4. Revision 9

Revision 9 of SAM V71 Xplained Ultra has engineering samples mounted with part number ATSAMV71Q21A-AAB-ES4.

Revision 9 of SAM V71 Xplained Ultra is otherwise identical to revision 8.

6.5. Revision 8

Revision 8 of SAM V71 Xplained Ultra has engineering samples mounted with part number ATSAMV71Q21A-AAB-ES2 or ATSAMV71Q21A-AAB-ES3.

Revision 8 of SAM V71 Xplained Ultra uses PCB (A08-2216) revision 3.

Revision 8 of SAM V71 Xplained Ultra fixes the issues described in Revision 6 on page 45.

6.5.1. PCB Revision Marking

One thousand SAM V71 Xplained Ultra revision 8 kits have revision 3 PCBs (A08-2216) that are marked with "Revision 2" under the location of the serial number sticker.

These PCBs can be identified by the addition of the "USB VBUS" and "SUPER CAP" connectors shown in Figure 4-2 SAM V71 Xplained Ultra Connector Overview on page 15 that were not present in revision 2 of the PCB.

6.6. Revision 6

Revision 6 of SAM V71 Xplained Ultra has engineering samples mounted with part number ATSAMV71Q21A-AAB-ES2.

Revision 6 of SAM V71 Xplained Ultra uses PCB (A08-2216) revision 2.

6.6.1. Device Marking

Some revision 6 kits may have SAM V71 devices marked as *ATSAMX7EA-AU-ES2*, these devices are equivalent to *ATSAMV71Q21A-AAB-ES2*.

6.6.2. Camera Connector and Audio

PD11 is shared between the camera connector ISI_D6, Audio CODEC IRQ, an Arduino connector, and Xplained Pro extension header 2 GPIO (EXT2). PD11 is pulled low strongly by the Audio CODEC and the pin is not usable by any other source unless it is disconnected. Removing R200 will disconnect PD11 from the Audio CODEC interrupt pin freeing it up to be used for camera and extension applications.

PD28 is shared between the camera connector ISI_D9, Arduino connectors, LCD extension connector IRQ1 (EXT4), and Xplained Pro extension header 1 IRQ (EXT1). If a camera with 10-bit mode is used together with a display connected to EXT4 the display IRQ line will conflict with the camera.

On revision 6 of SAM V71 Xplained Ultra pin 41 (DISPLAY ENABLE) on the LCD connector is not connected to anything (floating).

6.6.3. Super Capacitor

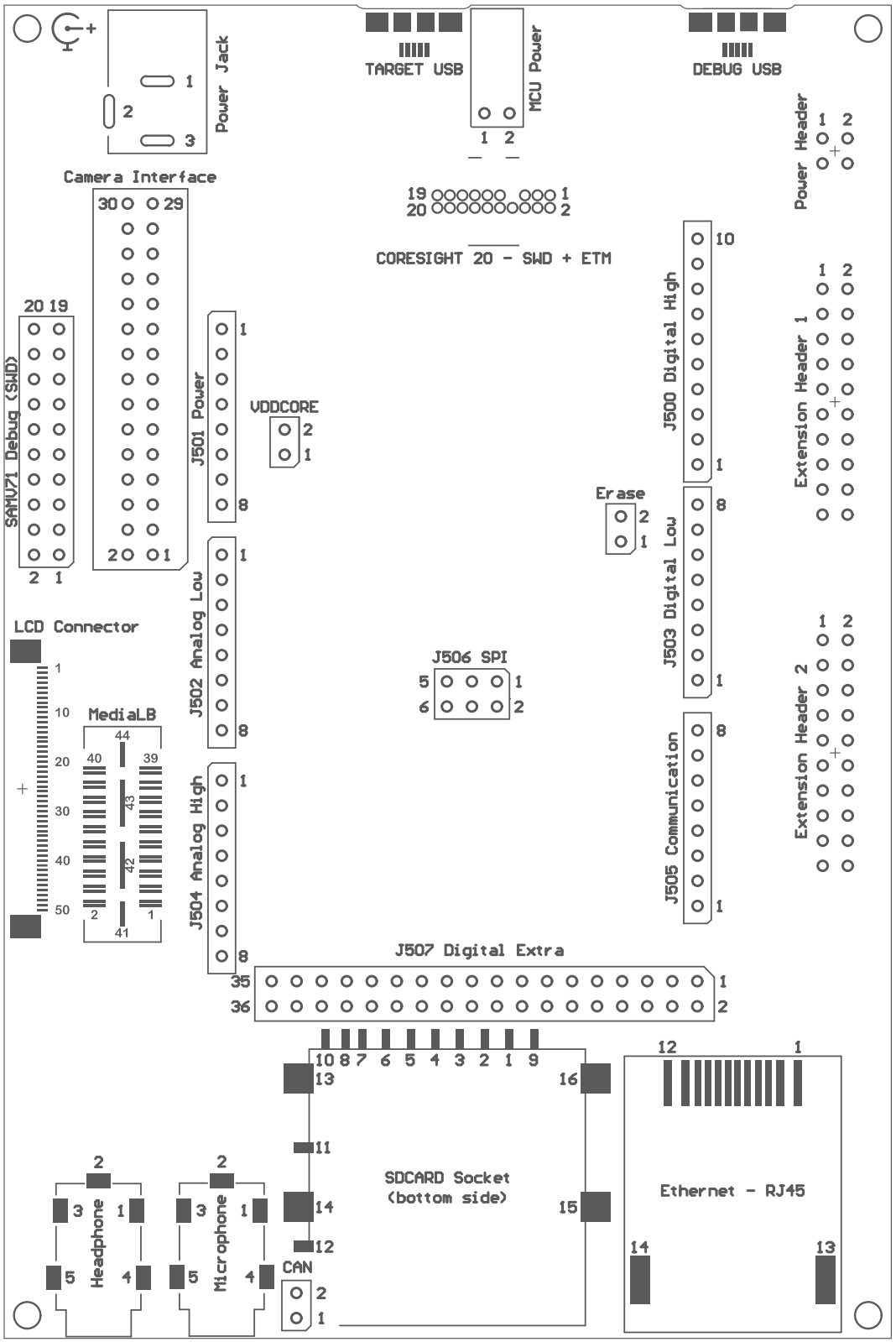
The charging circuit for the on-board super capacitor described in Power Distribution on page 13 does not work as intended. It is therefore not possible to run the ATSAMV71Q21 from the on-board super capacitor. It is, however, fully possible to run the ATSAMV71Q21 in low power modes with external power connected and measure the devices power consumption trough the Current Measurement Header on page 26.

Revision 6 of SAM V71 Xplained Ultra does not have the super capacitor disconnect pin-header described in Super Capacitor on page 26.

6.6.4. Connectors

Revision 6 of SAM V71 Xplained Ultra has fewer connectors than newer revision. Figure 6-2 SAM V71 Xplained Ultra Connector Overview on page 46 is applicable for revision 6 instead of the figure described in Figure 4-2 SAM V71 Xplained Ultra Connector Overview on page 15.

Figure 6-2 SAM V71 Xplained Ultra Connector Overview



6.6.5. Target USB

Revision 6 of SAM V71 Xplained Ultra does not have the ability to detect power on the target USB connector. The pin-header marked "USB VBUS" in Figure 4-2 SAM V71 Xplained Ultra Connector Overview on page 15 and described in Table 4-16 USB VBUS Selection on page 26 is not implemented in the PCB.

6.6.6. Ethernet RJ-45 Connector

On revision 6 of SAM V71 Xplained Ultra the TX and RX differential pairs has a swapped position on the RJ-45 connector compared to what is normal.

Table 6-1 Ethernet RJ-45 Connector Pin-out

Component pin number	Revision 6	Later revisions
1	LED0 VCC	LED0 VCC
2	LED0 GPIO	LED0 GPIO
3	**RX_P**	**TX_P**
4	**RCT**	**TCT**
5	**RX_N**	**TX_N**
6	**TX_P**	**RX_P**
7	**TCT**	**RCT**
8	**TX_N**	**RX_N**
9	NC	NC
10	GND	GND
11	LED1 GPIO	LED1 GPIO
12	LED1 VCC	LED1 VCC
13	TAB	TAB
14	TAB	TAB

6.6.7. Zero Ohm Resistors

Revision 6 of SAM V71 Xplained Ultra does not have R203 that is listed in Table 4-33 Zero Ohm Resistors on page 35.

The assembly drawings below are applicable for revision 6 of SAM V71 Xplained Ultra instead of the ones shown in Zero Ohm Resistors on page 35.

Figure 6-3 Zero Ohm Resistors Top Revision 6

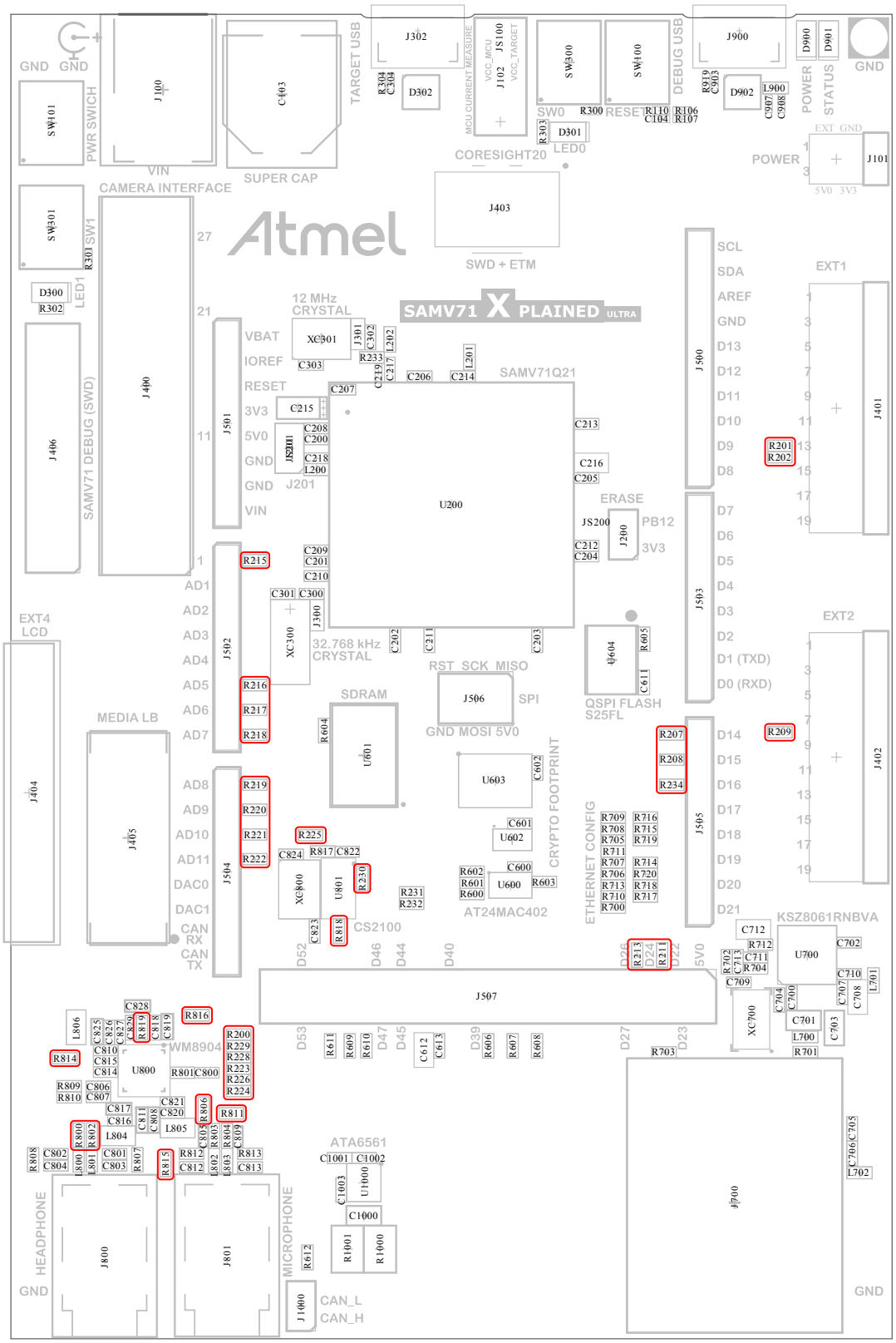
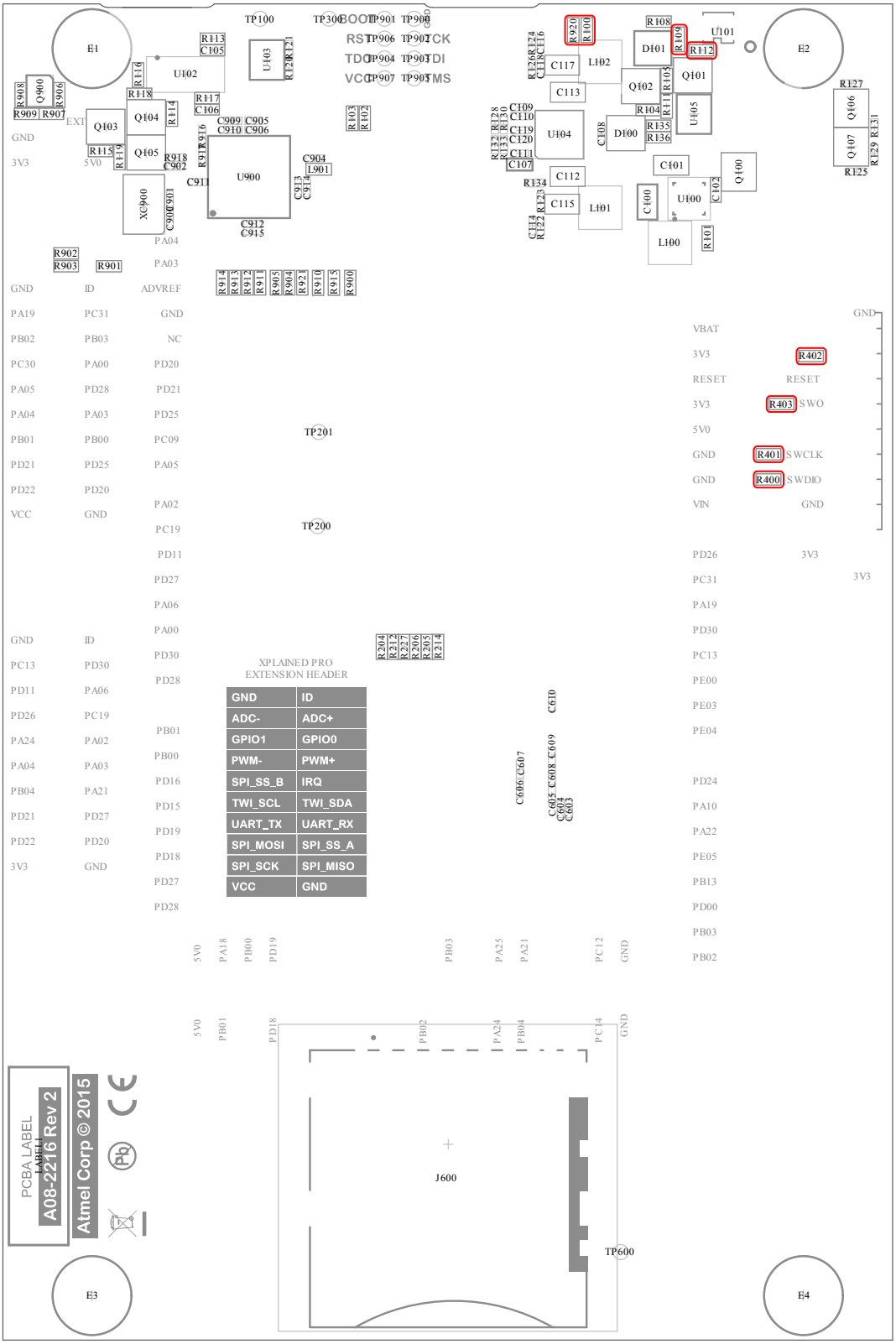


Figure 6-4 Zero Ohm Resistors Bottom Revision 6



7. Appendix

7.1. Getting Started with IAR

IAR Embedded Workbench® for ARM® is a proprietary high efficiency compiler not based on GCC. Programming and debugging of Xplained Pro kits are supported in IAR™ Embedded Workbench for ARM using the common CMSIS-DAP interface. Some initial settings have to be set up in the project to get the programming and debugging to work.

The following steps will explain how to get your project ready for programming and debugging:

1. Make sure you have opened the project you want to configure. Open the **OPTIONS** dialog for the project.
2. In the category **General Options**, select the **Target** tab. Select the device for the project or, if not listed, the core of the device.
3. In the category **Debugger**, select the **Setup** tab. Select **CMSIS DAP** as the driver.
4. In the category **Debugger**, select the **Download** tab. Check the check box for **Use flash loader(s)** option.
5. In the category **Debugger** > **CMSIS DAP**, select the **Setup** tab. Select **System (default)** as the reset method.
6. In the category **Debugger** > **CMSIS DAP**, select the **JTAG/SWD** tab. Select **SWD** as the interface and optionally select the **SWD speed**.

Figure 7-1 Select Target Device

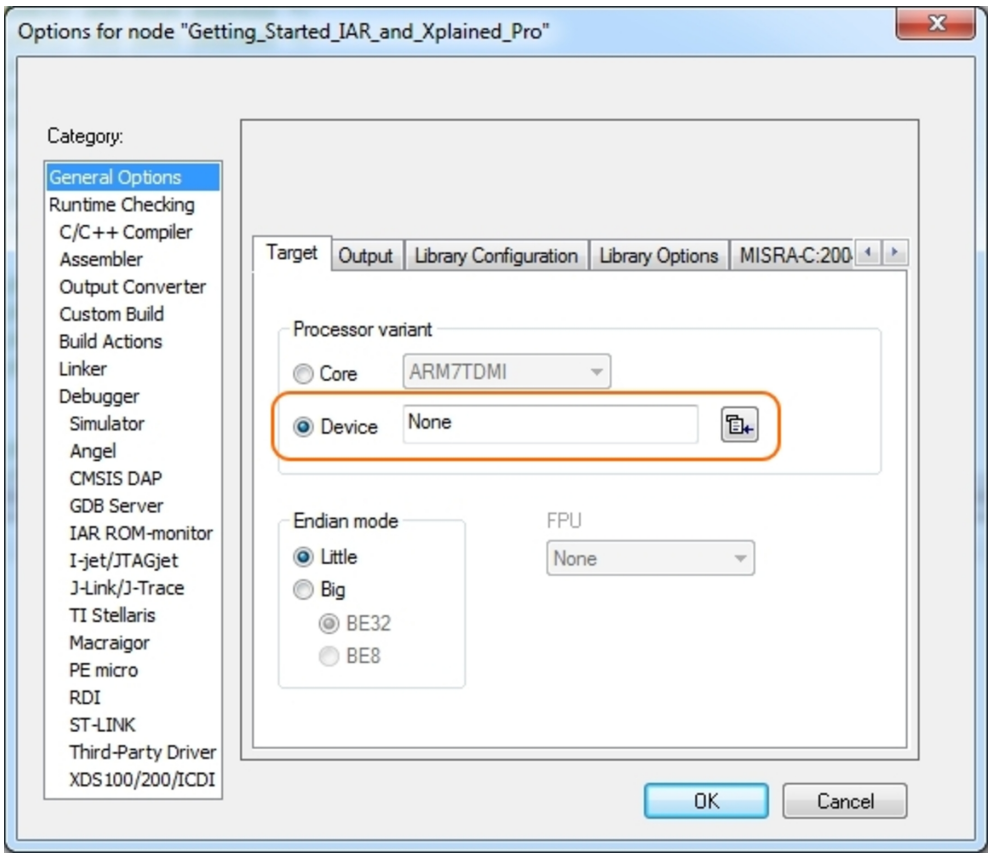


Figure 7-2 Select Debugger

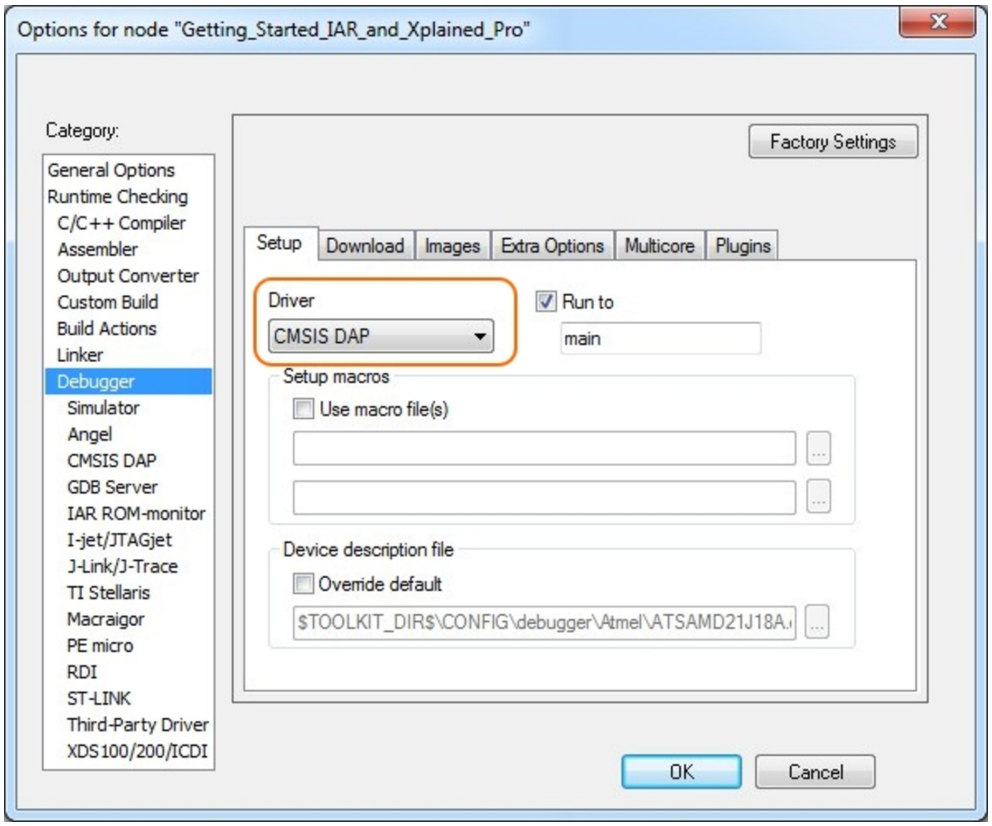


Figure 7-3 Configure Flash Loader

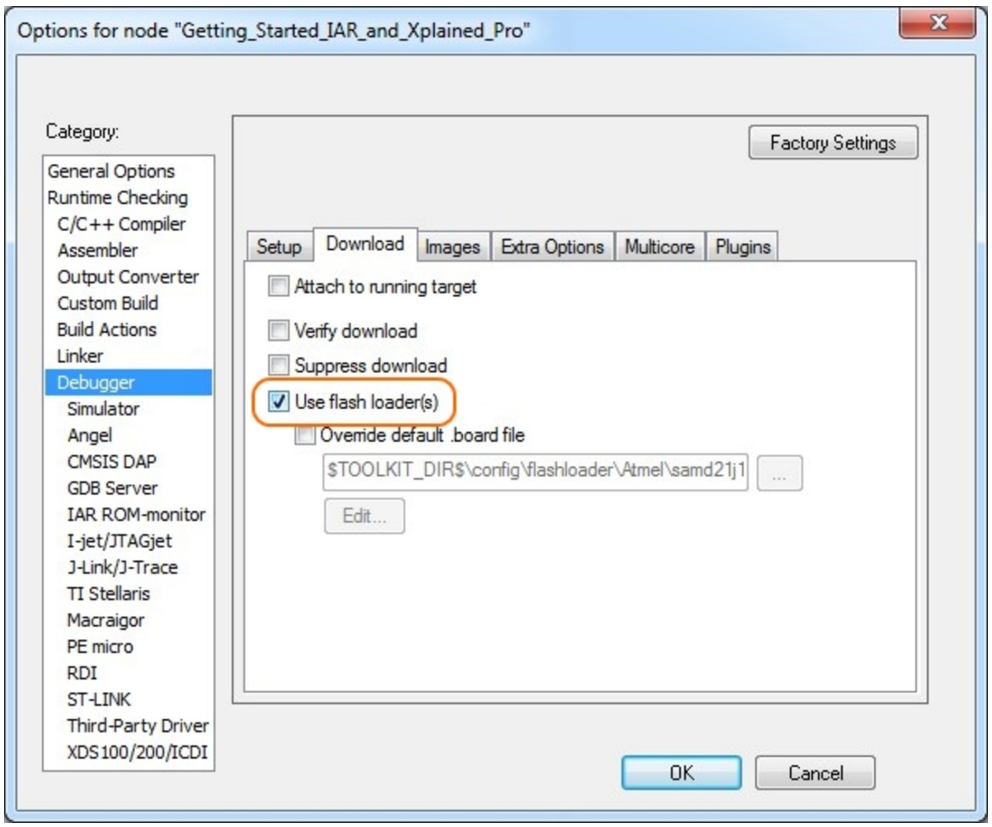


Figure 7-4 Configure Reset

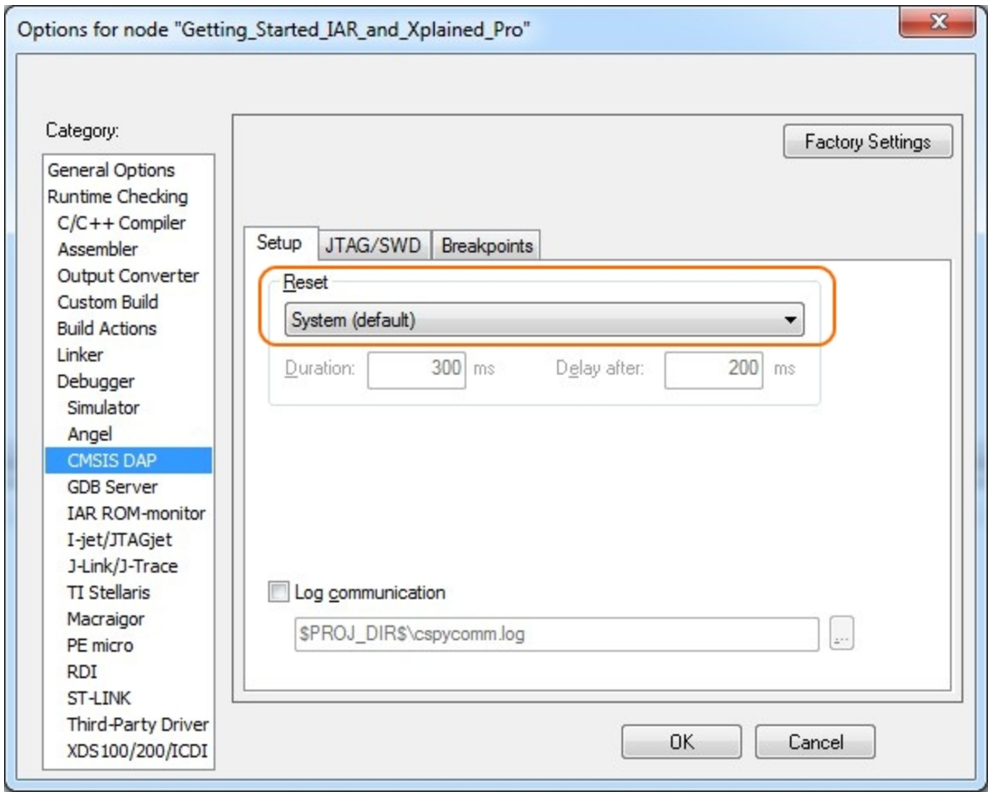
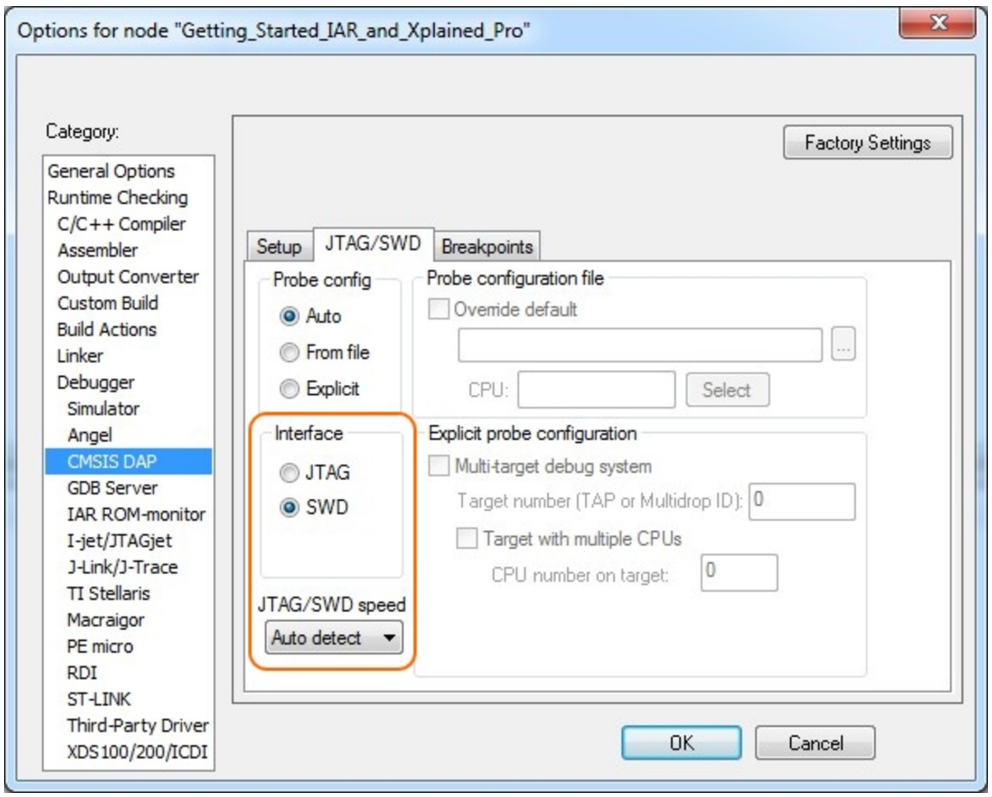


Figure 7-5 Configure Interface



8. Document Revision History

Doc. rev.	Date	Comment
42408C	09/2015	Updated user guide to reflect revision 9 of the kit, added 12MHz crystal selection ERRATA, and added IAR getting started guide.
42408B	06/2015	Updated user guide to reflect revision 8 of the kit, see Revision 6 on page 45 for ERRATA.
42408A	02/2015	Initial document release.

9. Evaluation Board/kit Important Notice

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Mailing Address:

Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA







Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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