Features

- **Three DSPs and 24-bit Audio Router On-chip**
- **32 kHz to 96 kHz Sampling Rate**
- **16-bit Microcontroller On-chip**
- **Variety of I/Os, including SmartMedia™ and DataFlash®**
- **Embedded RAM for Single Chip Operation (530 kbit)**
- **Warm Start Power-down**
- **1 µA Typical Deep Power-down, 0.5 mW/MIPS Typical Operating**
- **External Flash/ROM Capability**
- **Available in a 64-lead TQFP Package**
- **Ideal for Real-time Audio Applications**
  - **MP3 Decoding Wavetable Synthesis (GM-Lite)**
  - **Effect Processing (Reverb, Echo, Chorus, etc.)**
  - **Speech Recognition and Synthesis**
  - **Filtering, Sampling Rate Conversion**
- **Typical Applications: Cellular Phones, MP3 Player, Effect Devices, Intelligent Answering Machinces, Toys**

Description

The ATSAM3103 is a member of the new ATSAM3000 family that uses DSP Array Technology. The ATSAM3103 includes three 24-bit DSPs, a 24-bit Audio Router and a general purpose 16-bit on-chip CISC Microcontroller. Its high performance and flexibility with eight input and eight output channels allow implementation of professional quality audio applications such as effects processing and MP3 decoding. A variety of I/Os, including SmartMedia™ and DataFlash® are provided. Sampling rates up to 96 kHz at 24 bits are supported.

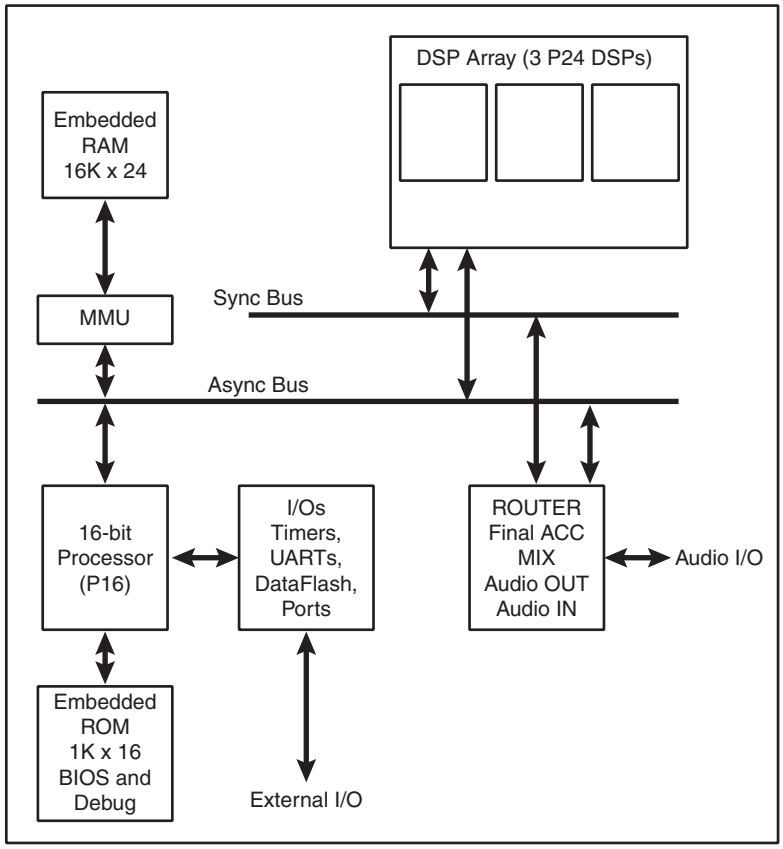
Audio Processing

ATSAM3103 Versatile Low-power Audio DSP/ Low-cost Effects DSP

6093A–DRMSD–25-Oct-04

DSP Array Block Diagram

Figure 1. ATSAM3103 DSP Array Block Diagram



Functional Description

DSP Array

The ATSAM3103 includes three on-chip DSPs.

Each DSP (P24) is built around a 2K x 24 RAM and a 1K x 24 ROM. The RAM contains both data and P24 instructions; the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data such as compressed audio through the Async Bus. Each P24 RAM can be accessed through the Async Bus.

Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop.

One P24 is sufficient for processing one channel of MP3, implementing a multi-tap delay line or a multi-tap transversal filter. A single P24 is also capable of generating 12 voices of wavetable sound at 32 kHz sampling rate (8 voices at 48 kHz), including sample cache, pitch control, second-order filter and two envelope generators.

Sync Bus

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48 or 96 kHz. Each frame is divided into 64 time slots. Each slot is divided into 4 bus cycles. Each P24 is assigned a hardwired time slot (8 to 63), during which it may provide 24-bit data to the bus (up to 4 data samples). Each P24 can read data on the bus at any time,

allowing inter P24 communication at the current sampling rate. Slots 0 to 7 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

Async Bus

The Async Bus is 24-bit data inside the chip and 16-bit outside.

The P16 processor normally masters the Async Bus; it can read/write the P24 memories and the external or embedded ROM/RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX convert fixed-point DSP data to floating-point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

16-bit Processor

The P16 processor is widely used in ATSAM products. Using the P16 allows to keep the large firmware investments from the ATSAM97xx series. A built-in ROM, connected to the P16, holds basic input/output software (BIOS) for peripherals such as UART, DataFlash, SmartMedia, MPU, as well as a debugger using a dedicated asynchronous serial line. The firmware can reside on external parallel ROM/Flash or it can be downloaded at power-up into the built-in 16K x 24 RAM from serial EEPROM, DataFlash, SmartMedia or host.

MMU (Memory Management Unit)

The MMU handles transfer requests between the external or embedded RAM/ROM, the P16 and the P24s through the Async Bus. The ATSAM3103 includes an on-chip 16K x 24 RAM.

Router: Final ACC, MIX, Audio Out, Audio In

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. Eight channels of audio in and eight channels of audio out are provided (4 stereo in/out, I2S format). The stereo audio in channels may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

I/O

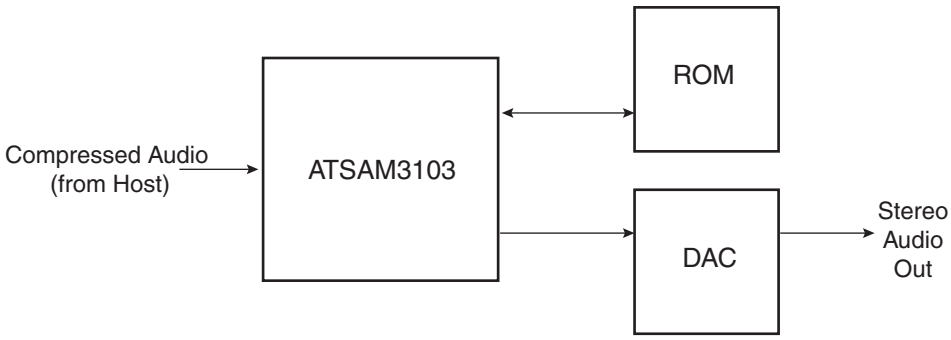
The ATSAM3103 includes versatile I/Os that share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.

The following peripherals are included on-chip:

- 2 x 8-bit timers
- 2 x 16-bit timers
- Parallel slave 8-bit port, MPU401 compatible
- Parallel master 8-bit port, for connection to SmartMedia and/or LCD display, switches, etc.
- 2 x asynchronous bi-directional serial ports
- Synchronous serial slave port (SPI type host connection)
- SPI master bi-directional port for EEPROM or DataFlash connection
- Firmware controlled I/O pins

Typical Application Examples

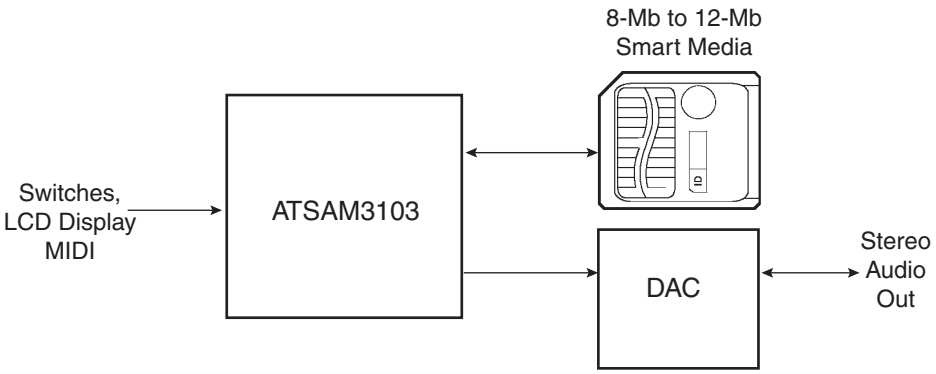
Figure 2. Host-controlled MP3 Player



- ATSAM3103 firmware download from host (when using parallel interface)
- Choice of host communication interfaces
  - 8-bit parallel
  - Asynchronous serial(1)
  - Synchronous serial (SPI)(1)
- Full MP3 support inculding very low bit rate extension (ISO/IEC 13813-3)
- Easily upgradeable to other coding standards
- Single CBGA on request

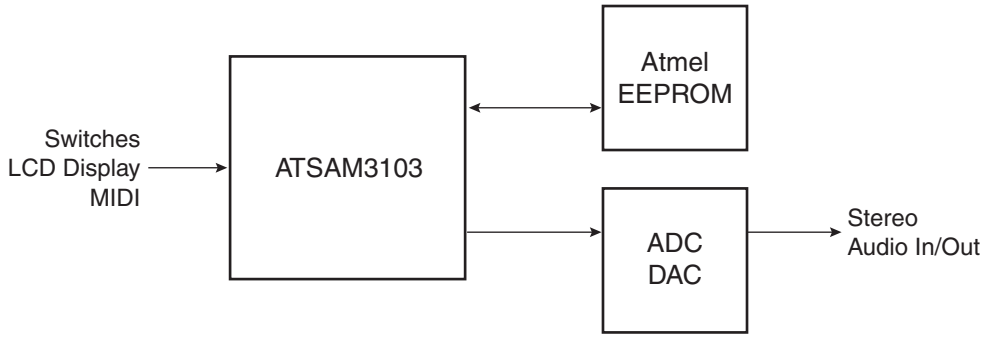
Note: 1. External firmware serial EEPROM required

Figure 3. Stand-alone MP3 Player (SmartMedia Based)



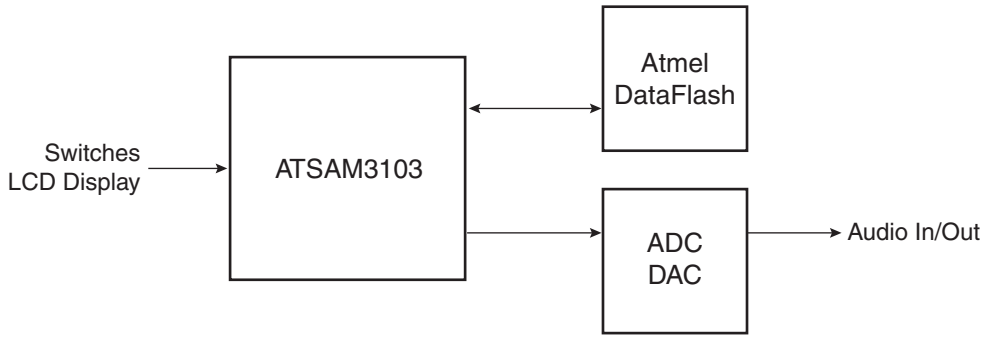
- S/Pdif connection possible
- PC connection possible

Figure 4. Low-cost High-quality Effect



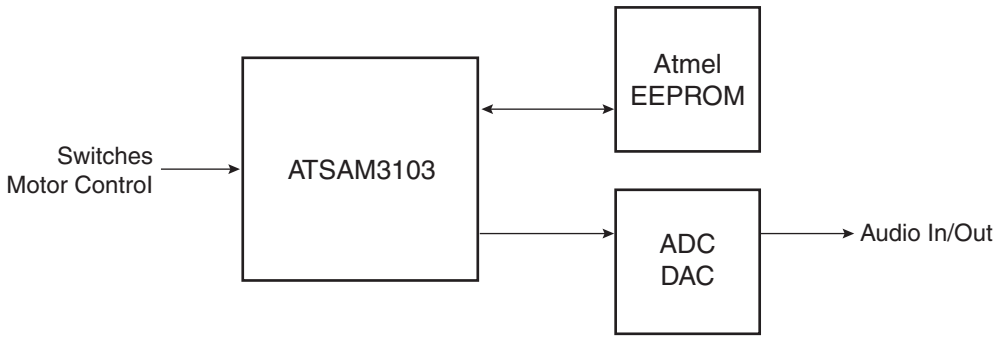
- High quality, full 24-bit Multi-effects such as reverb, chorus and compression
- Stereo 10-band graphic equalizer

Figure 5. Intelligent Answering Machines (DataFlash-based)



- High quality telephone recording at low bit rate (8 kbit/sec)
- Close to one hour recording capacity using 32-Mbit DataFlash
- Detects touch-tone
- Easy to program

Figure 6. Toys with Artificial Intelligence



- Speech recognition
- Learning functions
- ADPCM record/play

DSP Capacity and I/O Configuration

DSP Considerations

The ATSAM3103 includes three P24 DSPs.

Table 1 lists the performance levels achievable by the P24.

Table 1. P24 Performance Levels

Function	P24s Required
MP3 decode	3
Stereo reverb and chorus @48 kHz	1
31-band equalizer @96 kHz	3
Stereo 31-band equalizer @48 kHz	3
256 points FFT or IFFT @96 kHz incl. windowing	1

The ATSAM3103 runs firmware from built-in 16 x 24 RAM. The firmware should be downloaded at power-up. This can be done from the following:

- A small 256-kbit external EEPROM with SPI interface such as the Atmel AT25256
- A DataFlash (current capacities range from 1 Mbit to 64 Mbits) if audio storage functions are required
- A SmartMedia card (supported capacities from 8 Mbytes to 128 Mbytes)
- Parallel MPU type interface

I/O Selection Considerations

I/Os are organized in groups that can be mutually exclusive because they share the same IC pins (please refer to the pinout to identify the exclusions). The two main types of operation are host controlled and stand-alone.

Host-controlled Operation

There are three main possible ways of communication with a host processor:

- 8-bit parallel MPU type bi-directional interface signals: D7 - D0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, IRQ
- Asynchronous serial, MIDI_IN and, optionally, MIDI_OUT
- Synchronous serial signals: SDIN, SCLK, SYNC, $\overline{INT}$

The MPU type interface allows downloading firmware to the chip from the host. If another interface is used, then external EEPROM or DataFlash is required.

Stand-alone Operation

Possible stand-alone modes are:

- Firmware into external ROM or DataFlash
- Firmware into external SmartMedia. In this case, the firmware should reside in the SmartMedia reserved sectors starting at sector #1.

Pinout

Pin Description

- Identical sharing number indicates multifunction pins.
- Pd indicates a pin with built-in pull-down resistor.
- Pu indicates a pin with built-in pull-up resistor.

Table 2. Pinout by Pin Name

Pin Name	Pin Number	Type	Sharing	Description
GND	4, 13, 19, 25 , 36, 43, 48, 57	PWR	-	Digital ground. All these pins should be returned to a ground plane
VC18	12, 31, 46, 63	PWR	-	Core power. All these pins should be returned to nominal 1.8V or to PWROUT if the built-in power switch is used.
VC33	3, 32	PWR	-	Periphery power. All these pins should be returned to nominal 3.3V.
PWRIN	18	PWR	-	Power switch input; should be returned to nominal 1.8V even if the power switch is not used
PWROUT	17	PWR	-	Power switch output; should be connected to all VC18 pins if the power switch is used
D7 - D0	59, 58, 56, 55, 52, 51, 50, 49	I/O	1	Slave 8-bit interface data. Output if $\overline{CS}$ and $\overline{RD}$ are low (read from chip), input if $\overline{CS}$ and $\overline{WR}$ are low (write to chip). Type of data defined by A0 input.
I/O7 - I/O0	59, 58, 56, 55, 52, 51, 50, 49	I/O	1	SmartMedia data or other peripheral data
P0.7 - P0.0	59, 58, 56, 55, 52, 51, 50, 49	I/O	1	General-purpose I/O; can be programmed individually as input or output
CLAD3 - 0	59, 58, 56, 55	In	1	Optional bit clocks for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif.
WSAD3 - 0	52, 51, 50, 49	In	1	Optional word selects for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/BEU or S/Pdif.
A0	60	In	2	Slave 8-bit interface address. Indicates data/status or data/ctrl transfer type ($\overline{CS}$ $\overline{RD}$ low or $\overline{CS}$ $\overline{WR}$ low)
SMPD	60	In	2	SmartMedia presence detect
P0.10	60	In	2	General-purpose input pin
SCLK	60	In	2	Serial slave synchronous interface input clock
$\overline{CS}$	64	In	3	Slave 8-bit interface chip select, active low
P0.11	64	In	3	General-purpose input pin
SYNC	64	In	3	Serial slave synchronous interface input sync signal
$\overline{WR}$	1	In	4	Slave 8-bit interface write, active low. D7 - D0 data is sampled by chip on $\overline{WR}$ rising edge if $\overline{CS}$ is low
$\overline{SMC}$	1	In	4	SmartMedia configuration. This pin is sensed after power-up. If found low, it is assumed that a SmartMedia connector is present. The built-in firmware will wait for SmartMedia SMPD.
P0.12	1	In	4	General-purpose input pin
$\overline{RD}$	2	In	5	Slave 8-bit interface read, active low. D7 - D0 data is output when $\overline{RD}$ goes low and $\overline{CS}$ is low

Table 2. Pinout by Pin Name (Continued)

Pin Name	Pin Number	Type	Sharing	Description
$\overline{RIB}$	2	In	5	SmartMedia Ready Busy/ status
P0.13	2	In	5	General-purpose input pin
IRQ	8	Out	6	Slave 8-bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host ($\overline{CS}$ = 0 and $\overline{RD}$ = 0)
$\overline{SMRE}$	8	Out	6	SmartMedia read enable ($\overline{RE}$), active low
FS0	8	In	6	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1).
P0.8	8	I/O	6	General-purpose I/O pin
$\overline{INT}$	8	Out	6	Serial slave synchronous interface data request, active low
MIDI_IN	9	In	7	Serial MIDI in
P0.14	9	In	7	General-purpose input pin
SDIN	9	In	7	Serial slave synchronous interface input data
MIDI_OUT	10	Out	8	Serial MIDI out
FS1	10	In	8	Freq sense, sensed at power up. FS1/FS0 allow firmware to know operating frequency of chip as follows: 00 6.9552 MHz 01 9.6 MHz 10 11.2896 MHz 11 12.288 MHz
P0.9	10	I/O	8	General-purpose I/O
DABD3 - 0	42, 41, 40, 39	Out	-	Four stereo channels of digital audio output, I2S format
CLBD	6	Out	-	Audio bit clock for DABD3 - 0. Audio bit clock for DAAD3 - 0 if the corresponding CLAD3 - 0 is not used.
WSBD	7	Out	-	Audio left/right channel select for DABD3 - 0. Audio left/right channel for DAAD3 - 0 if the corresponding WSAD3 - 0 is not used.
CKOUT	5	Out	-	External DAC/Codec master clock. Same frequency as X2 pin. Can be programmed to be 128 x Fs, 192 x Fs, 256 x Fs, 384 x Fs, where Fs is the DAC/Codec sampling rate.
DAAD0	34	In	9	Stereo audio data input, I2S format. Can operate on CLBD master rate or CLAD0 external rate when sampling rate conversion is requested.
P0.15	34	In	9	General-purpose input pin
DAAD3 - 1	38, 37 35	In Pd	-	Three additional channels of stereo audio input, I2S format. Can individually operate on CLBD master rate or corresponding CLAD3 - 1 when sampling rate conversion is requested. DAAD3 - 1 have built-in pull-downs. They may be left open if not used.
MUTE	11	I/O	10	External DAC/Codec Mute. Sensed at power up. If found high, then MUTE becomes an active high output. If found low, then MUTE becomes an active low output.
P1.6	11	I/O	10	General-purpose I/O pin
$\overline{SMCE}$	29	Out	11	SmartMedia chip enable ($\overline{CE}$), active low
P1.5	29	I/O	11	General-purpose I/O pin
SMALE	28	Out	12	SmartMedia address latch enable (ALE)

Table 2. Pinout by Pin Name (Continued)

Pin Name	Pin Number	Type	Sharing	Description
P1.4	28	I/O	12	General-purpose I/O pin
$\overline{\text{SMWE}}$	27	Out	13	SmartMedia write enable ($\overline{\text{WE}}$), active low
P1.3	27	I/O	13	General-purpose I/O pin
SMCLE	26	Out	14	SmartMedia command latch enable (CLE)
P1.2	26	I/O	14	General-purpose I/O pin
$\overline{\text{DFCS}}$	14	Out	-	DataFlash chip select
DFSI	16	Out	-	DataFlash serial input (to DataFlash)
DFSO	21	In Pd	-	DataFlash serial output (from DataFlash). This pin has a built-in pull-down. It may be left open if not used.
DFSCK	15	Out	-	DataFlash data clock
P1.15 - P1.11	30, 62, 61, 54, 53	I/O Pu	-	Five General-purpose I/O pins. These pins have built-in pull-ups. They may be left open if not used.
X1 - X2	45, 44	-	-	External crystal connection. Standard frequencies are 6.9552 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. $1.8V_{PP}$) can be connected to X1 using AC coupling (22 pF). A built-in PLL multiplies the clock frequency by 4 for internal use.
LFT	47	-	-	PLL decoupling RCR filter
$\overline{\text{RESET}}$	22	In	-	Master reset Schmitt trigger input, active low. $\overline{\text{RESET}}$ should be held low during at least 10 ms after power is applied. On the rising edge of $\overline{\text{RESET}}$, the chip enters an initialization routine, which may involve firmware download from an external SmartMedia, DataFlash or host.
STIN	23	In Pd	-	Serial test input. This is a 57.6 Kbaud asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.
STOUT	24	Out	-	Serial test output. 57.6 Kbaud async output used for firmware debugging.
$\overline{\text{PDWN}}$	20	In	-	Power down input, active low. High level on this pin is typ. VC18. When $\overline{\text{PDWN}}$ is low, the oscillator and PLL are stopped, the power switch opens, and the chip enters a deep sleep mode (1 µA typ. consumption when power switch is used). To exit from power down, $\overline{\text{PDWN}}$ has to be set high then $\overline{\text{RESET}}$ applied. Alternate programmable power-downs are available which allow warm restart of the chip.
TEST	33	In Pd	-	Test input. Should be grounded or left open.

Pinout by Pin Number

Table 3. ATSAM3133 Pinout by Pin Number

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	$\overline{WR}$ $\overline{SMC}$ P0.12	17	PWROUT	33	TEST	49	D0 I/O0 P0.0 WSAD0
2	$\overline{RD}$ $\overline{RIB}$ P0.13	18	PWRIN	34	DAAD0 P0.15	50	D1 I/O1 P0.1 WSAD1
3	VC33	19	GND	35	DAAD1	51	D2 I/O2 P0.2 WSAD2
4	GND	20	$\overline{PDWN}$	36	GND	52	D3 I/O3 P0.3 WSAD3
5	CKOUT	21	DFSO	37	DAAD2	53	P1.11
6	CLBD	22	$\overline{RESET}$	38	DAAD3	54	P1.12
7	WSBD	23	STIN	39	DABD0	55	D4 I/O4 P0.4 CLAD0
8	IRQ $\overline{SMRE}$ FS0 P0.8	24	STOUT	40	DABD1	56	D5 I/O5 P0.5 CLAD1
9	MIDI_IN P0.14 SDIN	25	GND	41	DABD2	57	GND
10	MIDI_OUT FS1 P0.9	26	SMCLE P1.2	42	DABD3	58	D6 I/O6 P0.7 CLAD2
11	MUTE P1.6	27	$\overline{SMWE}$ P1.3	43	GND	59	D7 I/O7 P0.7 CLAD3
12	VC18	28	SMALE P1.4	44	X2	60	A0 SMPD P0.10 SCLK
13	GND	29	$\overline{SMCE}$ P1.5	45	X1	61	P1.13
14	$\overline{DFCS}$	30	P1.15	46	VC18	62	P1.14
15	DFSCK	31	VC18	47	LFT	63	VC18
16	DFSI	32	VC33	48	GND	64	$\overline{CS}$ P0.11 SYNC

Mechanical Dimensions

Figure 7. Thin Plastic 64-lead Quad Flat Pack (TQFP64)

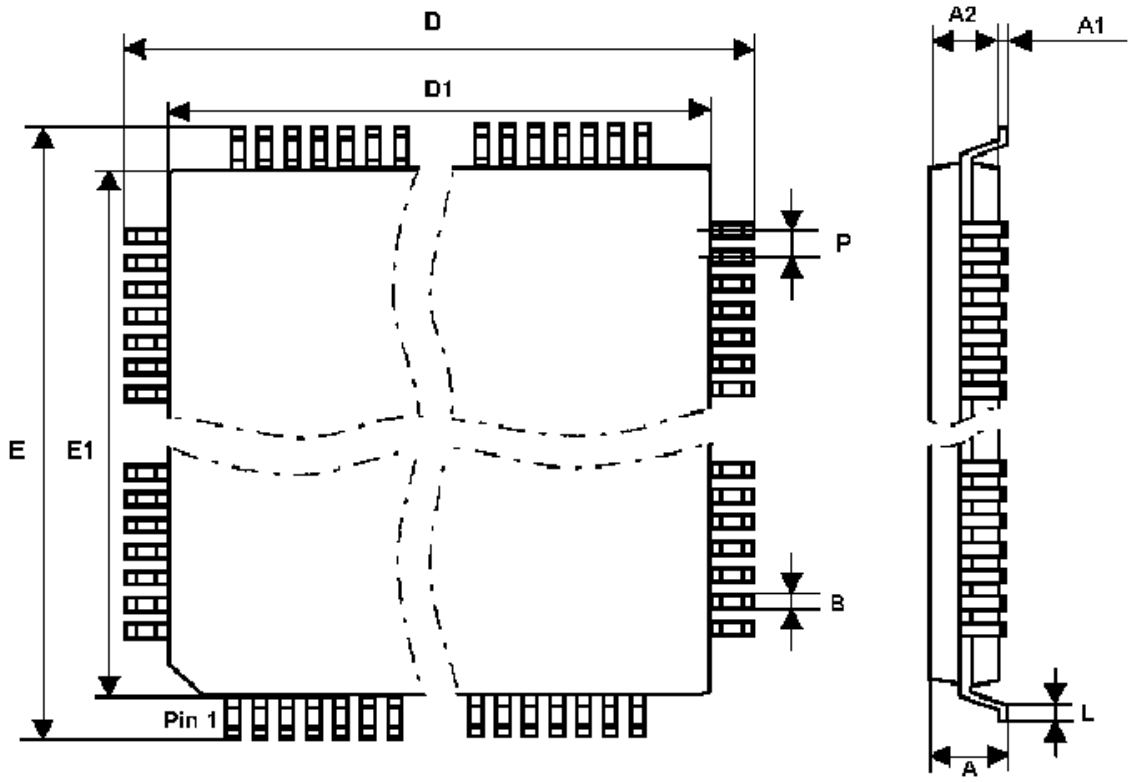


Table 4. Package Dimensions in mm

Denomination	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
L	0.45	0.60	0.75
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
P		0.50	
B	0.17	0.22	0.27

Electrical Characteristics

Absolute Maximum Ratings(*)

Ambient Temperature (power applied).....-40°C to 85°C Storage Temperature .....-65°C to 150°C Voltage on any pin X1, LFT ..... -0.3 to V_{C18} + 0.3V Others ..... -0.3 to V_{C33} + 0.3V Supply Voltage..... V_{C18}.....-0.3V to 1.95V V_{C3} .....-0.3V to 3.6V Maximum IOL per I/O pin..... 4 mA	*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{C18}	Supply voltage	1.65	1.8	1.95	V
V_{C33}	Supply voltage(1)	3	3.3	V_{C18} + 1.5 3.6	V
PWRIN	Supply voltage PWRIN pin	1.75	1.9	1.95	V
T_A	Operating ambient temperature	0	-	70	°C

Note: 1. Operation at lower V_{C33} values down to V_{C18} is possible, however external timing may be impaired. Please contact Atmel in case of use of these circuits with V_{C33} outside the recommended operating range.

DC Characteristics

Table 6. DC Characteristics (T_A = 25°C, V_{C18} = 1.8V ± 10%, V_{C33} = 3.3V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	-0.3	-	1.0	V
V_{IH}	High level input voltage, except X1, $\overline{PDWN}$	2.3	-	V_{C33} + 0.3	V
V_{IH}	High level input voltage X1, $\overline{PDWN}$	1.2	-	V_{C18} + 0.3	V
V_{OL}	Low level output voltage I_{OL} = -2 mA	-	-	0.4	V
V_{OH}	High level output voltage I_{OH} = 2 mA	2.9	-	-	V
I_{CC1}	V_{C18} power supply current (crystal freq. = 11.2896 MHz, all three P24s running)	-	40	-	mA
I_{CC2}	V_{C18} power supply current (crystal freq. = 11.2896 MHz, all P24s stopped)	-	22	-	mA
I_{CC3}	V_{C18} power supply current (crystal freq. = 11.2896 MHz, all P24s stopped, warm start power-down active)	-	4	-	mA
I_{CC4}	V_{C18} deep power down supply current (using power switch)	-	1	10	µA
PU/PD	Built-in pull-up/pull-down resistor	10	-	56	kΩ

Slave 8-bit Parallel Interface

Pins used: D7-D0 (I/O), $\overline{CS}$ (input), A0 (input), $\overline{WR}$ (input), $\overline{RD}$ (input), IRQ (output).

This interface is typically used to connect the chip to a host processor.

Timings

Figure 8. Host Interface Read Cycle

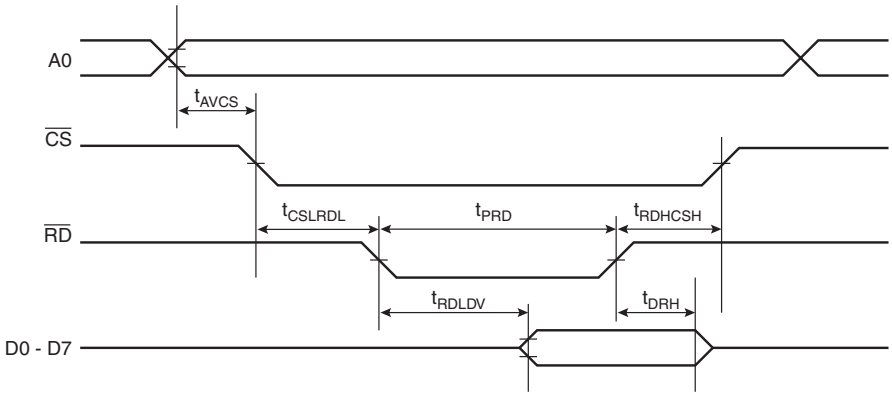


Figure 9. Host Interface Write Cycle

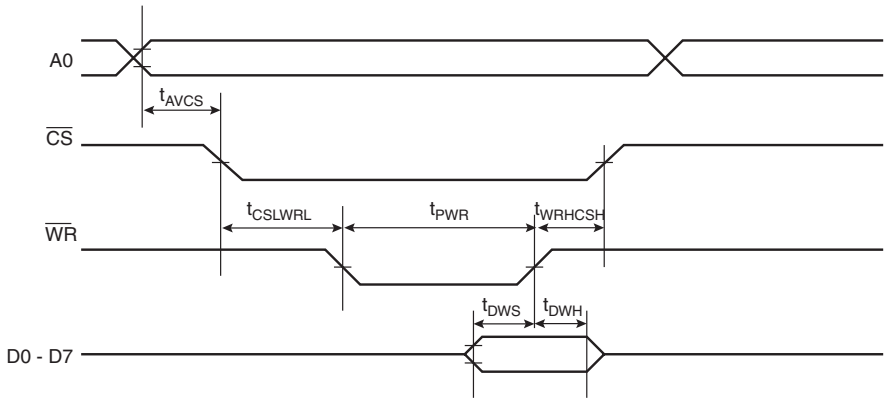


Table 7. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address valid to chip select low	0	-	-	ns
t_{CSLRDL}	Chip select low to $\overline{RD}$ low	5	-	-	ns
t_{RDHCSH}	$\overline{RD}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PRD}	$\overline{RD}$ pulse width	50	-	-	ns
t_{RDLDV}	Data out valid from $\overline{RD}$	-	-	20	ns
t_{DRH}	Data out hold from $\overline{RD}$	5	-	10	ns
$t_{CSLRWRL}$	Chip select low to $\overline{WR}$ low	5	-	-	ns
t_{WRHCSH}	$\overline{WR}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PWR}	$\overline{WR}$ pulse width	50	-	-	ns
t_{DWS}	Write data setup time	10	-	-	ns
t_{DWH}	Write data hold time	0	-	-	ns

IO Status Register

7	6	5	4	3	2	1	0
TE	RF	X	X	X	X	X	X

Status register is read when A0 = 1, $\overline{RD}$ = 0, $\overline{CS}$ = 0.

- **TE: Transmit Empty**

If 0, data from ATSAM3103 to host is pending and IRQ is high. Reading the data at A0 = 0 will set TE to 1 and clear IRQ.

- **RF: Receiver Full**

If 0, then ATSAM3103 is ready to accept DATA from host.

Note: If status bit RF is not checked by host, write cycle time should not be lower than 3 µs.

SmartMedia and Other Peripheral Interfaces

This is a master 8-bit parallel interface that provides connection to SmartMedia or other peripherals such as LCD screens.

Pins used: I/O7 - I/O0 (I/O), SMPD (input), $\overline{SMCE}$, SMALE, SMCLE, $\overline{SMRE}$, $\overline{SMWE}$ (outputs)

All these pins are fully under firmware control, therefore timing compatibility is ensured by firmware only.

EEPROM/DataFlash Interface

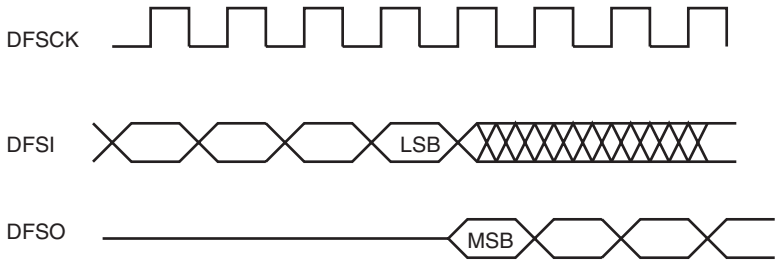
This is a master synchronous serial interface, operating in SPI mode 0.

Pins used: $\overline{DFCS}$, DFSI, DFSCK (outputs), DFSO (input)

The DFSCK frequency is firmware programmable from fck to fck/64, where fck is the crystal frequency. Thus a large variety of EEPROM/DataFlash devices can be accomodated.

Please refer to Atmel DataFlash datasheets for accurate SPI mode 0 timing.

Figure 10. Typical DataFlash Interface Timing



Serial Slave Synchronous Interface

The ATSAM3103 can be controlled by an external host processor through the unidirectional serial interface. However, no firmware can be downloaded at power-up through this interface. Therefore an external ROM/Flash/EEPROM is required.

Pins used: SCLK, SYNC, SDIN (input), $\overline{INT}$ (output)

Data is shifted MSB first. The IC samples an incoming SDIN bit on the rising edge of SCLK, therefore the host should change SDIN on the negative SCLK edge.

SYNC allows initial synchronization. The rising edge of SYNC, which should occur with SCLK low, indicates that SDIN will hold MSB data on the next rising SCLK.

The data is stored internally in a 256-byte FIFO.

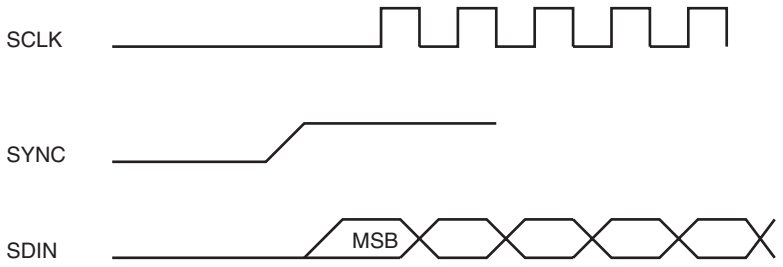
When the FIFO count is below 64, the $\overline{INT}$ output goes low. This allows the host processor to send data in burst mode.

The maximum SCLK frequency is fck (fck being the crystal frequency).

The minimum time between two bytes is 64 fck periods.

The contents of the SDIN data are defined by the firmware.

Figure 11. Serial Slave Interface Typical Timing



Digital Audio

Pins used: CLBD (output), WSBD (output), DABD3 - 0 (outputs), DAAD3 - 0 (inputs)

Optionally: CLAD3 - 0 (inputs), WSAD3 - 0 (inputs)

The ATSAM3103 allows for 8 digital audio output channels and 8 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD3 - 0 inputs can be synchronized with incoming CLAD3 - 0 and WSAD3 - 0 signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S standard, with up to 24 bits per sample

Figure 12. Digital Audio

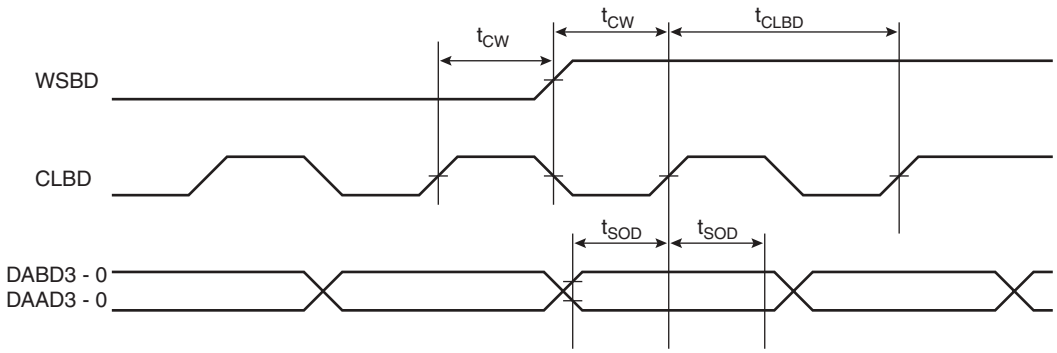


Table 8. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD rising to WSBD change	t_C - 10	-	-	ns
t_{SOD}	DABD valid prior/after CLBD rising	t_C - 10	-	-	ns
t_{CLBD}	CLBD cycle time	-	2 * t_C	-	ns

t_C is related to t_{CK}, the crystal period at X1 as follows:

Table 9. Sample Frequency

Sample Frequency WSBD	Typical Sample Frequency	t_C	CLBD/WSBD Frequency Ratio
1/(t_{CK} * 128)	96 kHz	t_{CK}	64
1/(t_{CK} * 192)	64 kHz	2 * t_{CK}	48
1/(t_{CK} * 256)	48 kHz	2 * t_{CK}	64
1/(t_{CK} * 384)	32 kHz	4 * t_{CK}	48

The choice of sample frequency is done by the firmware.

Figure 13. Digital Audio Frame Format, 128 x Fs and 256 x Fs Modes

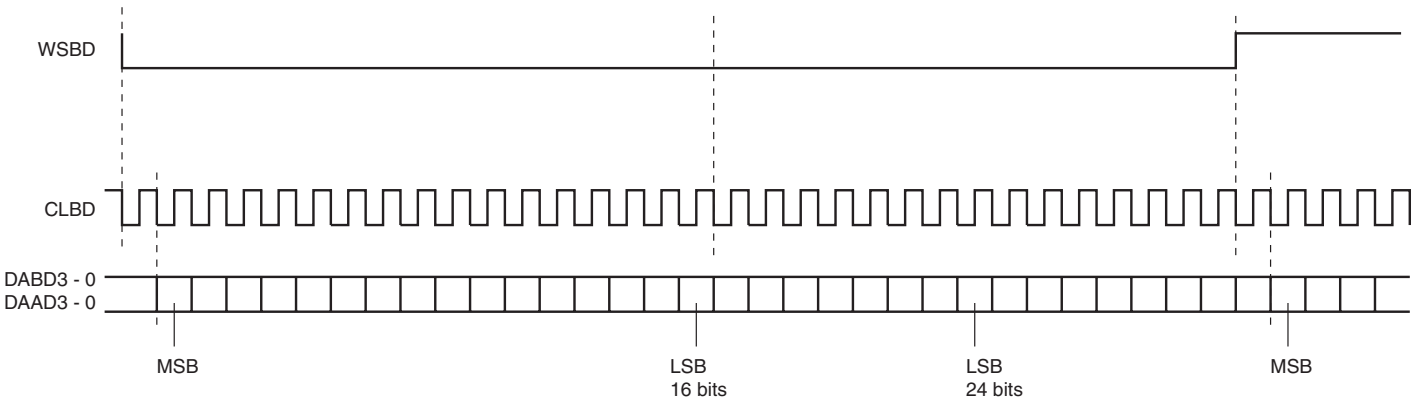
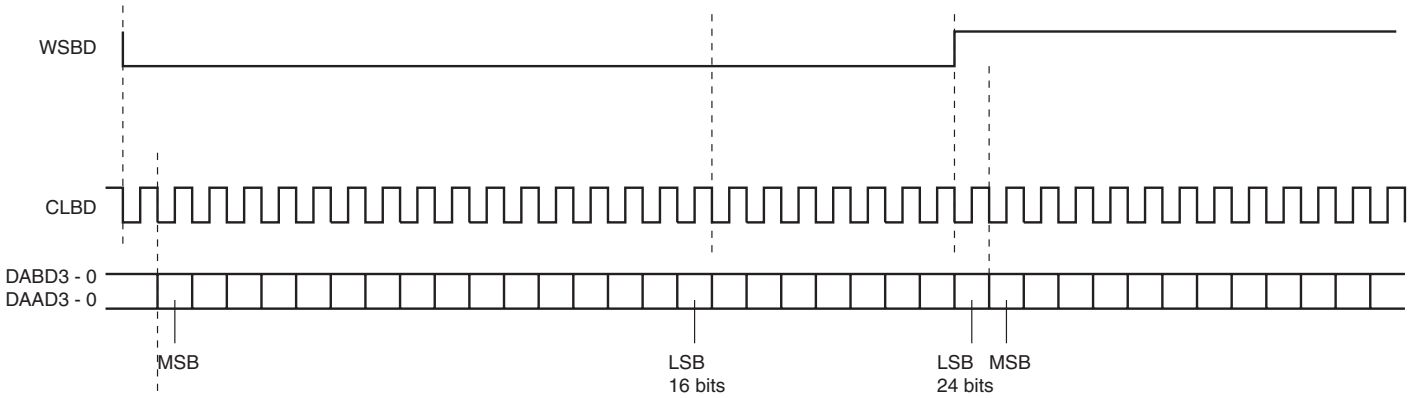


Figure 14. Digital Audio Frame Format, 192 x Fs and 384 x Fs Modes



Serial MIDI_IN and MIDI_OUT

The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

- Baud rate: 31.25 kHz
- Format: start, 8 data bits, 1 stop

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10 ms.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- $\overline{\text{SMC}}$ is sensed. If LOW, then the built-in loader waits for SmartMedia presence detect (SMPD). When detected, the firmware is downloaded from SmartMedia reserved sector 1 and started.
- An attempt is made to read the first two bytes of an external EEPROM or DataFlash. If “DR” is read, then the built-in loader loads the firmware from the external EEPROM/DataFlash and starts it.
- Firmware download from a host processor is assumed.

1. The byte 0ACh is written to the host, this raises IRQ. The host can recognize that the chip is ready to accept program download. Higher speed transfer can be reached by polling the parallel interface status ($\overline{\text{CS}}$ = 0, A0 = 1, $\overline{\text{RD}}$ = 0).
2. The host sends the firmware size (in words) on two bytes (Low byte first).
3. The host sends the ATSAM3103 firmware. The firmware should begin with string “DR”.
4. The byte 0ACh is written to the host, this raises IRQ. The host recognizes that the chip has accepted the firmware.
5. ATSAM3103 starts the firmware.

If $\overline{\text{PDWN}}$ is asserted low, then the crystal oscillator and PLL are stopped. If the power switch is used, then the chip enters a deep power-down sleep mode, as power is removed from the core. To exit power down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped.
- The clock frequency can be internally divided by 256.

Recommended Board Layout

Like all HCMOS high integration ICs, the following simple rules of board layout are mandatory for reliable operation:

- GND, VC33, VC18 Distribution and Decouplings

All GND, VC33, VC18 pins should be connected. A GND plane is strongly recommended. The board GND + VC33 distribution should be in grid form.

Recommended VC18 decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. VC33 requires a single 0.1µF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the ATSAM3103 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from ATSAM3103.

- Buses

A ground plane should be implemented below the D0 - D7 bus, which is connected to the host and to the ATSAM3103 GND.

A ground plane should be implemented below the WA0 - WA21/WD0 - WD15 bus, which is connected to the ROM/Flash grounds and to the ATSAM3103.

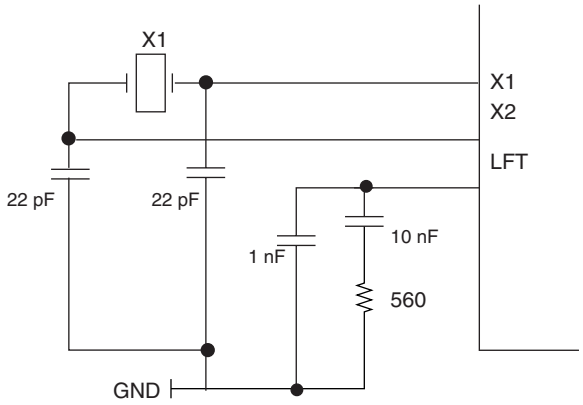
- Analog Section

A specific AGND ground plane should be provided, which is connected to the GND ground by a single trace. No digital signals should cross the AGND plane.

Refer to the Codec vendor recommended layout for correct implementation of the analog section.

Recommended Crystal Compensation and LFT Filter

Figure 15. Recommended Crystal Compensation and LFT Filter



Product Development and Debugging

Atmel provides an integrated product development and debugging tool SamVS. SamVS runs under Windows® (98, ME, 2000, XP). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In-circuit Emulation)
- Program Dataflash, EEPROM, SmartMedia on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 Kbauds. Thus time-to-market is optimized by testing directly on the final prototype.

A library of frequently used functions is available, such as:

- Reverb/Chorus
- MP3 decode
- 31-band equalizer
- Parametric equalizer

Atmel engineers are available to study customer-specific applications.

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