Three-Wire True Zero-Speed Differential Peak-Detecting Sensor IC with Continuous Calibration

FEATURES AND BENEFITS

- Wide operating voltage range
- Peak detecting algorithm robust against signal perturbations
- Capable of sensing a wide range of target types
- Running mode calibration for continuous optimization
- Single chip IC for high reliability
- Precise duty cycle signal throughout operating temperature range
- Large operating air gaps
- Automatic Gain Control (AGC) for air-gap–independent switchpoints
- Automatic Offset Adjustment (AOA) for signal processing optimization
- True zero-speed operation

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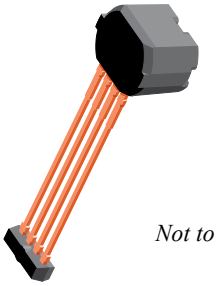
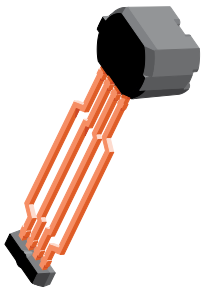
Packages:

4-Pin SIP (suffix SG)



Not to scale

4-Pin SIP (suffix SJ)



DESCRIPTION

The ATS468 is a true zero-speed gear tooth sensor IC consisting of an optimized Hall IC and a permanent magnet pellet configuration in a single overmolded package. The integrated circuit provides a manufacturer-friendly solution for digital gear tooth sensing applications. This small package can be easily assembled and used in conjunction with gears of various shapes and sizes.

The integrated circuit incorporates dual Hall effect elements with a 2.2 mm spacing and signal processing that switches in response to differential magnetic signals created by a ferromagnetic target. The circuitry contains a sophisticated digital circuit to reduce system offsets, to calibrate the gain for air-gap–independent switchpoints, and to achieve true zero-speed operation. Signal optimization occurs at power-on through the combination of offset and gain adjust, and is maintained throughout the operating time with the use of a running-mode calibration. The running-mode calibration provides immunity to environmental effects such as micro-oscillations of the target or sudden air gap changes.

The device is ideally suited to obtaining speed and duty cycle information in gear tooth–based speed, position, and timing applications, such as in speedometers.

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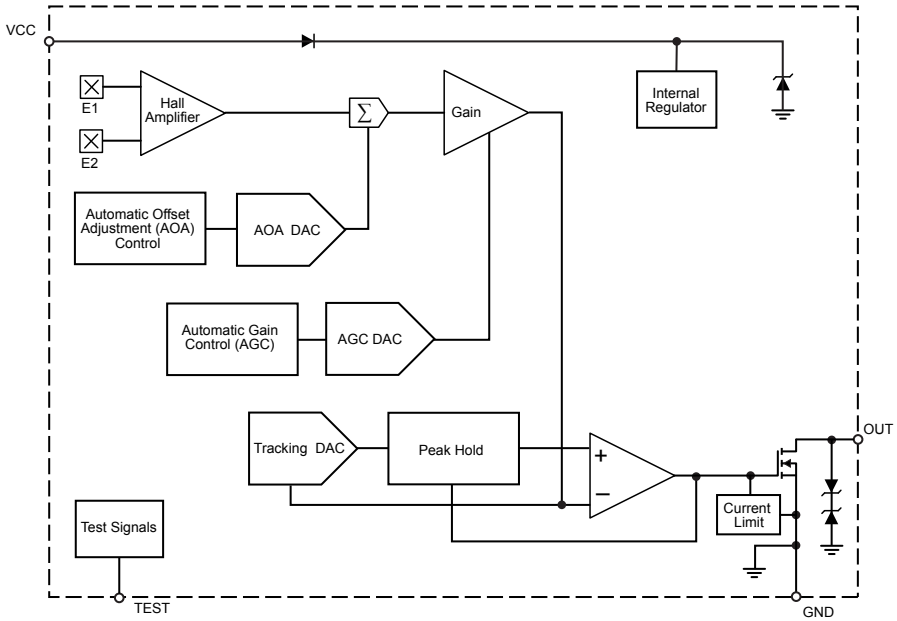


Functional Block Diagram

Features and Benefits (continued)

- Undervoltage lockout
- Reverse battery protection
- Robust test coverage capability with Scan Path and IDDQ measurement

Description (continued)

The ATS468 is available in two 4-pin SIPs (suffix SG and SJ). The packages are lead (Pb) free, with 100% matte tin leadframe plating.

SPECIFICATIONS

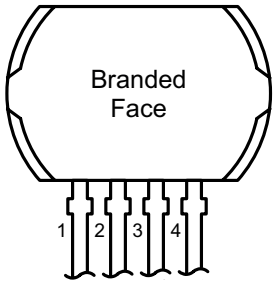
Selection Guide

Part Number	Package	Packing*	Operating Ambient Temperature Range, T_A (°C)
ATS468LSGTN-T	4-pin through hole SIP	800 pieces per reel	-40 to 150
ATS468LSJTN-T	4-pin through hole SIP	800 pieces per reel	-40 to 150

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Refer to Power Derating Curves chart	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Current	I_{OUT}		30	mA
Reverse Output Current	I_{ROUT}		–50	mA
Reverse Output Voltage	V_{ROUT}		–0.5	V
Output Off Voltage	V_{OUT}		28	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C



Package SG and SJ, 4-Pin SIP Pin-out Diagram

Terminal List Table

Number	Name	Function
1	VCC	Supply voltage
2	VOUT	Output
3	TEST	Test pin, float
4	GND	Ground

OPERATING CHARACTERISTICS: valid throughout operating voltage and ambient temperature ranges using Allegro reference target 60-0, typical data applies at V_{CC} = 12 V and T_A = 25°C; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Electrical Characteristics						
Supply Voltage[2]	V_{CC}	Operating, $T_J \le 165°C$	4	–	26.5	V
Undervoltage Lockout	$V_{CC(uv)}$	$V_{CC} = 0 \rightarrow V_{CC}(min) + 1$ V and $V_{CC}(min) + 1$ V $\rightarrow 0$ V	–	–	$V_{CC}(min)$	V
Supply Current	I_{CC}	$V_{CC} > V_{CC}(min)$	3.0	5.0	7.5	mA
Power-On Characteristics						
Power-On State	POS	V_{OUT}, connected as in figure 6	–	High	–	V
Power-On Time[3]	t_{PO}	$V_{CC} > V_{CC}(min)$	–	–	2.3	ms
Transient Protection Characteristics						
Supply Zener Clamp Voltage	$V_{Z(supply)}$	$I_{CC} = I_{CC}(max) + 3$ mA, T_A = 25 °C	38	–	–	V
Supply Zener Current	$I_{Z(supply)}$	V_{supply} = 38 V	–	–	$I_{CC}(max) + 3$	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –18 V, $T_J < T_J(max)$	–	–	–1	mA
Output Zener Clamp Voltage	$V_{Z(output)}$	I_{OUT} = 3 mA, T_A = 25°C	28	–	–	V
Output Zener Current	$I_{Z(output)}$	V_{OUT} = 28 V	–	–	3	mA
Output Current Limit	$I_{OUT(lim)}$		30	–	85	mA
Output Stage Characteristics						
Output Saturation Voltage	$V_{OUT(sat)}$	$I_{OUT(sink)}$ = 20 mA	–	220	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, output off	–	–	10	µA
Output Fall Time	t_f	R_{PU} = 1 kΩ, V_{PU} = 20 V, C_{OUT} = 10 pF	–	2	–	µs

[1]1 G (gauss) = 0.1 mT (millitesla).
[2]Maximum voltage operation must not exceed maximum junction temperature. Refer to Power Derating Curves chart.
[3]Time required to initialize device. Power-On Time includes the time required to complete the internal automatic offset adjust. The DAC is then ready for peak acquisition.

OPERATING CHARACTERISTICS (continued): valid throughout operating voltage and ambient temperature ranges using Allegro reference target 60-0, typical data applies at V_{CC} = 12 V and T_A = 25°C; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Performance Characteristics						
Operational Air Gap Range[2]	AG	D_{OUT} within specification	0.5	–	3.5	mm
Operating Magnetic Signal Range	B_{DIFF}	Peak-to-peak of differential signal; operation within specification	20	–	1200	G
Operate Point[3]	B_{OP}	See figure 5	–	120	–	mV
			3	–	10	G
Release Point[3]	B_{RP}	See figure 5	–	120	–	mV
			3	–	10	G
Operating Frequency	f_{OP}		0	–	10	kHz
Analog Signal Bandwidth	BW	Equivalent to f = –3 dB	20	–	–	kHz
Initial Calibration Cycle[4]	n_{cal}	Output rising edges before calibration is completed, 0 offset, $f_{OP} \leq 200$ Hz	–	–	3	edge
Output Duty Cycle Precision	D_{OUT}	Using a pure sine magnetic signal, with f_{OP} and B_{DIFF} within specification	–	–	±15	%
Output Period Precision	T_{OUT}	Using pure sine magnetic signal with B_{DIFF} = 50 G_{pk-pk} and f_{OP} = 1 kHz	–	0.3	–	%
Allowable User Induced Differential Offset	$B_{DIFFEXT}$	Output switching only	–60	–	60	G

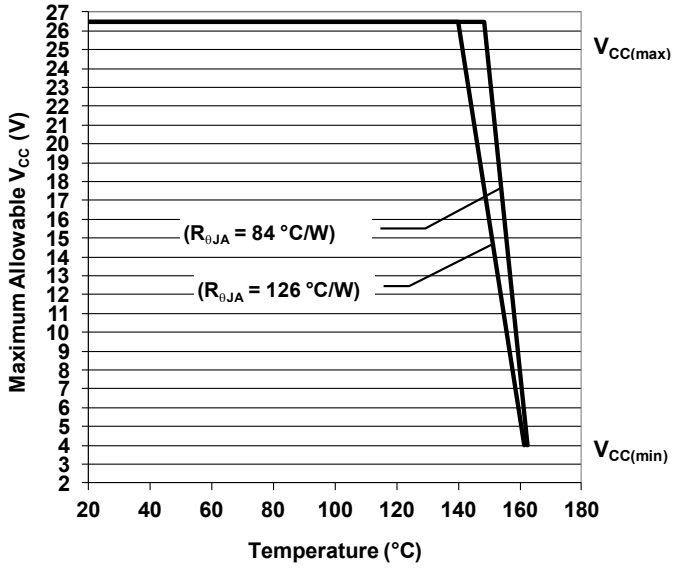
[1]1 G (gauss) = 0.1 mT (millitesla).
[2]AG is dependent on the available magnetic field. The available field is dependent on target geometry and material,and should be independently characterized. The field available from the reference target is given in the reference target parameter section of the datasheet.
[3]Values in G are based on device in maximum gain setting.
[4]Non-uniform magnetic profiles may require additional output pulses before calibration is complete.

Thermal Characteristics may require derating at maximum conditions, see Power Derating section

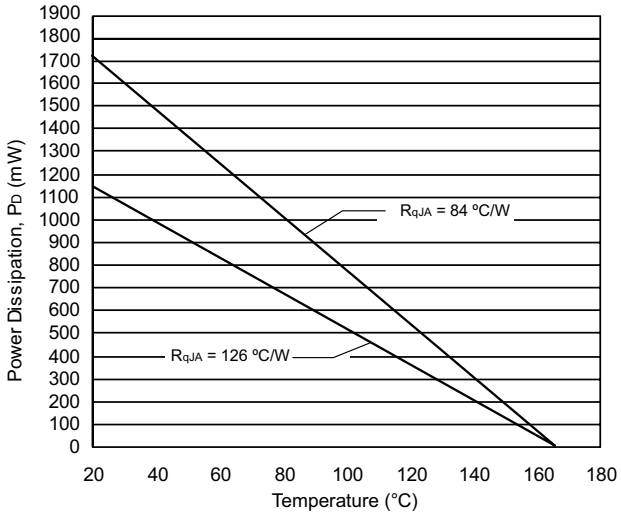
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single layer PCB, with copper limited to solder pads	126	°C/W
		Single layer PCB, with copper limited to solder pads and 3.57 in.^{2} (23.03 cm^2) copper area each side	84	°C/W

*Additional thermal information available on the Allegro website

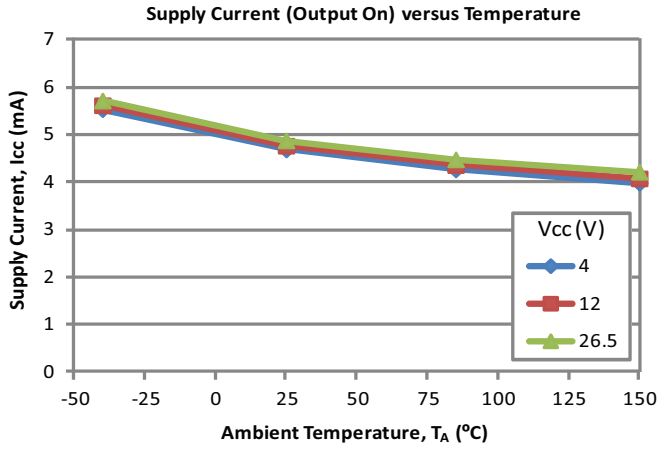
Power Derating Curve

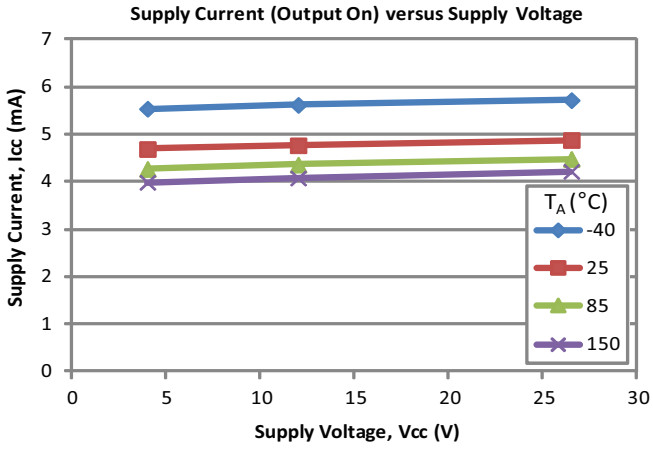


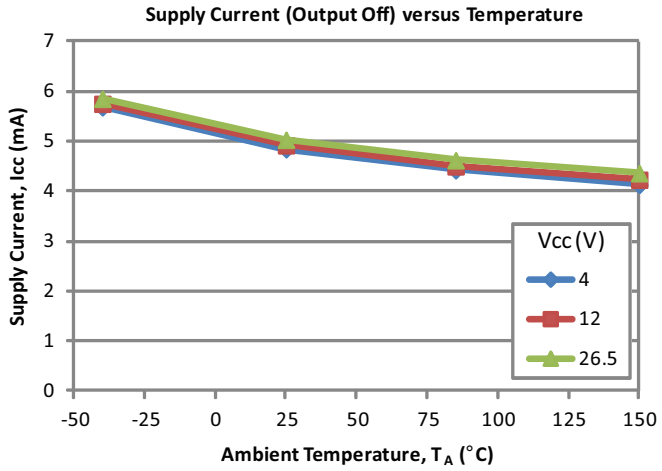
Power Dissipation versus Ambient Temperature

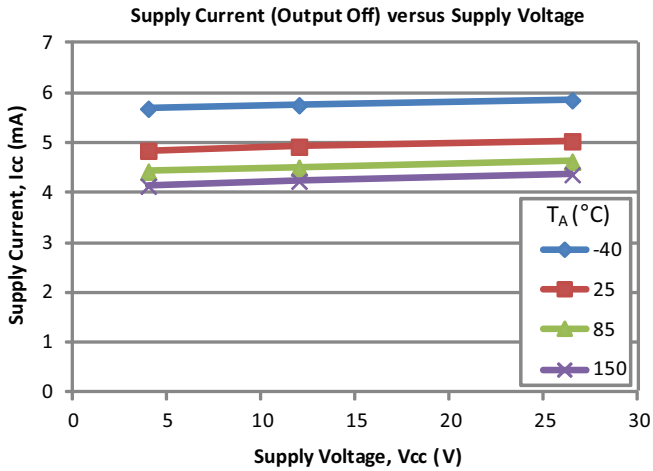


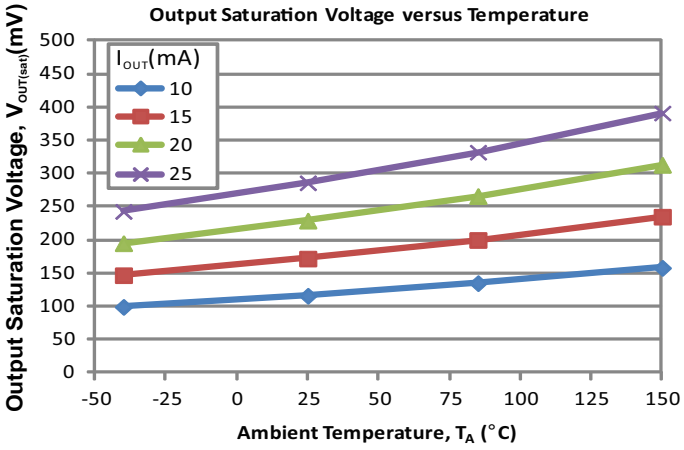
CHARACTERISTIC PERFORMANCE

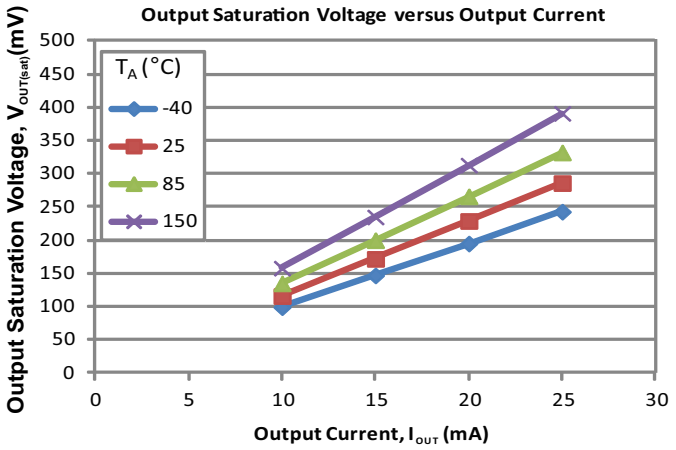






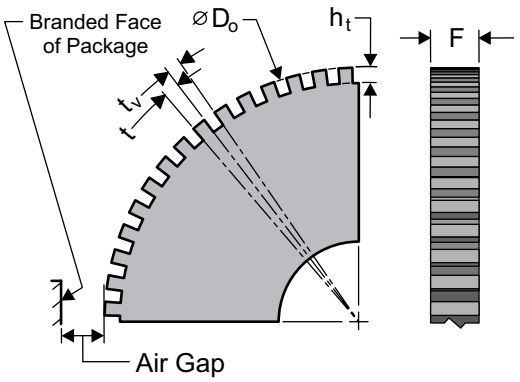


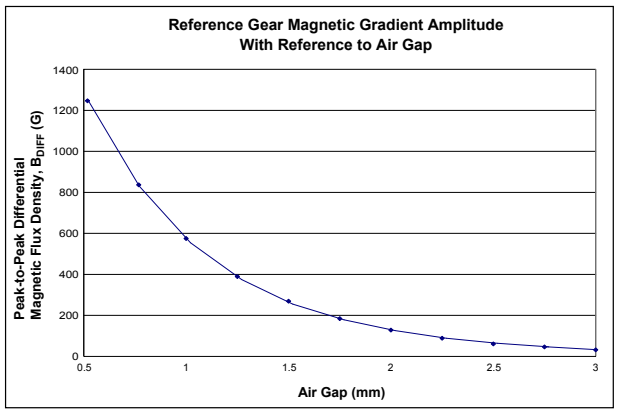


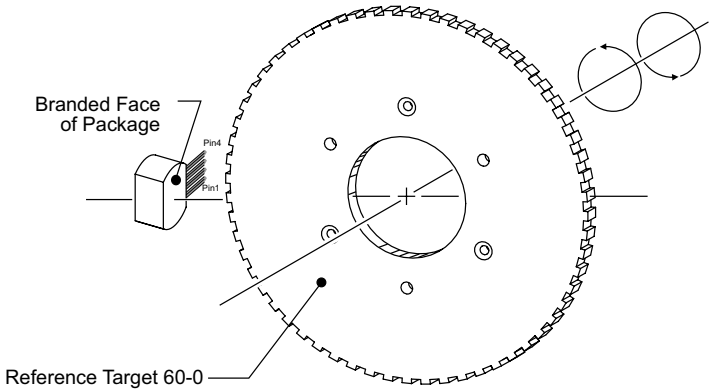


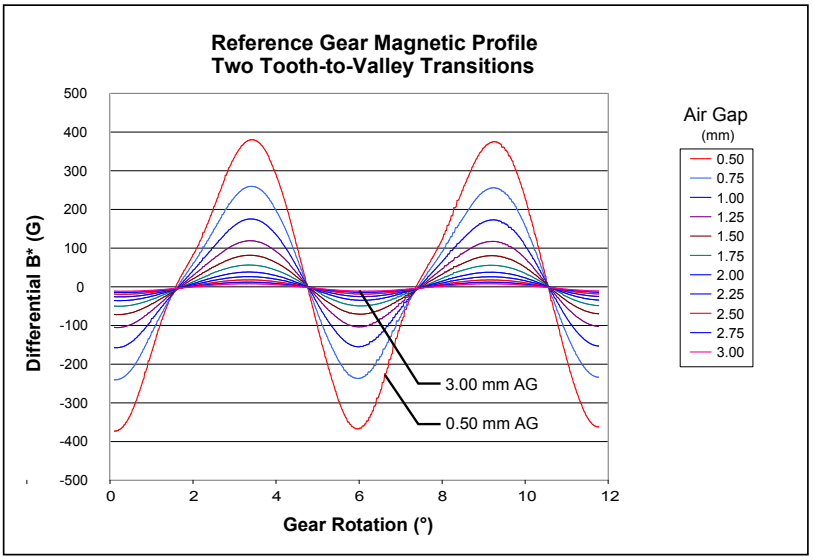
REFERENCE TARGET CHARACTERISTICS

Reference Target 60-0

Characteristics	Symbol	Test Conditions	Typ.	Unit	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Angular Tooth Thickness	t	Length of tooth, with respect to branded face; measured at D_o	3	deg.	
Angular Valley Thickness	t_v	Length of valley, with respect to branded face; measured at D_o	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	







FUNCTIONAL DESCRIPTION

Sensing Technology

The ATS468 contains a single-chip differential Hall-effect sensor IC, a permanent magnet pellet, and a flat ferrous pole piece (concentrator). As shown in Figure 1, the Hall IC supports two Hall elements, which sense the magnetic profile of the ferrous gear target simultaneously, but at different points (spaced at a 2.2 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature compensated amplifier and offset cancellation circuitry. The built-in voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset compensation circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling During Operation

An operating device is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in Figure 3 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the ATS468. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

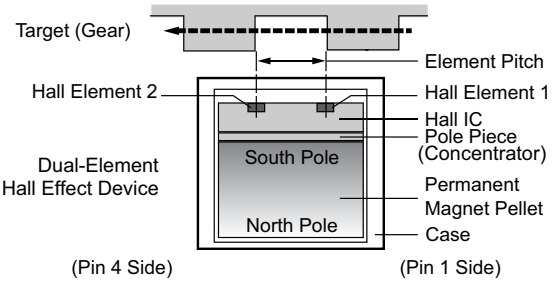


Figure 1: Relative Motion of the Target

Relative Motion of the Target is Detected by the Dual Hall Elements in the Hall IC.

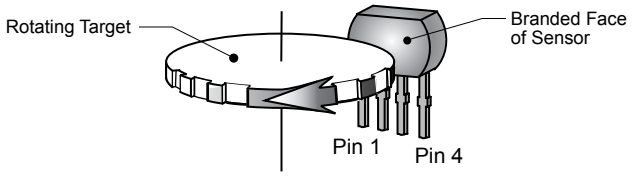


Figure 2: Left-to-Right Direction of Target Rotation

This left-to-right (pin 1 to pin 4) direction of target rotation results in a high output state when a tooth of the target gear is nearest the package face (see figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

Determining Output Signal Polarity

In Figure 3 the top panel, labeled Mechanical Position, represents the mechanical features of the target gear and orientation to the device. The bottom panel, labeled Device Output Signal, displays the square waveform corresponding to the digital output signal that results from a rotating gear configured as shown in Figure 2, and electrically connected as in Figure 6. That direction of rotation (of the gear side adjacent to the package face) is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side. This results in the IC output switching from low state to high state as the leading edge of a tooth (a rising mechanical edge, as detected by the IC) passes the package face. In this configuration, the device output switches to its high polarity when a tooth is the target feature nearest to the package. If the direction of rotation is reversed, so that the gear rotates from the pin 4 side to the pin 1 side, then the output polarity inverts. That is, the output signal goes high when a falling edge is detected, and a valley is nearest to the package.

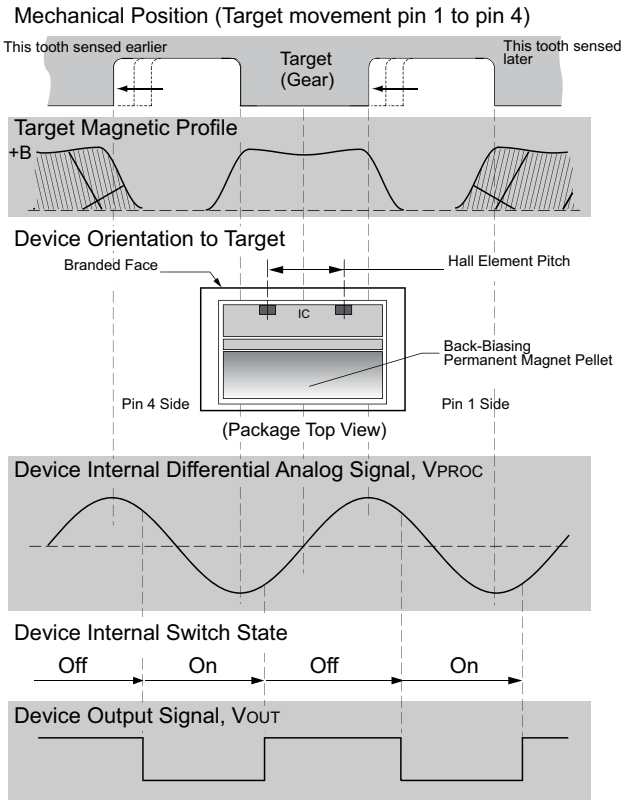


Figure 3: Magnetic Profile

The magnetic profile reflects the geometry of the target, allowing the ATS468 to present an accurate digital output response.

Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the differential signal amplitude (within the B_{DIFF} and $B_{DIFFEXT}$ specifications). During calibration, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain of the device is then automatically adjusted. Figure 4 illustrates the effect of this feature. During running mode, the AGC continues to monitor the system amplitude, reducing the gain if necessary; see the Device Operation section for more details.

Automatic Offset Adjust (AOA)

The AOA is patented circuitry that automatically compensates for the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including both during calibration mode and running mode, compensating for offset drift. Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

Digital Peak Detection

A digital DAC tracks the internal analog voltage signal, V_{PROC}, and is used for holding the peak value of the internal analog signal. In the example shown in Figure 5, the DAC would first track up with the signal and hold the upper peak's value. When V_{PROC} drops below this peak value by B_{OP}, the device hysteresis, the output would switch and the DAC would begin tracking the signal downward toward the negative V_{PROC} peak. After the DAC acquires the negative peak, the output will again switch states when V_{PROC} is greater than the peak by the value B_{RP}. At this point, the DAC tracks up again and the cycle repeats. The digital tracking of the differential analog signal allows the device to achieve true zero-speed operation.

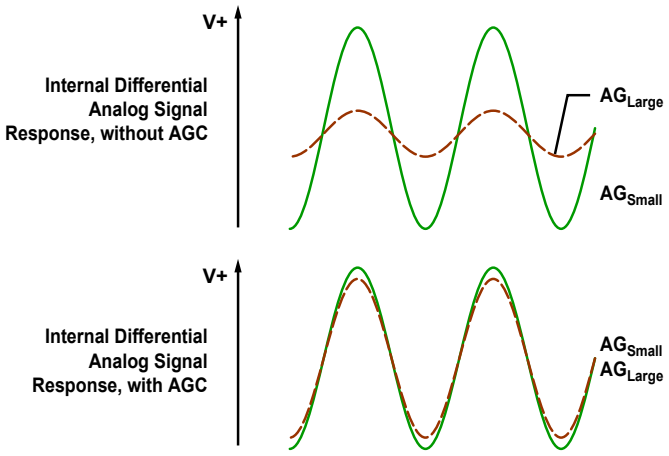


Figure 4: Automatic Gain Control (AGC)
The AGC function corrects for variances in the air gap. Differences in the air gap affect the magnetic gradient, but AGC prevents that from affecting device performance, as shown in the lowest panel.

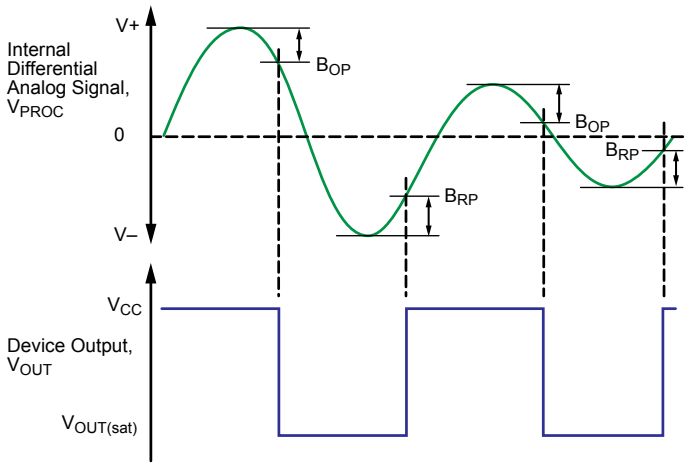


Figure 5: The Peaks in the Resulting Differential Signal are Used to Set the Operate, B_{OP}, and Release, B_{RP}, Switchpoints.

Power Supply Protection

The device contains an on-chip regulator and can operate throughout a wide V_{CC} range. For devices that must be operated from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/ RFI protection may still be required. Contact Allegro for information on the circuitry required for compliance with various EMC specifications. Refer to figure 6 for an example of a basic application circuit.

Undervoltage Lockout

When the supply voltage falls below the undervoltage lockout voltage, $V_{CC(uv)}$, the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied.

Assembly Description

This device is integrally molded into a plastic body that has been optimized for size, ease of assembly, and manufacturability. High operating temperature materials are used in all aspects of construction.

Device Operation

Each operating mode is described in detail below.

Power-On When power ($V_{CC} > V_{CC}$(min)) is applied to the device, a short period of time is required to power the various portions of the IC. During this period, the ATS468 powers-on in the high voltage state, V_{OUT}(high), and the digital tracking DAC gets ready to track the V_{PROC} signal. After power-on, there are conditions that could induce a change in the output state. Such an event could be caused by thermal transients, but would require a static applied magnetic field, proper signal polarity, and particular direction and magnitude of internal signal drift.

Initial Offset Adjust The device initially cancels the effects of chip, magnet, and installation offsets. After offsets have been cancelled, the device is ready to provide the first output switch. The period of time required for both Power-On and Initial Offset Adjust is defined as the Power-On Time.

Calibration Mode The calibration mode allows the device to automatically select the proper signal gain and continue to adjust for offsets. The AGC is active, and selects the optimal signal gain based on the amplitude of the V_{PROC} signal. Following each adjustment to the AGC DAC, the Offset DAC is also adjusted to ensure the internal analog signal is properly centered.

During this mode, the tracking DAC is active and output switching occurs, but the duty cycle is not guaranteed to be within specification.

Running Mode After the Initial Calibration period, CI, establishes a signal gain, the device moves to running mode. During running mode, the device tracks the input signal and gives an output edge for every peak of the signal. AOA remains active to compensate for any offset drift over time.

The ATS468 incorporates an algorithm for adjusting the signal gain during running mode. This algorithm is designed to optimize the V_{PROC} signal amplitude in instances where the magnetic

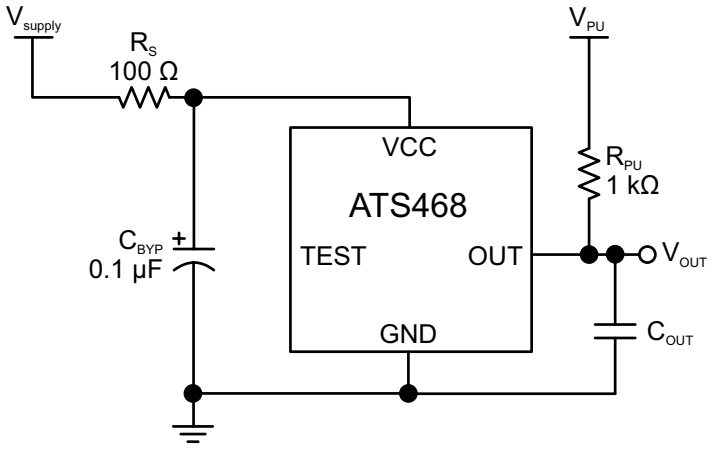


Figure 6: Typical Application Diagram

signal “seen” during the calibration period is not representative of the amplitude of the magnetic signal for the installed device air gap (see figure 7). Note that in this mode, the gain can be reduced but not increased, so this algorithm applies only to instances in which the magnetic signal amplitude during running is higher than that during calibration.

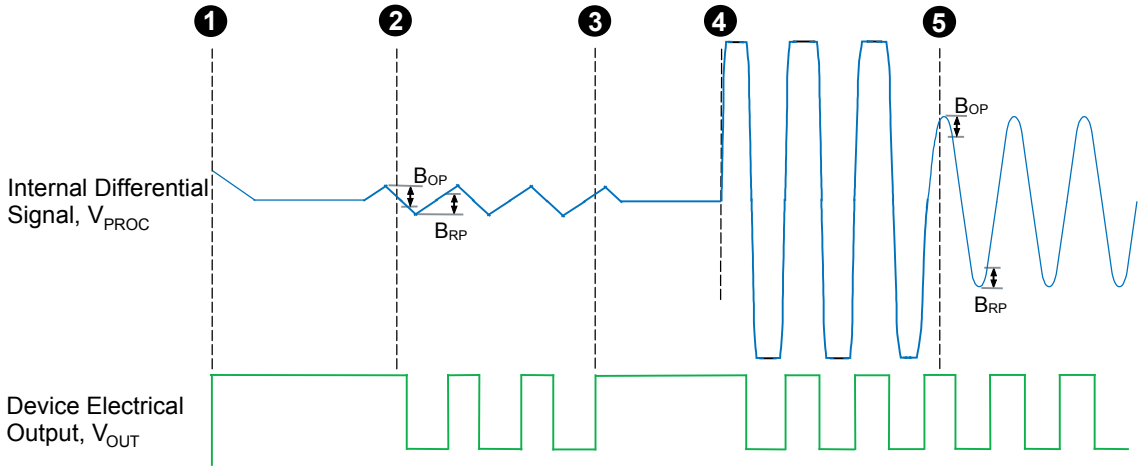


Figure 7: Operation of Running Mode Gain Adjust

• Position1. The device is initially powered-on. Self-calibration occurs.
• Position 2. Small amplitude oscillation of the target sends an erroneously small differential signal to the device. The amplitude of V_{PROC} is greater than the switching hysteresis (B_{OP} and B_{RP}), and the device output switches.
• Position 3. The calibration period completes on the third rising output edge, and the device enters running mode.
• Position 4. True target rotation occurs and the correct magnetic signal is generated for the installation air gap. The established signal gain is too large for the target rotational magnetic signal at the given air gap.
• Position 5. Running mode calibration corrects the signal gain to an optimal level for the installation air gap.

Power Derating

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 5 mA, and $R_{\theta JA}$ = 126 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 5\ mA = 60\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 60\ mW \times 126\ °C/W = 7.6°C$$

$$T_J = T_A + \Delta T = 25°C + 7.6°C = 32.6°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package SG or SJ using single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=126°C/W, T_J(max)=165°C, V_{CC}(max)= 26.5 V, and I_{CC}(max) = 7.5 mA.

Calculate the maximum allowable power level, P_D(max). First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 126\ °C/W = 119\,mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 119\,mW \div 7.5\ mA = 15.9\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤V_{CC}(est).

Compare V_{CC}(est) to V_{CC}(max). If V_{CC}(est) ≤ V_{CC}(max), then reliable operation between V_{CC}(est) and V_{CC}(max) requires enhanced $R_{\theta JA}$. If V_{CC}(est) ≥ V_{CC}(max), then operation between V_{CC}(est) and V_{CC}(max) is reliable under these conditions.

PACKAGE OUTLINE DRAWINGS

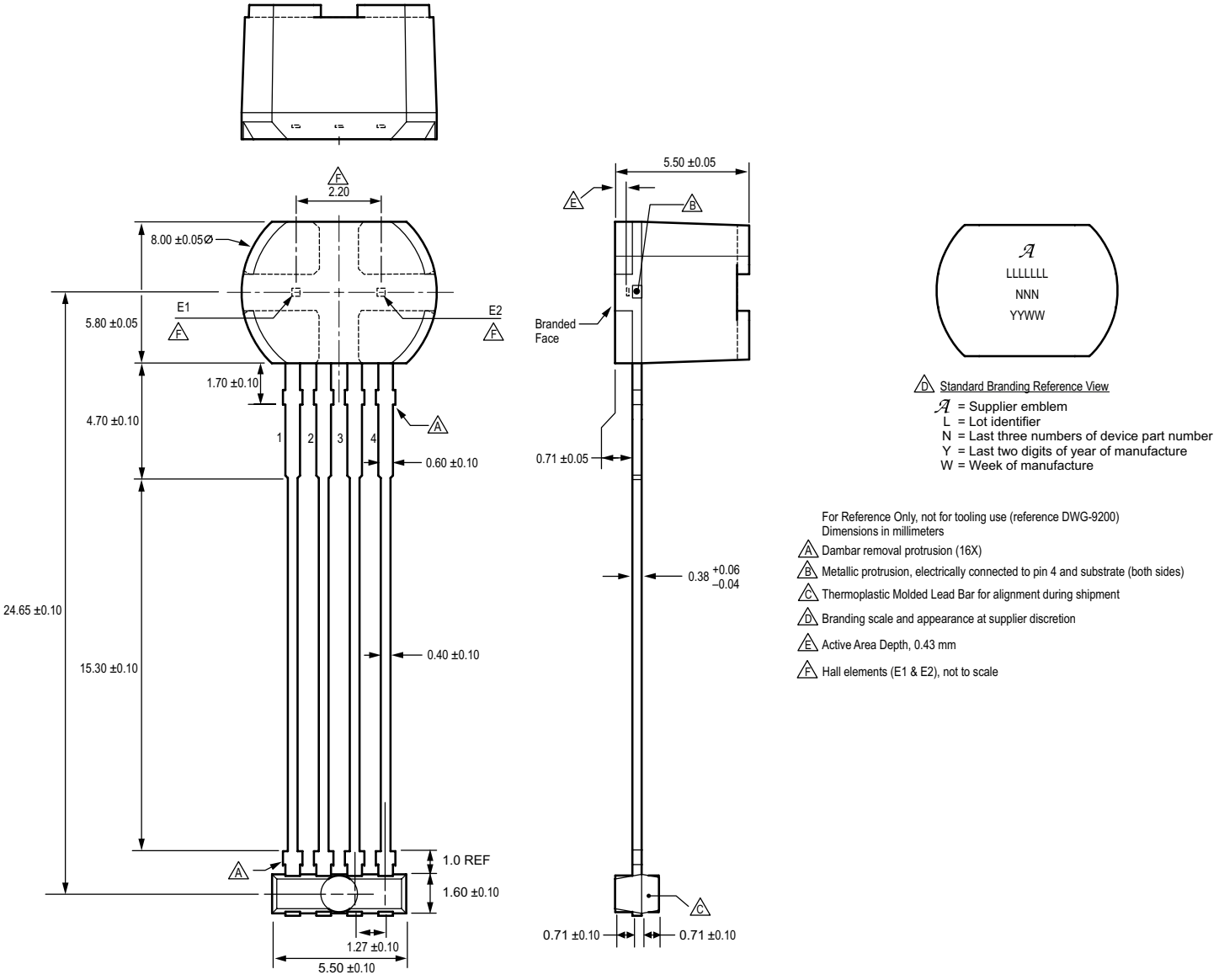
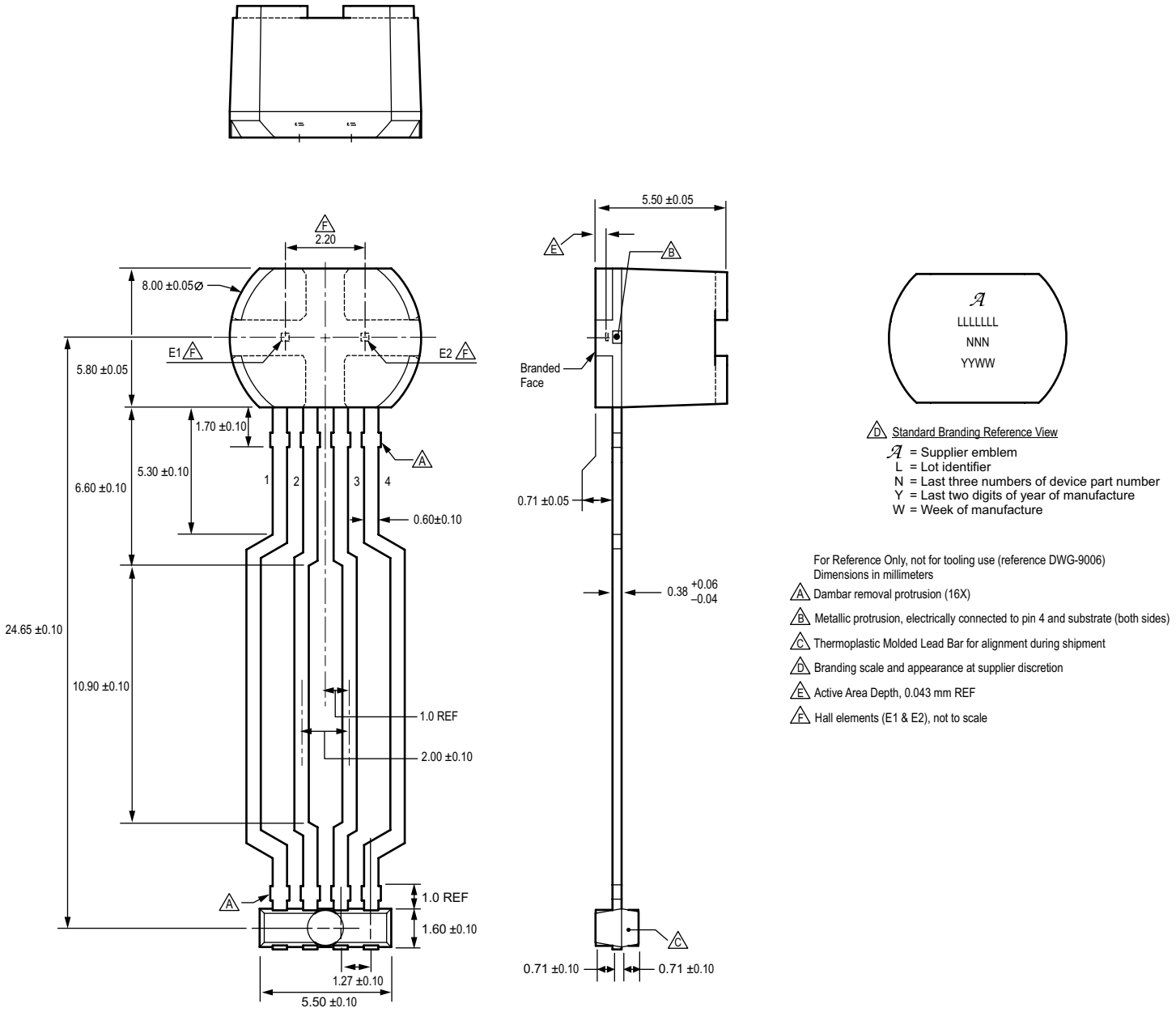


Figure 8: Package SG, 4-Pin SIP



Digure 9: Package SJ, 4-Pin SIP

Revision History

Revision	Current Revision Date	Description of Revision
–	September 29, 2014	Initial Release

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