Ordering number : ENA1457A

ATP301

P-Channel Power MOSFET
−100V, −28A, 75mΩ, ATPAK

ON Semiconductor®

http://onsemi.com

Features

- ON-resistance $R_{DS}(on)$=57mΩ (typ.)
- 10V drive
- Input capacitance Ciss=4000pF (typ.)
- Halogen free compliance

Specifications

Absolute Maximum Ratings at Ta=25°C

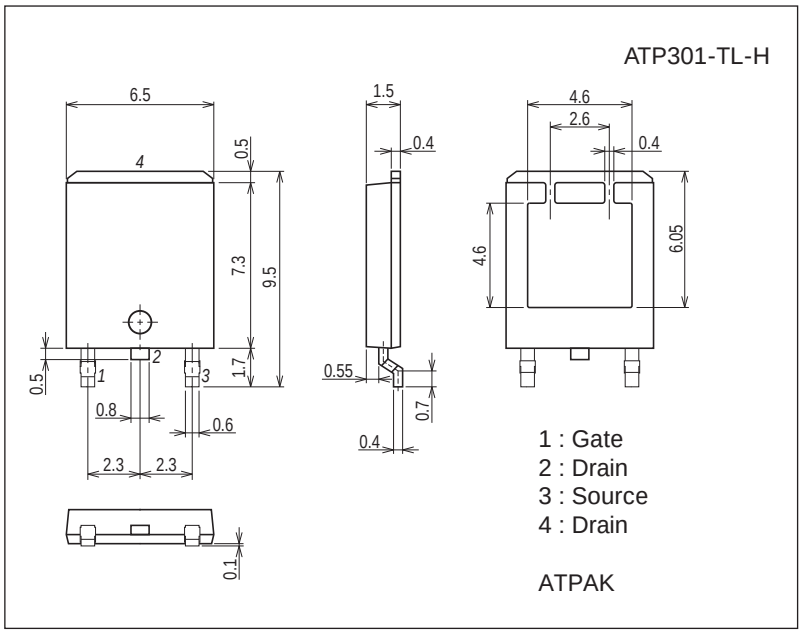
Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−100	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		−28	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	−112	A
Allowable Power Dissipation	P_D	Tc=25°C	70	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C
Avalanche Energy (Single Pulse) *1	E_{AS}		54	mJ
Avalanche Current *2	I_{AV}		−28	A

Note :*1 V_{DD}=−30V, L=100μH, I_{AV}=−28A
*2 L≤100μH, Single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

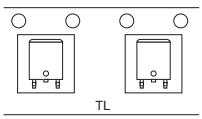
unit : mm (typ)
7057-001



Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

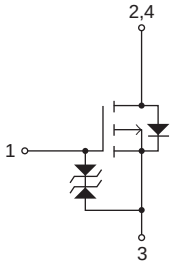
Packing Type: TL



Marking



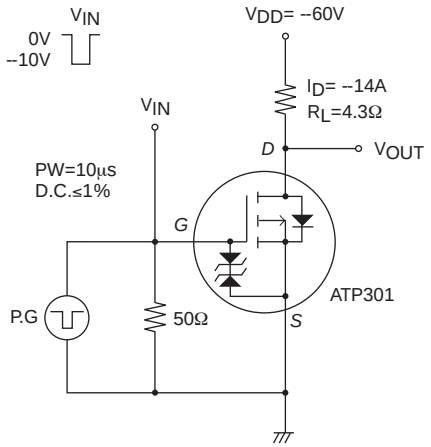
Electrical Connection



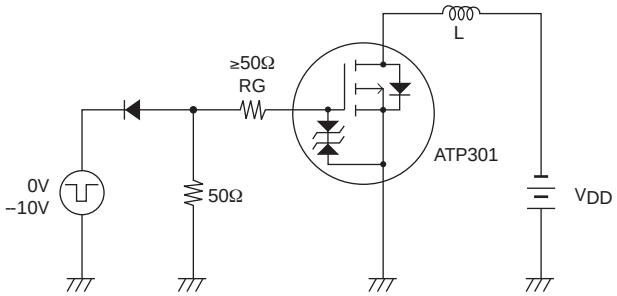
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−100			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−100V, V_{GS}=0V			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_D=−1mA	−2.0		−3.5	V
Forward Transfer Admittance	| yfs |	V_{DS}=−10V, I_D=−14A		32		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)	I_D=−14A, V_{GS}=−10V		57	75	mΩ
Input Capacitance	Ciss	V_{DS}=−20V, f=1MHz		4000		pF
Output Capacitance	Coss			270		pF
Reverse Transfer Capacitance	Crss			150		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		32		ns
Rise Time	t_r			130		ns
Turn-OFF Delay Time	$t_{d(off)}$			330		ns
Fall Time	t_f			190		ns
Total Gate Charge	Qg	V_{DS}=−60V, V_{GS}=−10V, I_D=−28A		73		nC
Gate-to-Source Charge	Qgs			16		nC
Gate-to-Drain “Miller” Charge	Qgd			14		nC
Diode Forward Voltage	V_{SD}	I_S=−28A, V_{GS}=0V		−1.0	−1.5	V

Switching Time Test Circuit

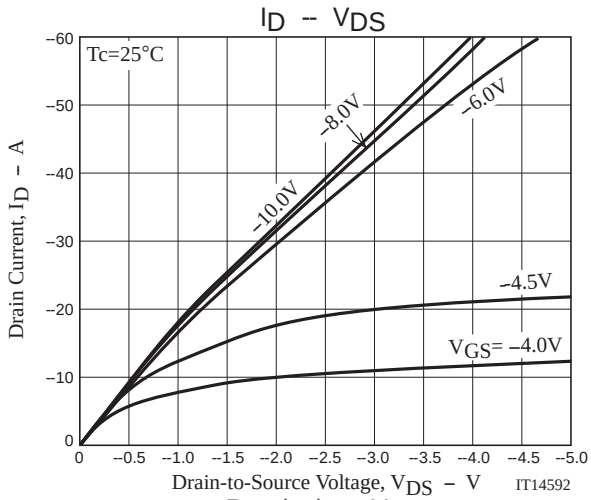


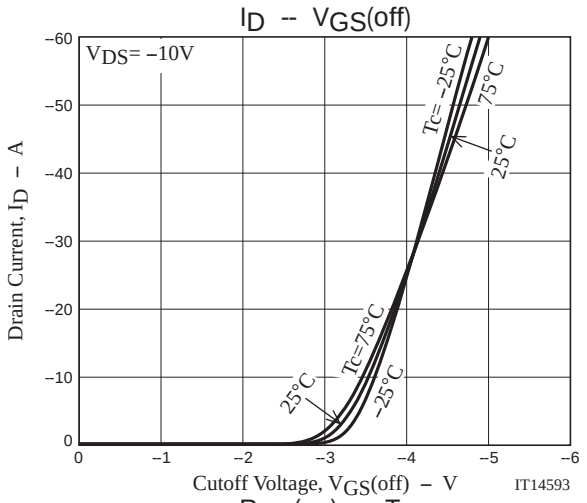
Avalanche Resistance Test Circuit

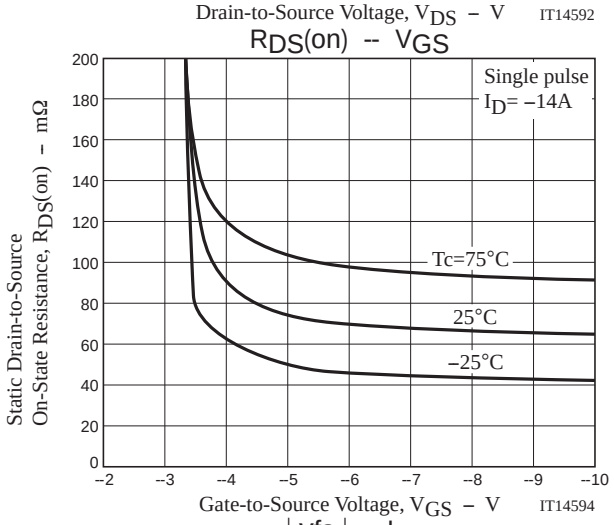


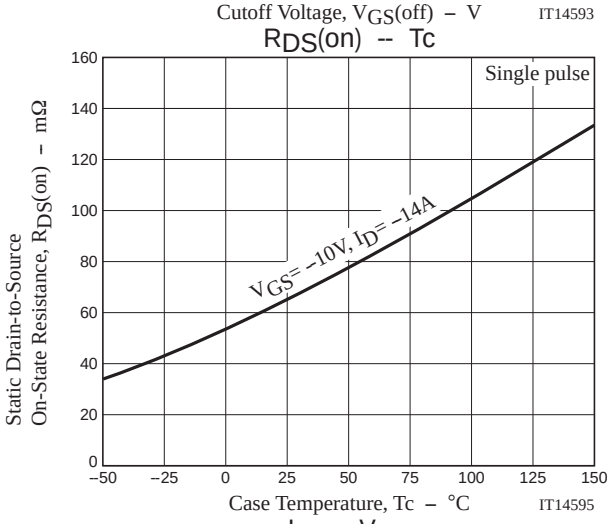
Ordering Information

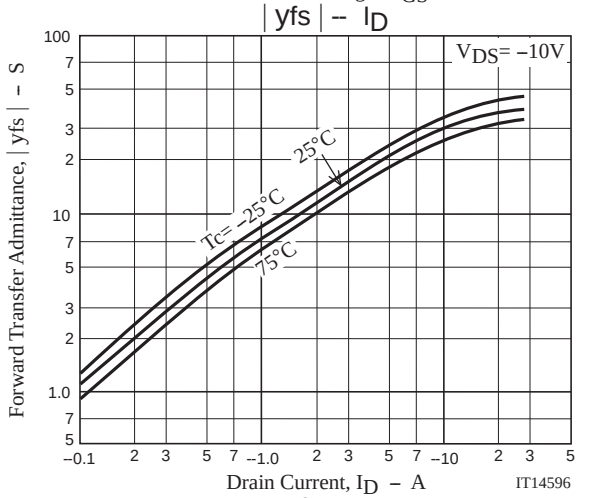
Device	Package	Shipping	memo
ATP301-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free

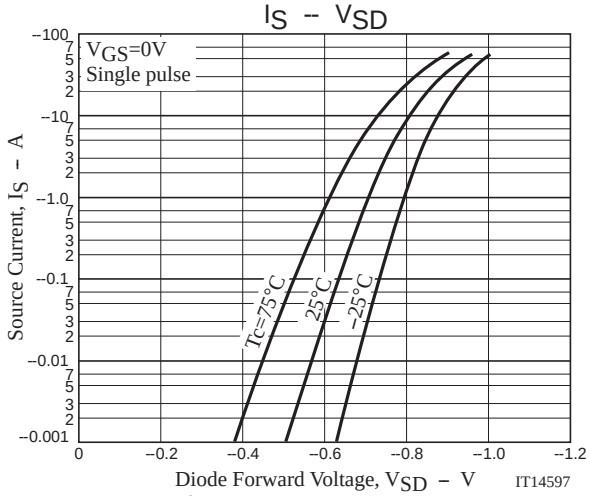

ID -- VDS
Tc=25°C
–8.0V
–6.0V
–10.0V
–4.5V
VGS= –4.0V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT14592

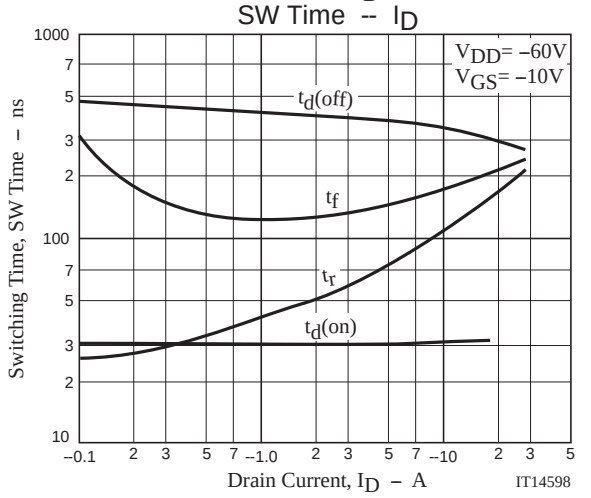

ID -- VGS(off)
VDS= –10V
Tc= –25°C
75°C
25°C
Tc=75°C
25°C
–25°C
Drain Current, ID – A
Cutoff Voltage, VGS(off) – V
IT14593

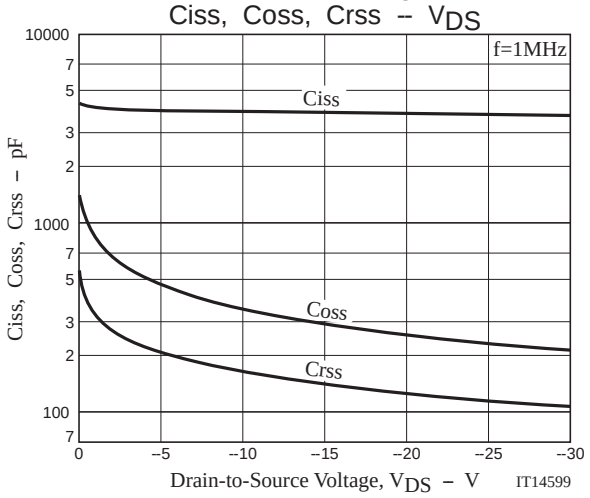

RDS(on) -- VGS
Single pulse
ID= –14A
Tc=75°C
25°C
–25°C
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT14594

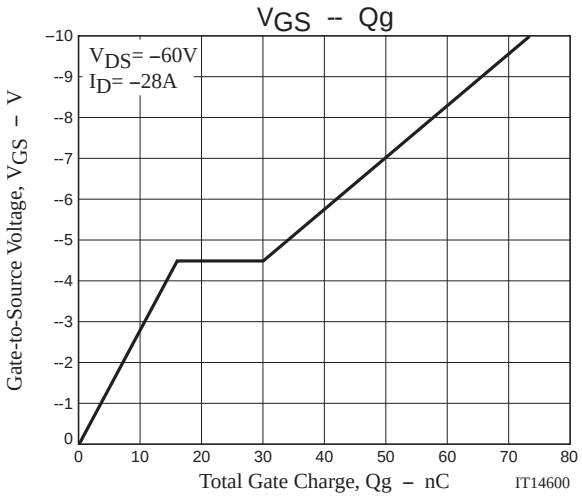

RDS(on) -- Tc
Single pulse
VGS= –10V, ID= –14A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Case Temperature, Tc – °C
IT14595

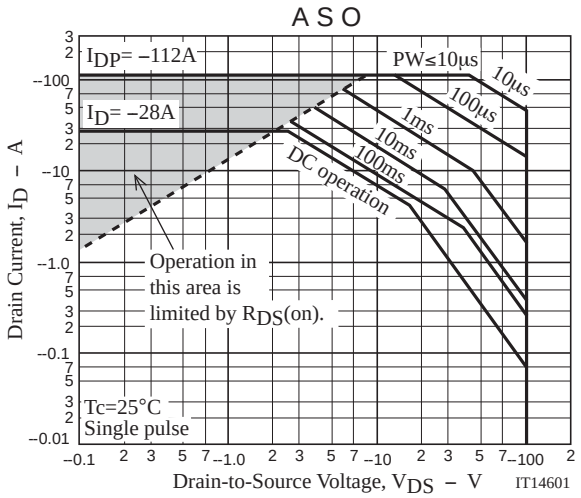

| yfs | -- ID
VDS= –10V
25°C
Tc= –25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT14596

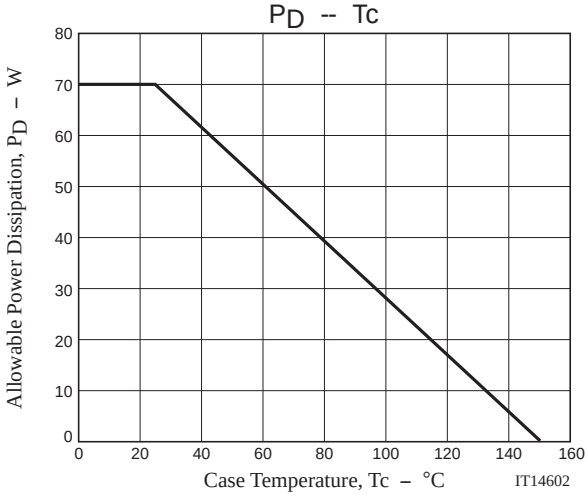

IS -- VSD
VGS=0V
Single pulse
Tc=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT14597

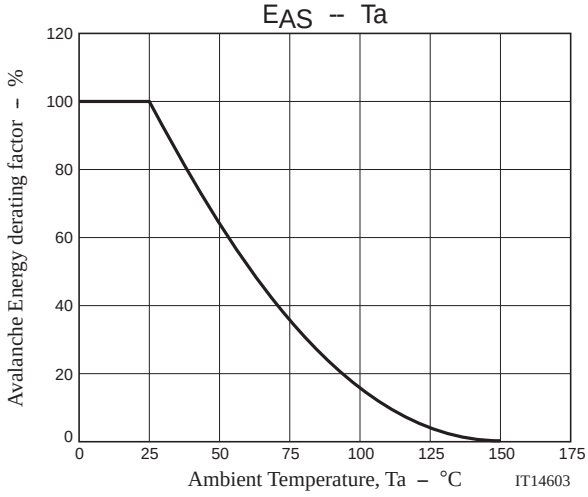

SW Time -- ID
VDD= –60V
VGS= –10V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT14598


Ciss, Coss, Crss -- VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT14599


VGS – Qg
VDS= –60V
ID= –28A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT14600


A S O
IDP= –112A
ID= –28A
PW≤10μs
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in this area is limited by RDS(on).
Tc=25°C
Single pulse
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT14601


PD -- Tc
Allowable Power Dissipation, PD – W
Case Temperature, Tc – °C
IT14602


EAS -- Ta
Avalanche Energy derating factor – %
Ambient Temperature, Ta – °C
IT14603

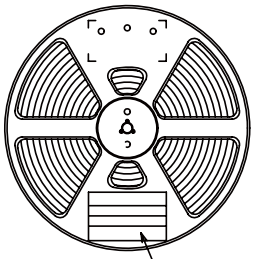
Taping Specification

ATP301-TL-H

1. Packing Format (TL)

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

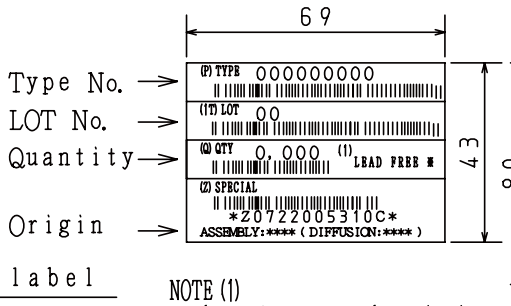
Packing method



Reel label

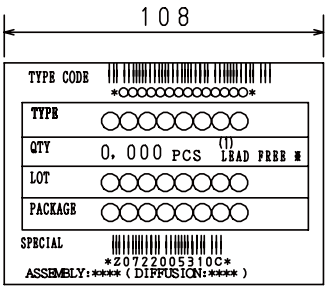
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



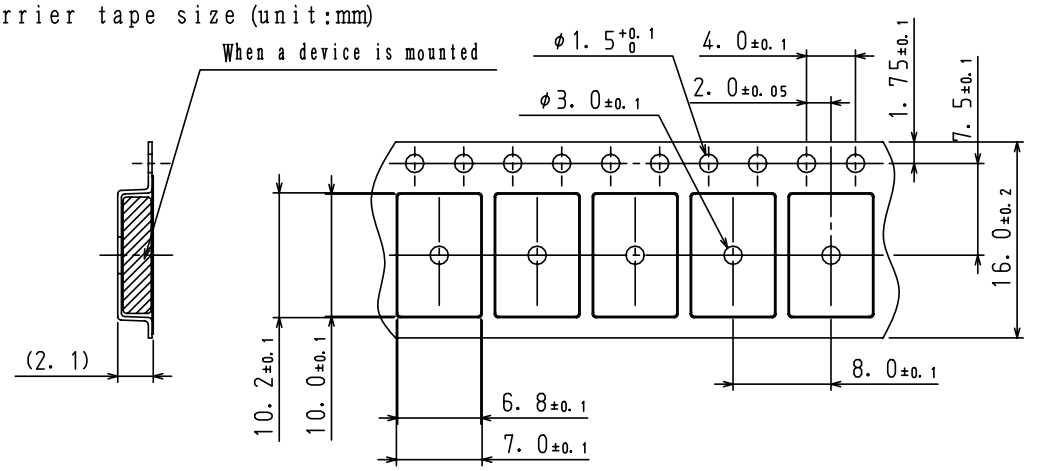
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

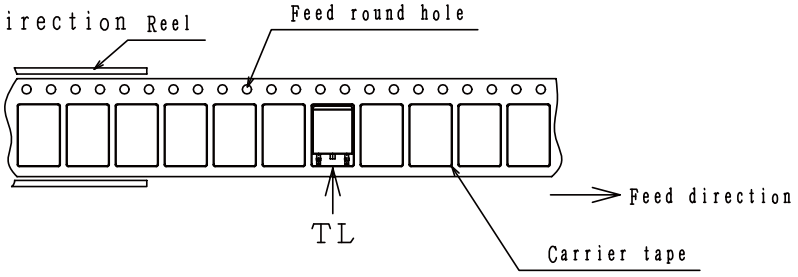
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



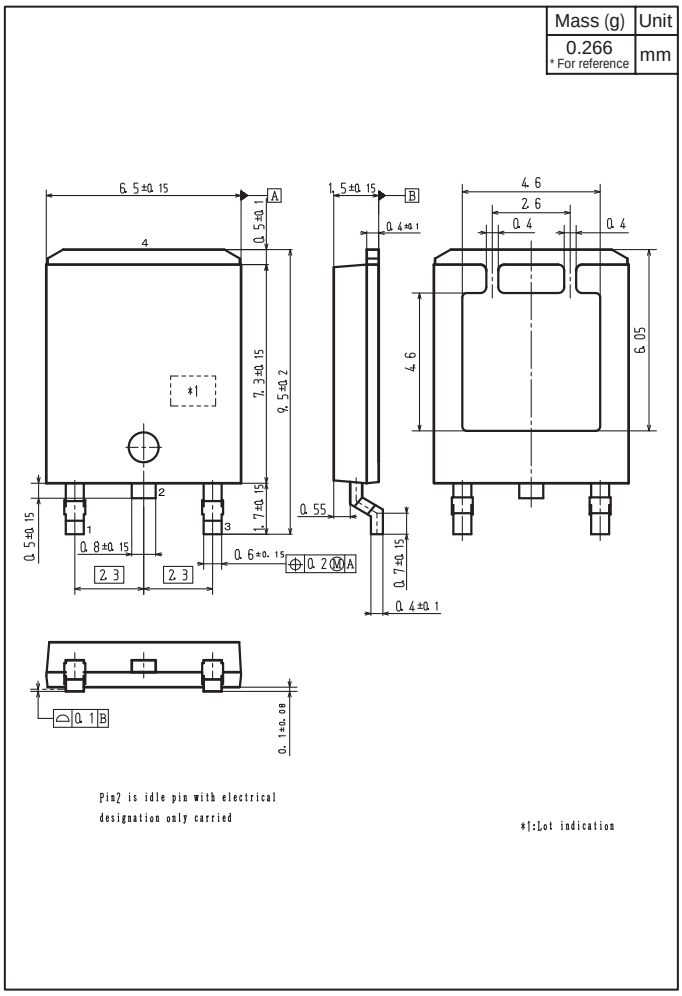
2-2. Device placement direction



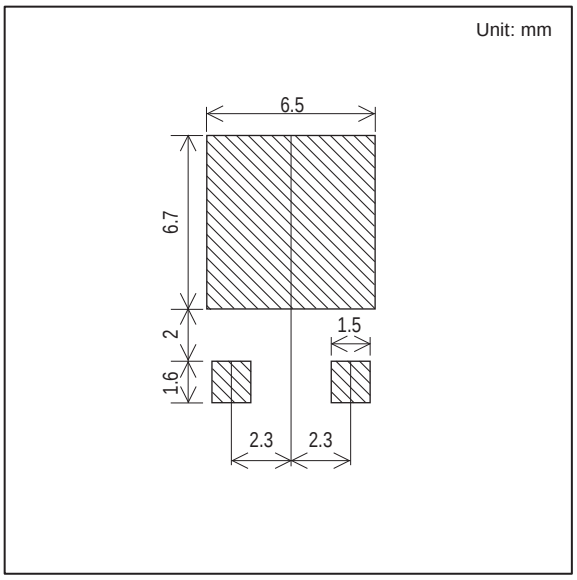
The one erectrode terminals on feed hole side····TL

Outline Drawing

ATP301-TL-H



Land Pattern Example



Note on usage : Since the ATP301 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.