Features

- 2nd Generation EE PROM-based Complex Programmable Logic Devices
  - V_{CCIO} of 5.0V or 3.3V with 3.3V Operation being 5V Tolerant
  - 32 - 256 Macrocells with Enhanced Features
  - Pin-compatible with Industry Standard Devices
  - Speeds to 5 ns Maximum Pin-to-pin Delay
  - Registered Operation to 250 MHz
- Enhanced Macrocells with Logic Doubling™ Features
  - Bury Either Register or COM while Using the Other for Output
  - Dual Independent Feedback Allows Multiple Latch Functions per Macrocell
  - 5 Product Terms per Macrocell, expandable to 40 per Macrocell with Cascade Logic, Plus 15 more with Foldback Logic
  - D/T/Latch Configurable Flip-flops plus Transparent Latches
  - Global and/or per Macrocell Register Control Signals
  - Global and/or per Macrocell Output Enable
  - Programmable Output Slew Rate per Macrocell
  - Programmable Output Open Collector Option per Macrocell
  - Fast Registered Input from Product Term
- Enhanced Connectivity
  - Single Level Switch Matrix for Maximum Routing Options
  - Up to 40 Inputs per Logic Block
- Advanced Power Management Features
  - ITD (Input Transition Detection) Available Individually on Global Clocks, Inputs and I/O for µA Level Standby Current for “L” Versions
  - Pin-controlled 1 mA Standby Mode
  - Reduced-power Option per Macrocell
  - Automatic Power Down of Unused Macrocells
  - Programmable Pin-keeper Inputs and I/Os
- Available in Commercial and Industrial Temperature Ranges
- Available in All Popular Packages Including PLCC, PQFP and TQFP
- EE PROM Technology
  - 100% Tested
  - Completely Reprogrammable
  - 10,000 Program/Erase Cycles
  - 20 Year Data Retention
  - 2000V ESD Protection
  - 200 mA Latch-up Immunity
- JTAG Boundary-scan Testing Port per IEEE 1149.1-1990 and 1149.1a-1993
  - Pull-up Option on JTAG Pins TMS and TDI
- IEEE 1532 Compatibility for Fast In-System Programmability (ISP) via JTAG
- PCI-compliant
- Security Fuse Feature

ATF15xxSE Family Datasheet

ATF1502SE(L)
ATF1504SE(L)
ATF1508SE(L)
ATF1516SE(L)

Preliminary

Rev. 2401D–PLD–09/02

General Description

Beginning with the introduction of the 100% connected ATF1500 with 32 enhanced macrocells in 1996, Atmel's CPLD products have delivered extra IO connectivity and logic reusability. Atmel's commitment to efficient, flexible architecture has continued with the current Atmel ATF15xxSE Family of industry-standard, pin-compatible CPLDs. Atmel's Logic Doubling architecture consists of wider fan-in, additional routing and clock options, combined with sophisticated, proprietary device fitters, extend CPLD place and route efficiency. Atmel enhanced macrocell includes double independent buried feedback that allows designers to pack more logic (particularly shifters and latches) into a smaller CPLD or leave spare room for later revisions. The Atmel ATF15xxSE family delivers enhanced functionality and flexibility with no additional design effort and is highly cost effective.

The Atmel ATF15xxSE Family includes all popular configurations and speeds.

Table 1. ATF15xxSE Family Device Features

Feature	ATF1502SE(L)	ATF1504SE(L)	ATF1508SE(L)	ATF1516SE(L)
Usable Gates	750	1500	3000	6000
Macrocells	32	64	128	256
Logic Blocks	2	4	8	16
Max. # Pins	44	100	256	256
Max. User I/Os	36	68	100	164
T_{PD} Grades (ns)	5, 6, 7, 10(15)	5, 6, 7, 10(15)	6, 7, 10(15)	7, 10(15)

The Atmel ATF15xxSE Family includes pin-compatible products in all popular packages.

Table 2. ATF15xxSE Family Device Packages and Number of Signal Pins[1][2]

Packages	ATF1502SE(L)	ATF1504SE(L)	ATF1508SE(L)	ATF1516SE(L)
44-pin PLCC	36	36		
44-pin TQFP	36	36		
84-pin PLCC		68	68	
100-pin TQFP		68	84	
100-pin PQFP			84	
160-pin PQFP			100	
208-pin PQFP				164
208-pin RQFP				164

Notes: 1. Contact Atmel for up-to-date information on device and package availability.
2. When the JTAG port is used for In System Programming (ISP) or Boundary-scan Testing (BST), the four associated pins become JTAG pins and are unavailable for user I/O.

Functional Description

The ATF15xxSE Family of 5.0 Volt supply, high-performance, high-density complex programmable logic devices (CPLDs) utilizes Atmel's proven electrically erasable non-volatile technology. With up to 512 macrocells, they easily integrate logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF15xxSE Family's enhanced macrocell architecture, switch matrices and routing increase usable gate count for new designs and increase odds of successful pin-locked design modifications while maintaining pin-compatibility with industry standard CPLDs.

The ATF15xxSE Family devices have four dedicated input pins and depending on the type of device and package, up to 208 bi-directional I/O pins. Each dedicated input pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell. Each input and I/O pin also feeds into the global bus.

The macrocells are organized into groups of sixteen called logic blocks. The switch matrix in each logic block selects 40 individual signals from the global bus. Macrocells within a given logic block may share their sixteen foldback signals on a regional foldback bus. Cascade logic between macrocells in the Logic Block allows fast, efficient generation of complex logic functions. All macrocells are capable of being I/Os, however, the actual number of I/O pins depends on the device and package type. The ATF15xxSE Family members contain two, four, eight, sixteen or thirty-two such logic blocks, each capable of creating sum term logic with a fan-in of 40 inputs from the switch matrix having access to up to 80 product terms.

Unused macrocells are automatically disabled by the fitter software to decrease power consumption. A security fuse, when programmed, protects the contents of the other fuses. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF15xxSE Family devices are in-system programmable (ISP) devices. They use the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and are fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Global Bus/Switch Matrix

The global bus (Figure 1) contains all input and I/O pin signals as well as the buried feedback signals from all macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Up to 40 of these signals can be selected as inputs to the individual logic blocks by the fitter software. Atmel's ATF15xx Family of CPLDs use a single level switch matrix signal distribution structure, where each logic block input has access to the same number of global bus inputs, maximizing the number of possible ways to route a global bus signal. This single level structure is in contrast with split switch matrix structures used by others in which routing a particular global bus input to a particular logic block input makes that signal unavailable to some other logic blocks, thus greatly limiting the available opportunities to route.

The ATF15xxSE Family macrocell, shown in Figure 2, consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, foldback bus, a flip-flop and output buffer. Extra fan-in and signal routing are provided throughout. Each macrocell can generate a foldback logic term from the product term mux and a buried feedback with extra routing that go to the global bus.

Figure 1. ATF15xxSE Family Typical Block Diagram

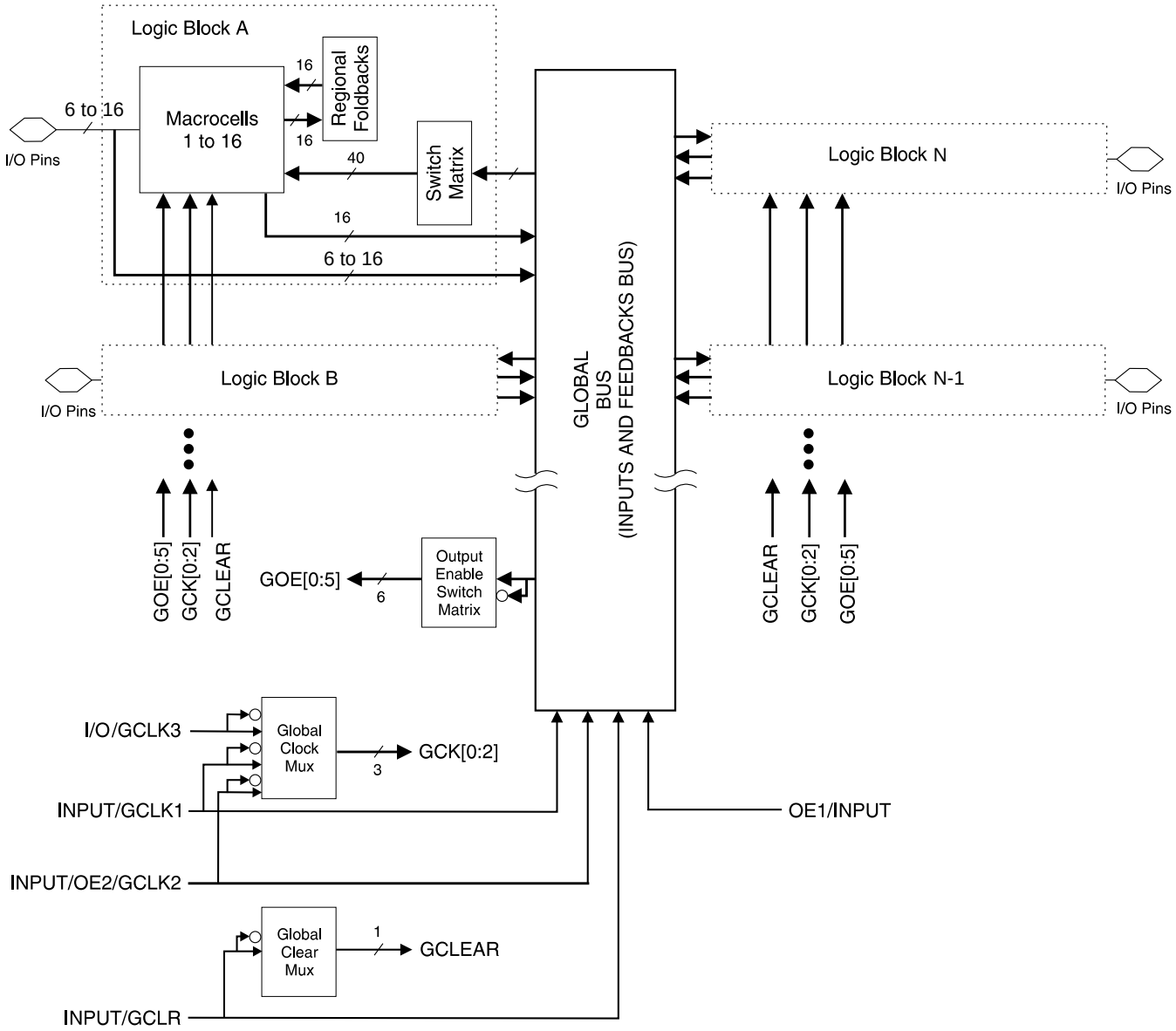
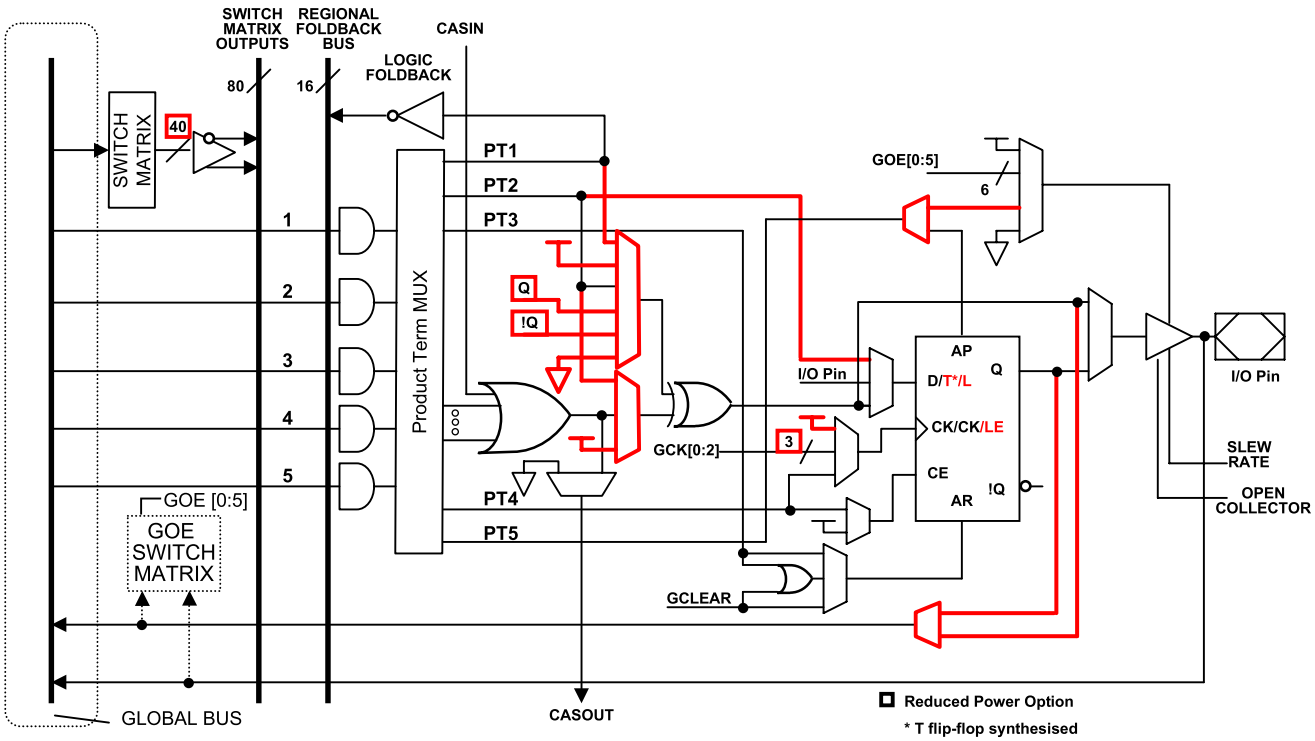


Figure 2. ATF15xxSE Family Macrocell with Enhanced Features In Red



Product Terms and Select Mux

Within each macrocell are five product terms. Each product term may receive as its inputs any combination of the signals from the switch matrix or regional foldback bus. The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the fitter software, which selects the optimum macrocell configuration.

OR/XOR/ CASCADE Logic

Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with little additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate may be fed from the flip-flop output to emulate T- and JK-type flip-flops, or fed to the buried feedback to synthesize an extra latch.

Foldback Bus

Each macrocell can also generate a foldback product term. This signal goes to the regional bus and is available to the 16 macrocells in a given logic block. The foldback is an inverse polarity of one of the macrocell's product terms. Although Cascade Logic is the preferred method for expanding the number of macrocell inputs to as many as 40, the 16 foldback terms in each region can also generate additional fan-in sum terms with nominal additional delay.

Flip-flop

The ATF15xxSE Family's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output or vice-versa. (This enhanced function is automatically implemented by the fitter software). The flip-flop can be configured for D, T, JK and SR operation, and changes state on the clock's rising edge. It can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

When a GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop has asynchronous reset and preset. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Extra Feedback

The ATF15xxSE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered. (This enhanced function is automatically implemented by the fitter software) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

I/O Control

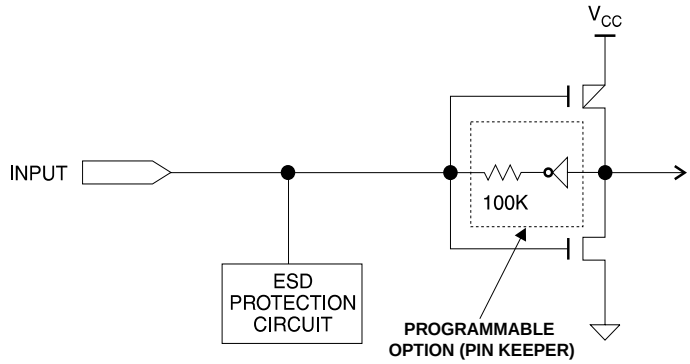
The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

The buffer has a fast/slow slew rate option to control EMI and an open-collector option which enables the device to provide control signals such as an interrupt that can be asserted by any of the several devices.

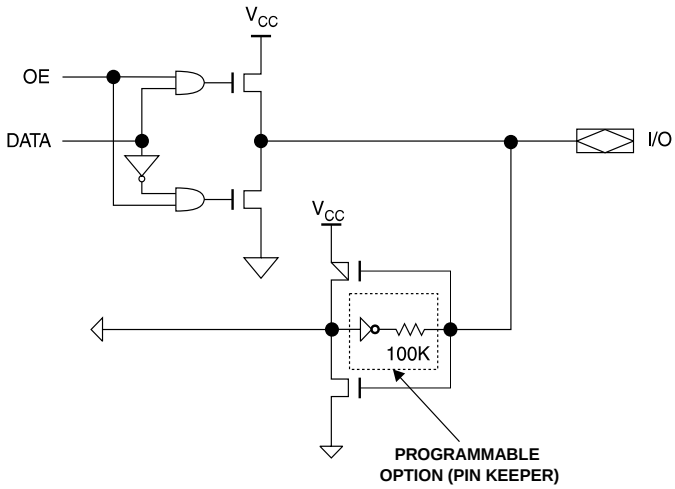
Programmable Pin-keeper Option for Inputs and I/Os

The ATF15xxSE Family offers the option of programming all input and I/O pins with pin-keeper circuits enabled. When any pin is driven high or low and then subsequently left floating, the pin keeper circuit will hold it at that previous high or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The pin-keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram



I/O Diagram



Speed/Power Management

The ATF15xxSE Family has several speed and power management features.

Multiple Power Supplies, Power Sequencing and Hot-Socketing

Because the ATF15xxSE Family can be used in a system with mixture of power supplies, it has been designed to function with the V_{CCINT} and V_{CCIO} power supplies applied in any sequence. Also, until the power up sequence completes, the input/output buffers are kept in a high impedance state, and so may be driven but do not drive power out.

Power-on Reset

The ATF15xx Family devices are designed with a power-on reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D.

The ATF15xx Family has two options for the hysteresis about the reset level, V_{RST}, Small and Large. In applications where the supply voltage may drop below 4.0V, Atmel recommends that during the fitting process users configure the device with the Power-on Reset hysteresis set to Large to ensure a robust operating environment.

Power Down of Unused Macrocells

To conserve power, Atmel fitters automatically power down all unused macrocells.

Input Transition Detection/ Automatic Power Down

The ATF15xxSEL versions provide automatic power-down to µA level stand-by power (the “L” suffix indicates “Low” power) through Atmel’s patented Input Transition Detection (ITD) circuitry on Global Clocks, Inputs and I/O. These ITD circuits automatically put the device into a low-power standby mode when no logic transitions are occurring. This reduces power consumption during inactive periods, and so provides proportional power savings for most applications running at system speeds below $f_{CRITICAL}$ (~5 MHz).

In clocked applications, where the device is operated at a frequency high enough to keep the device from going into stand-by (above $f_{CRITICAL}$), the device will perform at the faster speeds given in the next faster speed column. These higher speeds can be achieved in combinatorial designs as well, as long as once activated by an initial input transition, the device continues to receive input transitions often enough to keep the device from going into standby mode again. That is, the time between input transitions is less than $1/f_{CRITICAL}$.

Reduced-Power per Macrocell

To further reduce power, each ATF15xxSE Family macrocell has a reduced-power bit feature. With this feature the designer can reduce power by 50% or more for logic that does not need to operate at the maximum switching speed. The reduced-power bit may be activated by changing the default OFF to ON for any or all macrocells. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced- power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}. All power-down AC characteristic parameters are computed from external input or I/O pins, with the reduced-power bit turned on.

Slew Rate Control

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching. The slew rate option is selected in the design source file.

Pin Controlled Power-down

All ATF15xx Family devices also have an optional pin-controlled power-down mode. When activated, one or both of two pins, PD1 and PD2, can act as power-down pins. The device goes into power-down when either PD1 or PD2 pins (or both) are high, and the device supply current is reduced to less than 1 mA. Also, all internal logic signals are latched and held, as are any enabled outputs. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. Input and I/O hold

latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled for PD1 or PD2, that pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals. The power-down option is selected in the design source file.

Power Consumption Estimates

An estimate of power consumption can be made based on typical designs and operation conditions, but because it is sensitive to these factors, power consumption must be verified with actual pattern and operation conditions. The equations given below are based on a pattern of 16-bit up/down counters in each logic block and may be used to estimate power consumption for both operating modes.

Standby Power

1. $P_{standby} = I_{ccstandby} \times V_{supply}$

Where:

$I_{ccstandby}$ = the standby current given for the particular device and standby mode (e.g. pin controlled Power Down)

V_{supply}= the power supply voltage

Active Power

2. $P_{active} = P_{internal} + P_{load} = I_{ccinternal} \times V_{supply} + P_{load}$

Where:

$I_{ccinternal}$ = the internal current estimated from equation 3 below

V_{supply}= the power supply voltage

P_{load} = depends on the device output load capacitance and switching frequency on each output pin.

P_{load} and additional power savings at low frequencies using Atmel Input Transition Detection ("L" versions) can be estimated according to the methods discussed in the Atmel Application Note "Saving Power with Atmel PLDs"

3. $I_{ccinternal} = [K_1 \times (MC_{inuse} - MC_{reducedpower})] + (K_2 \times MC_{reducedpower}) + (K_3 \times MC_{inuse} \times f_{op} \times NS)$

Where:

$MC_{reducedpower}$ = the number of macrocells operating at reduced power (from fitter report file)

MC_{inuse}= the number of macrocells in use (from fitter report file. Unused macrocells are powered down.)

NS = the proportion of logic nodes switching (typically 10-20%)

f_{op} = the switching frequency

K_1, K_2, and K_3 = device constants given in the table below.

Device	K_1 (mA/MC)	K_2 (mA/MC)	K_3 (mA/MC · MHz)
ATF1502SE	0.6	0.3	0.015
ATF1504SE	0.6	0.3	0.015
ATF1508SE	0.6	0.3	0.015
ATF1516SE	0.6	0.3	0.015

Note: Shaded data is preliminary and subject to change without notice.

Design Software

Atmel ATF15xxSE Family fitters allow logic synthesis using a variety of high-level description languages and formats. ATF15xxSE Family designs are supported by Atmel specific design tools as well as by several third-party tools. Free conversion software is also offered for industry standard devices. Check the Atmel web site or contact your authorized Atmel sales representative for up-to-date design software information.

Programming

ATF15xxSE Family devices can be programmed using standard third-party programmers. With third-party programmers, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic. Check the Atmel web site, contact your authorized Atmel sales representative or Atmel PLD Applications for details of third-party programmers.

ATF15xxSE Family devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes. Atmel provides ISP hardware and software to allow programming of the ATF15xxSE Family via the PC. ISP is performed by using either a download cable, a compatible board tester or a simple microprocessor interface.

It is most common to devote the JTAG pins to ISP, but it is possible to use ISP to program the part through the JTAG pins, and set these four pins I/O pins. However, this will effectively disable further ISP and the device will need to be erased on a programmer to re-enable ISP. Contact Atmel PLD Applications by email at pld@atmel.com or call our Hotline at (408) 436-4333 for details.

To allow ISP programming support by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by the Atmel ISP software. Conversion to other ATE tester formats is also possible. Check the Atmel web site for up-to-date programming and software support information.

ISP Programming Protection

The ATF15xxSE Family also incorporates a protection feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF15xxSE Family devices are initially shipped in the erased state thereby making them ready to use for ISP.

For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF15xxSE Family fuse patterns. Once programmed, fuse verify is inhibited. However, the User Signature and device ID remain accessible.

JTAG-BST Overview

The JTAG-BST (JTAG boundary-scan testing) is controlled by the Test Access Port (TAP) controller. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own Boundary-scan Cell (BSC) in order to support boundary-scan testing. The ATF15xxSE Family does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The ATF15xxSE Family implements six BST instructions, and seven Atmel-defined In System Programming (ISP) instructions. All ATF15xx Family BST and ISP instructions have a length of 10 bits.

JTAG BST Instructions	Description
SAMPLE/PRELOAD	Captures signals at the device pins for later examination, or loads a data pattern prior to an EXTEST instruction.
EXTEST	Allows testing of off-chip circuitry and interconnections by forcing a pattern on the output pins or capturing signals from the input pins.
BYPASS	Places a single shift register stage between TDI and TDO, allowing test BST data to pass through a particular device in a chain of devices.
IDCODE	Places the 32-bit IDCODE register between TDI and TDO, allowing the IDCODE data to be shifted out of TDO.
UESCODE	Places the 16-bit user electronic signature register between TDI and TDO, allowing the UESCODE data to be shifted out of TDO.
HIGHZ	Places the BYPASS register between TDI and TDO in a high impedance mode, protecting the device from damage from externally applied test signals.
7 ISP instructions	These seven instructions allow in-system programming via the four JTAG pins.

The ATF15xxSE Family BST implementation complies with the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF15xxSE Family.

The ATF15xxSE Family also has the option of using four JTAG-standard I/O pins for in-system programming (ISP). The ATF15xxSE Family is programmable through the four JTAG pins using programming-compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins. Refer to Atmel Application Note “Designing for In-System Programmability with Atmel CPLDs for more details.

JTAG Boundary-scan Cell (BSC) Testing

The ATF15xxSE Family has four dedicated input pins and a number of I/O pins depending on the device type and package type selected. Each input pin and I/O pin has a boundary-scan cell (BSC) which supports boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller.

Device	Boundary-Scan Register Length	IDCODE MSB LSB
ATF1502SE	96	0000,0001,0101,0100,0010,0000,0011,1111
ATF1504SE	192	0000,0001,0101,0100,0100,0000,0011,1111
ATF1508SE	352	0000,0001,0101,0100,1000,0000,0011,1111
ATF1516SE	672	0000,0001,0101,0101,0000,0000,0011,1111

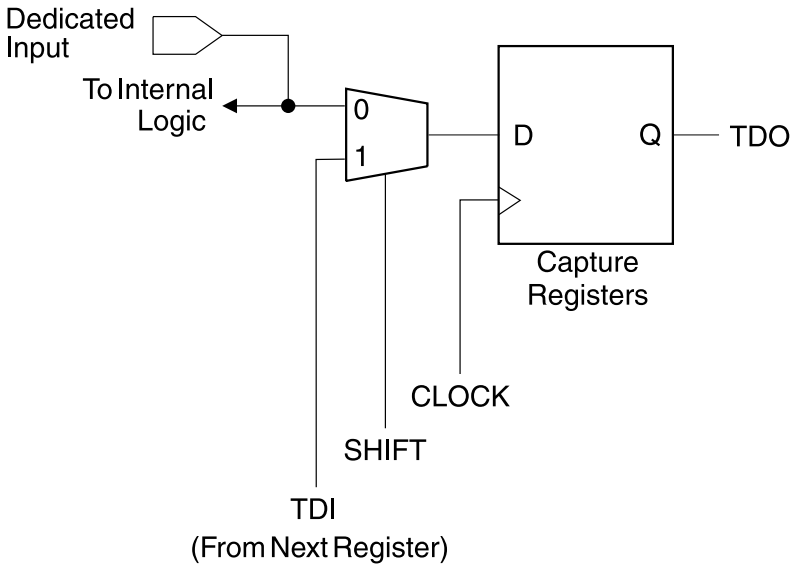
Note: Shaded data is preliminary and subject to change without notice.

Boundary-scan Definition Language (BSDL) Models

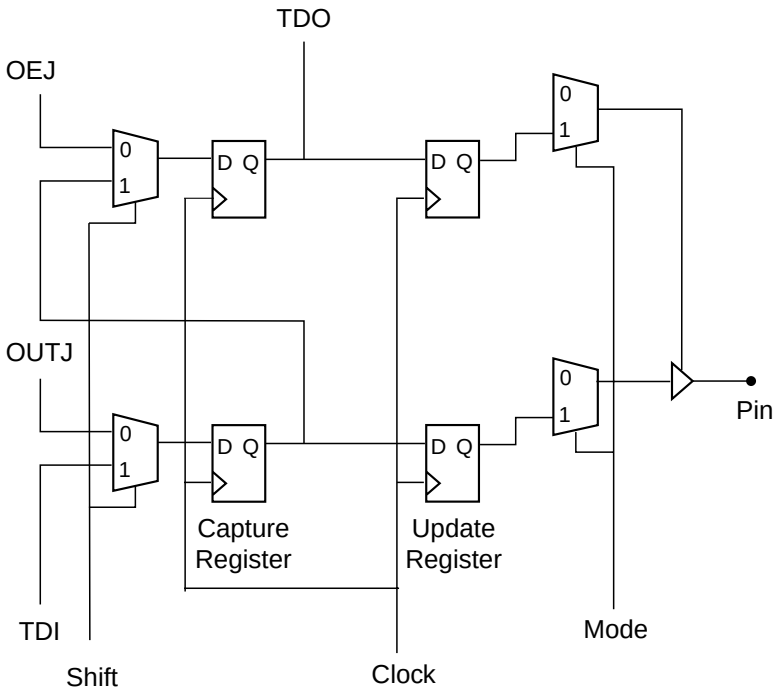
These are now available in all package types via the Atmel web site. These models conform to the IEEE 1149.1 standard and can be used for Boundary-scan Test Operation of the ATF15xxSE Family.

The BSC configuration for the input and I/O pins and macrocells are shown on page 13.

BSC Configuration for Pins (Except JTAG TAP Pins)



BSC Configuration for Macrocell

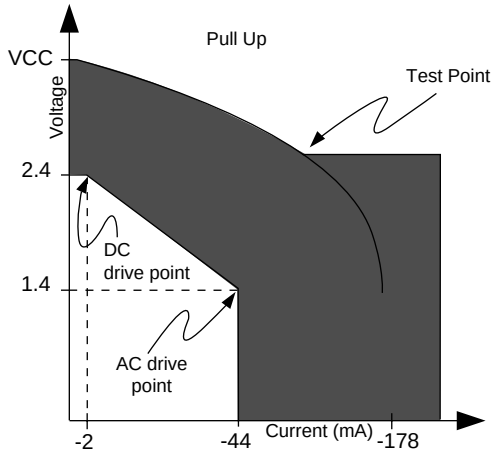


Macrocell BSC

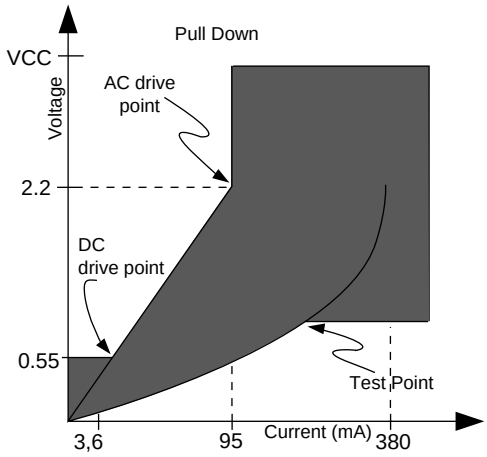
PCI Compliance

The ATF15xx Family also supports peripheral component interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers.

PCI Voltage-to-Current Curves for +5V Signaling in Pull-up Mode



PCI Voltage-to-Current Curves for +5V Signaling in Pull-down Mode



PCI DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7V		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5V		-70	µA
V_{OH}	Output High Voltage	I_{OUT} = -2 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance			12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

Note: Leakage current is without pin-keeper off.

PCI AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching	$0 < V_{OUT} \leq 1.4$	-44		mA
	Current High	$1.4 < V_{OUT} < 2.4$	$-44+(V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A	mA
	(Test High)	V_{OUT} = 3.1V		-142	µA
$I_{OL(AC)}$	Switching	$V_{OUT} > 2.2V$	95		mA
	Current Low	$2.2 > V_{OUT} > 0$	$V_{OUT}/0.023$		mA
		$0.1 > V_{OUT} > 0$		Equation B	mA
	(Test Point)	V_{OUT} = 0.71		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25+(V_{IN} + 1)/0.015$		mA
$SLEW_R$	Output Rise Slew Rate	0.4V to 2.4V load	0.5	3.0	V/ns
$SLEW_F$	Output Fall Slew Rate	2.4V to 0.4V load	0.5	3.0	V/ns

Notes: 1. Equation A: $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1V$.
2. Equation B: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-65°C to +135°C
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C$_{(MAX)}$
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V[1]
Programming Voltage with Respect to Ground	-2.0V to +14.0V[1]
DC Output Current per Pin	-25 to +25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. For currents less than 100 mA, minimum voltage is -0.6 VDC and maximum voltage is V_{CC} + 0.75 VDC. Pulses of less than 20µs may undershoot to -2.0V or overshoot to 7.0V.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient), T_A	0°C - 70°C	-40°C - 85°C
Junction Temperature, T_J[1]	–	–
V_{CCINT} (5.0V) Power Supply	5V ± 5%	5V ± 10%
V_{CCIO} (5.0V) Power Supply	5V ± 5%	5V ± 10%
V_{CCIO} (3.3V) Power Supply	3.0 - 3.6	3.0 - 3.6
V_I Input Voltage	-0.5 - V_{CCINT} + .5	-0.5 - V_{CCINT} + .5
V_O Output Voltage	0 - V_{CCIO}	0 - V_{CCIO}
t_R	40 ns Max	40 ns Max
t_F	40 ns Max	40 ns Max

Note: 1. Junction temperature is package and device dependant and can be calculated as follows: $T_{J(MAX)} = T_{A(MAX)} + (\theta_{JA}|_{Air\ Flow\ =\ 0} * P_{(MAX)})$. For more information see "Thermal Characteristics of Atmel Packages."

DC Characteristics[1] ATFxxSE Family

Symbol	Parameter	Condition			Min	Typ	Min	Unit
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	µA
I_{OZ}	Tri-State Output Off-State Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		[3]		mA
				Ind.		[3]		mA
			"ITD" Mode	Com.		1		mA
				Ind.		1		mA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max V_{IN} = 0, V_{CC}	PD Mode			0.1	1	mA
I_{CC3}[2]	Reduced-power Mode Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		[3]		mA
				Ind.		[3]		mA
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CCINT} +0.5	V
V_{OL}	5.0V Output Low Voltage (TTL)	I_{OL} = 12 mA, V_{CCIO} = 4.75V					0.45	V
	3.3V Output Low Voltage (TTL)	I_{OL} = 12 mA, V_{CCIO} = 3.0V					0.45	V
	3.3V Output Low Voltage (CMOS)	I_{OL} = 0.1 mA, V_{CCIO} = 3.0V					0.2	V
V_{OH}	5.0V Output High Voltage (TTL)	I_{OH} = -4 mA, V_{CCIO} = 4.75V			2.4			V
	3.3V Output High Voltage (TTL)	I_{OH} = -4 mA, V_{CCIO} = 3.0V			2.4			V
	3.3V Output High Voltage (CMOS)	I_{OH} = -0.1 mA, V_{CCIO} = 3.0V			V_{CCIO} – 0.2			V

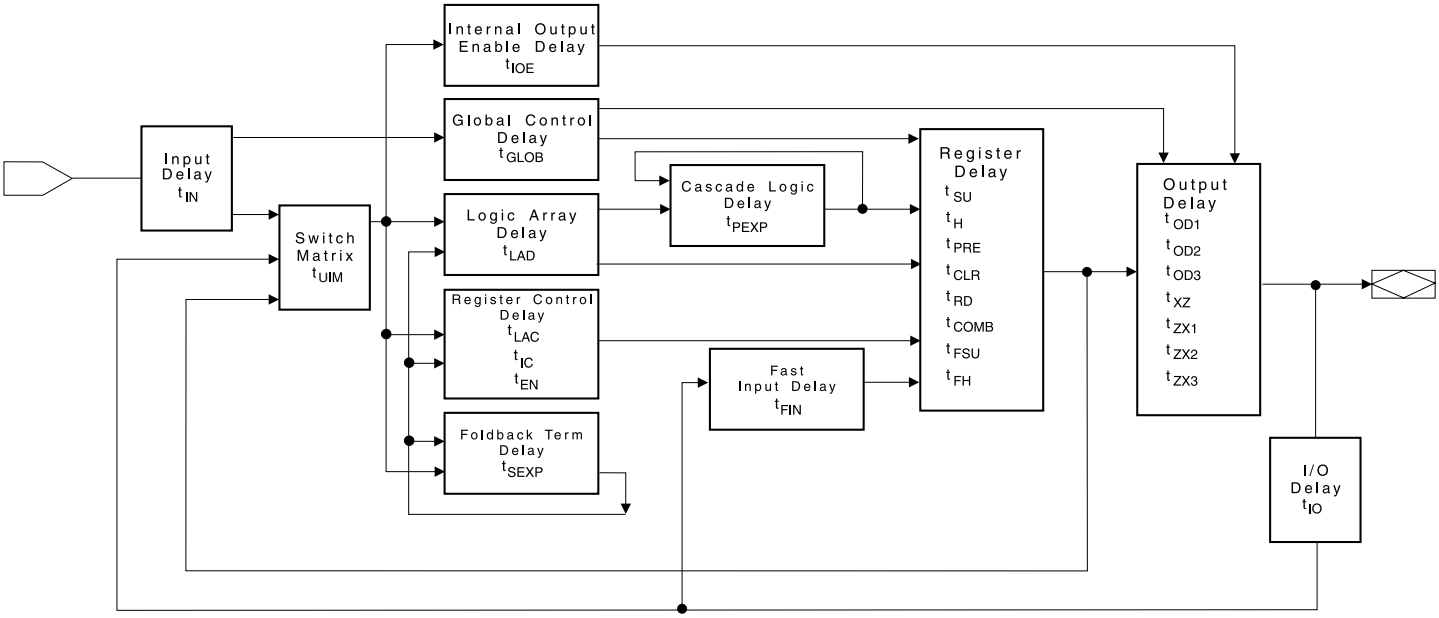
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.
3. See characteristic curves for each device.

Power-down AC Characteristics[1] ATFxxSE Family

		-5		-6		-7		-10		-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IVDH}	Valid 1, I/O before PD High	5.0		6.0		7.0		10		15		ns
t_{GVDH}	Valid 1, OE[2] before PD High	5.0		6.0		7.0		10		15		ns
t_{CVDH}	Valid 1, Clock[2] before PD High	5.0		6.0		7.0		10		15		ns
t_{DHIX}	I, I/O Don't Care after PD High		9.0		10.0		12		15.0		25	ns
t_{DHGX}	OE[2] Don't Care after PD High		9.0		10.0		12		15.0		25	ns
t_{DHCX}	Clock[2] Don't Care after PD High		9.0		10.0		12		15.0		25	ns
t_{DLIV}	PD Low to Valid I, I/O		1.0		1.0		1.0		1.0		1.0	µs
t_{DLGV}	PD Low to Valid OE, (Pin or Term)		1.0		1.0		1.0		1.0		1.0	µs
t_{DLCV}	PD Low to Valid Clock, (Pin or Term)		1.0		1.0		1.0		1.0		1.0	µs
t_{DLOV}	PD Low to Valid Output		1.0		1.0		1.0		1.0		1.0	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

Timing Model

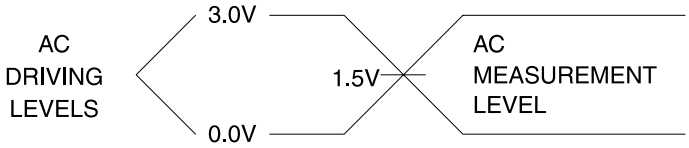


Pin Capacitance

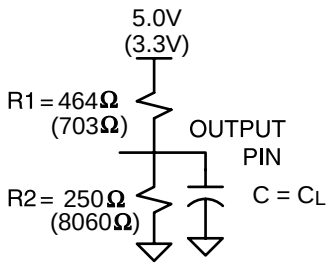
	Typ[1]	Max	Units	Condition
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Input Test Waveforms and Measurement Levels



Output AC Test Loads



AC Characteristics[1] ATF1502SE(L)

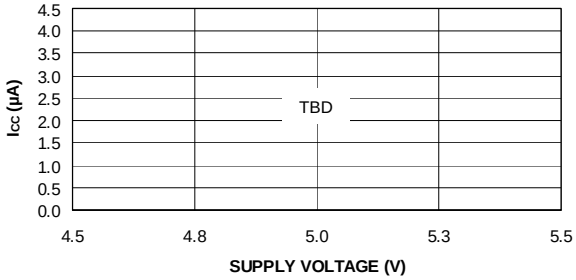
Symbol	Parameter	SE -5		SE -6		SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		5.0		6.0		7.5		10		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		5.0		6.0		7.5		10		12	ns
t_{SU}	Global Clock Setup Time	2.9		4.0		5.0		7.0		11		ns
t_{H}	Global Clock Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		2.5		2.5		3.0		3.0		ns
t_{FH}	Global Clock Hold of Fast Input	0.0		0.0		0.0		0.0		1.0		ns
t_{CO1}	Global Clock to Output Delay		3.2		3.5		4.3		5.0		8.0	ns
t_{CH}	Global Clock High Time	2.0		2.5		3.0		4.0		5.0		ns
t_{CL}	Global Clock Low Time	2.0		2.5		3.0		4.0		5.0		ns
t_{ASU}	Array Clock Setup Time	0.7		0.9		1.1		2.0		4.0		ns
t_{AH}	Array Clock Hold Time	1.8		2.1		2.7		3.0		4.0		ns
t_{ACO1}	Array Clock Output Delay		5.4		5.4		6.6		8.2		15	ns
t_{ACH}	Array Clock High Time	2.5		2.5		3.0		4.0		6.0		ns
t_{ACL}	Array Clock Low Time	2.5		2.5		3.0		4.0		6.0		ns
t_{CNT}	Minimum Clock Global Period		5.7		7.0		8.6		10.0		13	ns
f_{CNT}[3]	Maximum Internal Global Clock Frequency		175.4	143		117		100		77 or 100[6]		MHz
t_{ACNT}	Minimum Array Clock Period		5.7		7.0		8.6		10.0		13	ns
f_{ACNT}[4]	Maximum Internal Array Clock Frequency	175.4		143		117		100		77 or 100[6]		MHz
f_{MAX}[5]	Maximum Clock Frequency	250		200		167		125		80 or 125[6]		MHz
t_{IN}	Input Pad and Buffer Delay		0.2		0.2		0.3		0.5		1.0	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.2		0.2		0.3		0.5		1.0	ns
t_{FIN}	Fast Input Delay		2.2		2.1		2.5		1.0		1.5	ns
t_{SEXP}	Foldback Term Delay		3.1		3.8		4.6		5.0		8.0	ns
t_{PEXP}	Cascade Logic Delay		0.9		1.1		1.4		0.8		1.0	ns
t_{LAD}	Logic Array Delay		2.6		3.3		4.0		5.0		6.0	ns
t_{LAC}	Logic Control Delay		2.5		3.3		4.0		5.0		6.0	ns
t_{IOE}	Internal Output Enable Delay		0.7		0.8		1.0		2.0		3.0	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		0.2		0.3		0.4		1.5		2.5	ns

AC Characteristics[1] ATF1502SE(L) (Continued)

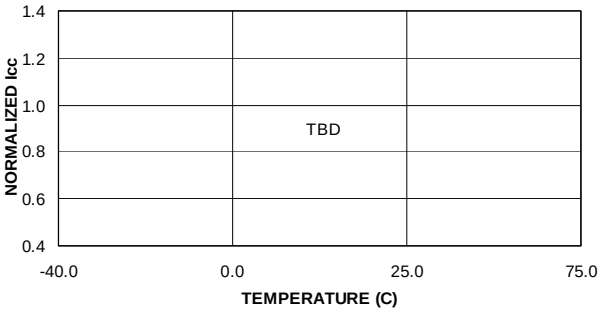
Symbol	Parameter	SE -5		SE -6		SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		0.7		0.8		0.9		2.0		3.0	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		5.2		5.3		5.4		5.5		6.0	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		4.0		4.0		4.0		5.0		7.0	ns
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		4.5		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		9.0		9.0		9.0		9.0		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5 pF)		4.0		4.0		4.0		5.0		6.0	ns
t_{SU}	Register Setup Time	0.8		1.0		1.3		2.0		4.0		ns
t_H	Register Hold Time	1.7		2.0		2.5		3.0		4.0		ns
t_{FSU}	Register Setup Time of Fast Input	1.9		1.7		1.7		3.0		5.0		ns
t_{FH}	Register Hold Time of Fast Input	0.6		0.7		0.8		0.5		2.0		ns
t_{RD}	Register Delay		1.2		1.6		1.2		2.0		2.0	ns
t_{COMB}	Combinatorial Delay		0.9		1.1		1.0		2.0		2.0	ns
t_{IC}	Array Clock Delay		2.7		3.4		2.0		5.0		7.0	ns
t_{EN}	Register Enable Time		2.6		3.3		1.0		5.0		7.0	ns
t_{GLOB}	Global Control Delay		1.6		1.4		1.3		1.0		1.0	ns
t_{PRE}	Register Preset Time		2.0		2.4		1.9		3.0		5.0	ns
t_{CLR}	Register Clear Time		2.0		2.4		3.0		3.0		5.0	ns
t_{UIM}	Switch Matrix Delay		1.1		1.1		1.4		1.0		2.0	ns
t_{RPA}[2]	Reduced Power Adder		8		9		10		11		13	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipelined data.
6. For clocked applications and frequencies above $f_{CRITICAL}$, OR, non-clocked applications with dormant times less than $1/f_{CRITICAL}$, the device will achieve the speeds of the –10 column. See “Input Transition Detection/ Automatic Power Down” on page 8.

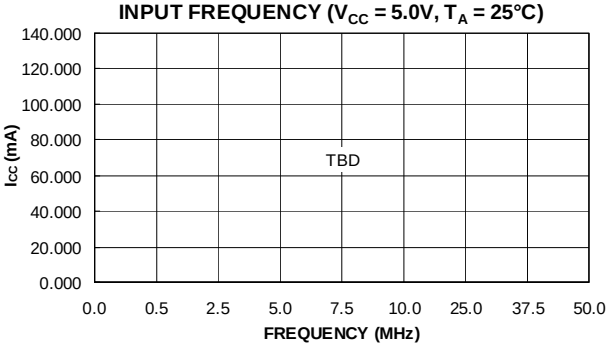
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



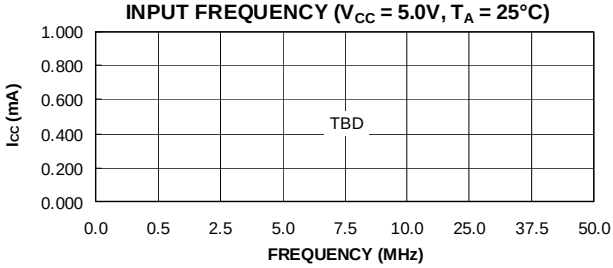
NORMALIZED I_{CC} VS. TEMP



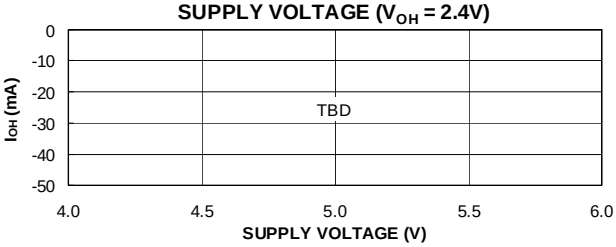
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



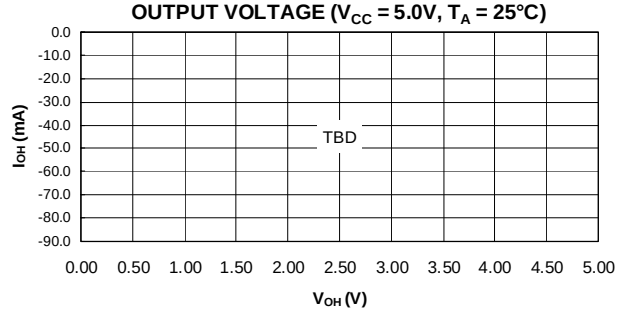
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



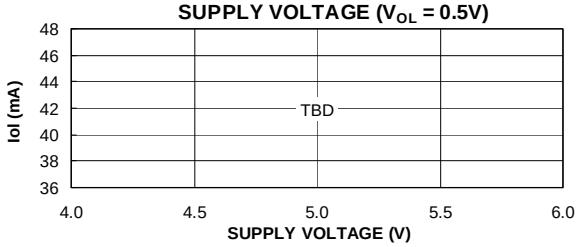
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



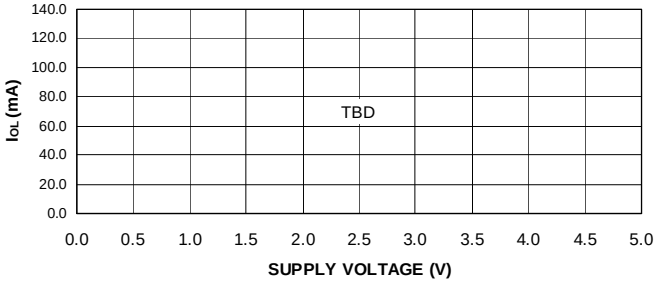
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



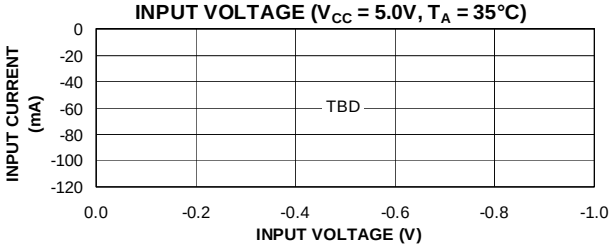
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



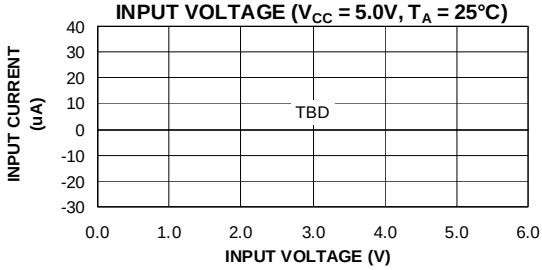
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



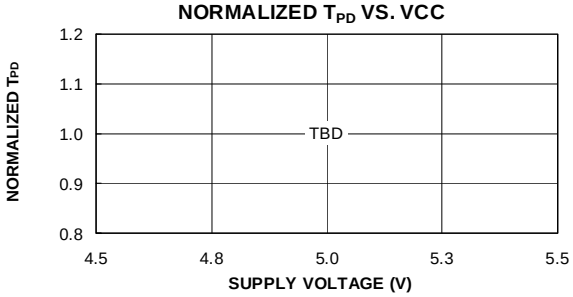
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



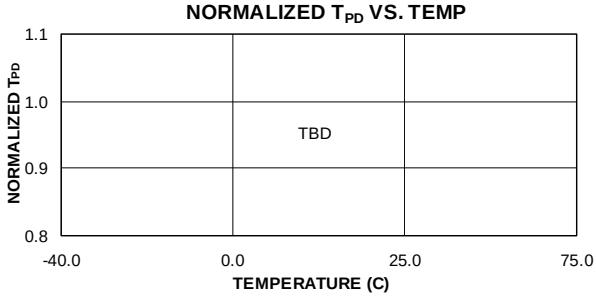
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



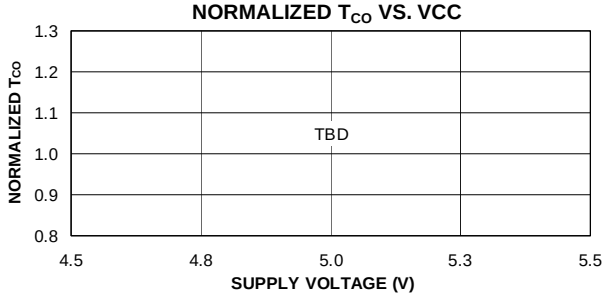
NORMALIZED T_{PD} VS. VCC



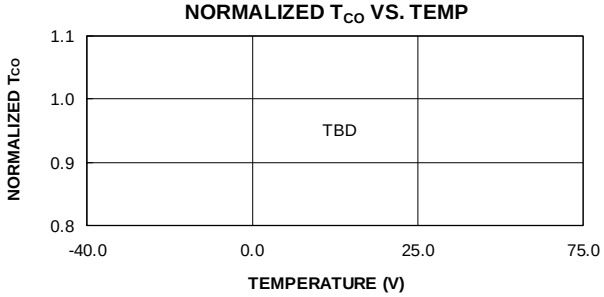
NORMALIZED T_{PD} VS. TEMP



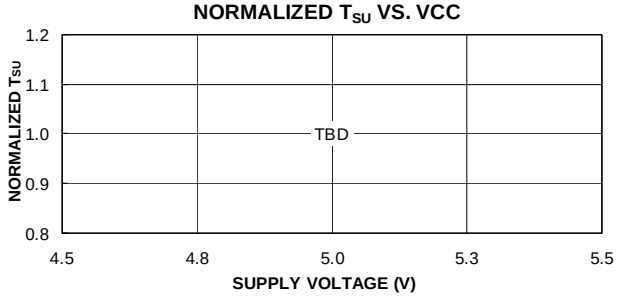
NORMALIZED T_{CO} VS. VCC



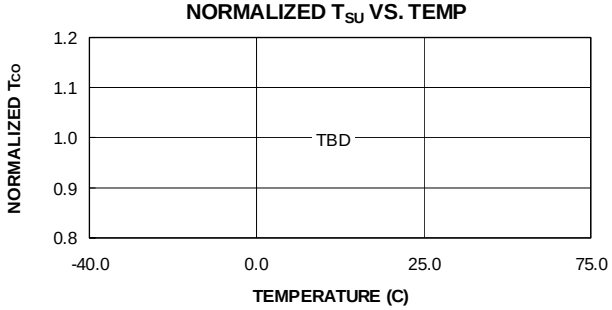
NORMALIZED T_{CO} VS. TEMP



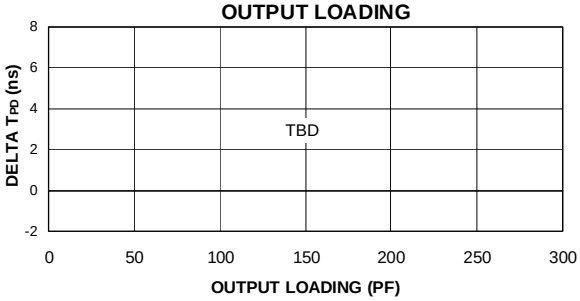
NORMALIZED T_{SU} VS. VCC



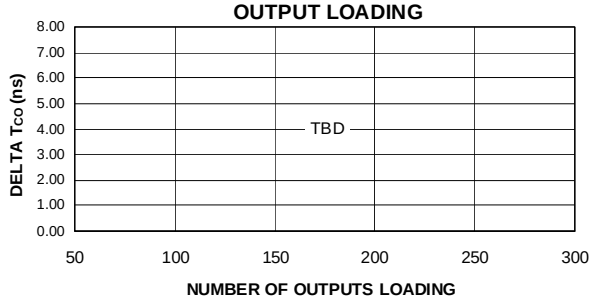
NORMALIZED T_{SU} VS. TEMP



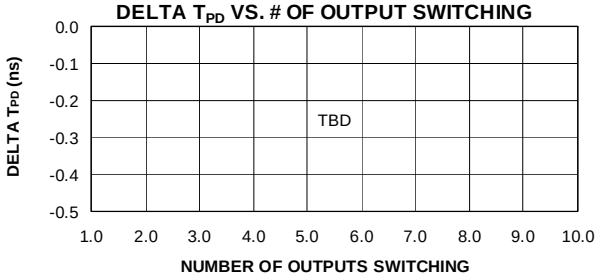
DELTA T_{PD} VS. OUTPUT LOADING



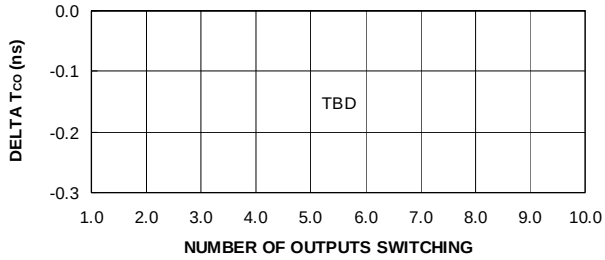
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING

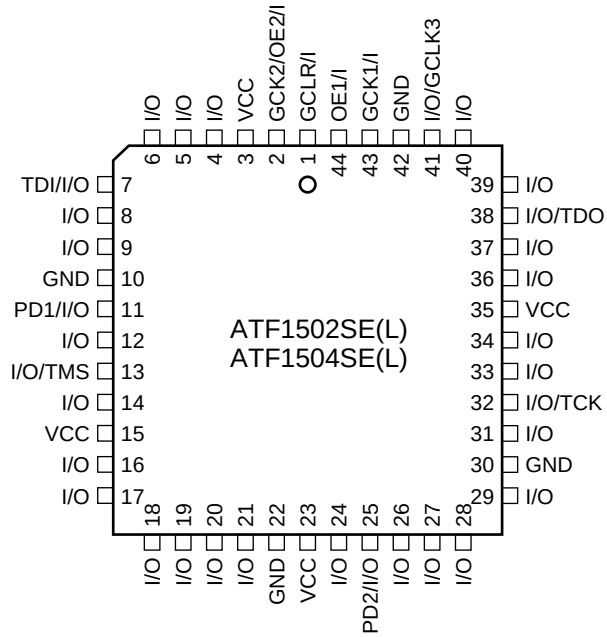


DELTA T_{CO} VS. # OF OUTPUT SWITCHING

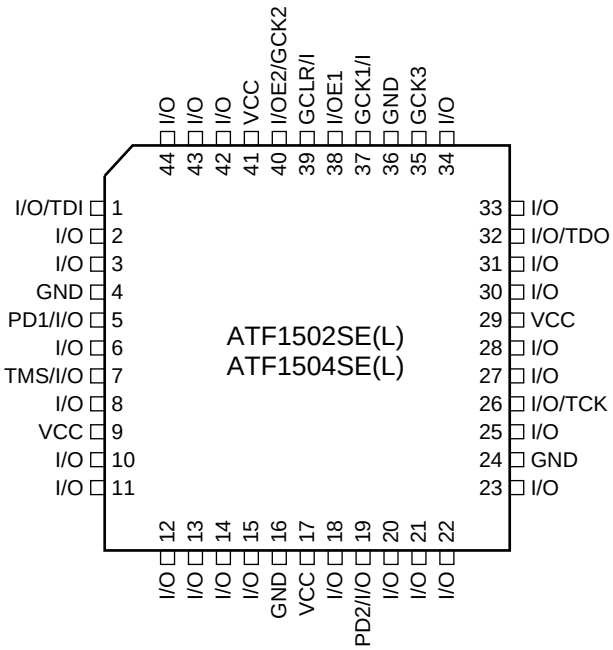


ATF1502SE(L) Pinouts

44-lead TQFP - Top View



44-lead PLCC - Top View



ATF1502SE(L) Dedicated Pinouts

Dedicated Pin	44-PLCC J-lead	44-lead TQFP
INPUT/GCLK1	43	37
INPUT/GCLR	1	39
INPUT/OE1	44	38
INPUT/OE2/GCLK2	2	40
I/O/GCLK3	41	35
I/O/PD (1,2)	11, 25	5, 19
I/O/TDI (JTAG)	7	1
I/O/TMS (JTAG)	13	7
I/O/TCK (JTAG)	32	26
I/O/TDO (JTAG)	38	32
GNDINT	22, 42	16, 36
GNDIO	10, 30	4, 24
VCCINT	3, 23	17, 41
VCCIO	15, 35	9, 29
# of Signal Pins	36	36
# User I/O Pins	32	32

OE (1, 2) Global OE pins
GCLR Global Clear pin
GCLK (1, 2, 3) Global Clock pins
PD (1, 2) Power-down pins
TDI, TMS, TCK, TDO JTAG pins used for boundary-scan testing or in-system programming
GNDINT Ground pins for the internal device logic
GNDIO Ground pins for the I/O drivers
VCCINT VCC pins for the internal device logic (+3.3V)
VCCIO VCC for the I/O drivers

ATF1502SE(L) I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP
1	A	4	42
2	A	5	43
3	A	6	44
4/**TDI**	A	7	1
5	A	8	2
6	A	9	3
7/**PD1**	A	11	5
8	A	12	6
9/**TMS**	A	13	7
10	A	14	8
11	A	16	10
12	A	17	11
13	A	18	12
14	A	19	13
15	A	20	14
16	A	21	15
17	B	41	35
18	B	40	34
19	B	39	33
20/**TDO**	B	38	32
21	B	37	31
22	B	36	30
23	B	34	28
24	B	33	27
25/**TCK**	B	32	26
26	B	31	25
27	B	29	23
28	B	28	22
29	B	27	21
30	B	26	20
31/**PD2**	B	25	19
32	B	24	18

ATF1502SE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	F_{MAX} (MHz)	Ordering Code	Package	Operation Range
5.0	3.2	250	ATF1502SE-5 AC44 ATF1502SE-5 JC44	44A 44J	Commercial (0°C to 70°C)
6.0	3.5	200	ATF1502SE-6 AC44 ATF1502SE-6 JC44	44A 44J	Commercial (0°C to 70°C)
7.5	4.3	167	ATF1502SE-7 AC44 ATF1502SE-7 JC44	44A 44J	Commercial (0°C to 70°C)
			ATF1502SE-7 AI44 ATF1502SE-7 JI44	44A 44J	Industrial (-40°C to +85°C)
10	5.0	125	ATF1502SE-10 AC44 ATF1502SE-10 JC44	44A 44J	Commercial (0°C to 70°C)
			ATF1502SE-10 AI44 ATF1502SE-10 JI44	44A 44J	Industrial (-40°C to +85°C)
15	8.0	77	ATF1502SEL-15 AC44 ATF1502SEL-15 JC44	44A 44J	Commercial (0°C to 70°C)

Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, downgrade one speed grade from the “I” to the “C” device, and de-rate power by 30%.

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)

AC Characteristics[1] ATF1504SE(L)

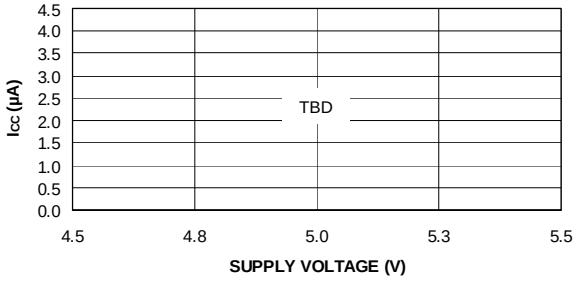
Symbol	Parameter	SE -5		SE -6		SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		5.0		6.0		7.5		10		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		5.0		6.0		7.5		10		12	ns
t_{SU}	Global Clock Setup Time	2.9		3.6		6.0		7.0		11		ns
t_{H}	Global Clock Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		2.5		3.0		3.0		3.0		ns
t_{FH}	Global Clock Hold of Fast Input	0.0		0.0		0.5		0.5		1.0		ns
t_{CO1}	Global Clock to Output Delay		3.2		4.0		4.5		5.0		9.0	ns
t_{CH}	Global Clock High Time	2.0		2.5		3.0		4.0		5.0		ns
t_{CL}	Global Clock Low Time	2.0		2.5		3.0		4.0		5.0		ns
t_{ASU}	Array Clock Setup Time	0.7		0.9		2.0		2.0		5.0		ns
t_{AH}	Array Clock Hold Time	1.8		2.9		2.0		3.0		4.0		ns
t_{ACO1}	Array Clock Output Delay		5.4		6.7		7.5		10.0		15	ns
t_{ACH}	Array Clock High Time	2.5		2.5		3.0		4.0		6.0		ns
t_{ACL}	Array Clock Low Time	2.5		2.5		3.0		4.0		6.0		ns
t_{CNT}	Minimum Clock Global Period		5.7		7.1		8.0		10		13	ns
f_{CNT}[3]	Maximum Internal Global Clock Frequency	176		141		125		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		5.7		7.1		8.0		10		13	ns
f_{ACNT}[4]	Maximum Internal Array Clock Frequency	176		141		125		100		77		MHz
f_{MAX}[5]	Maximum Clock Frequency	250		200		167		125		77		MHz
t_{IN}	Input Pad and Buffer Delay		0.2		0.2		0.5		0.5		1.0	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.2		0.2		0.5		0.5		1.0	ns
t_{FIN}	Fast Input Delay		2.2		2.6		1.0		1.0		2.0	ns
t_{SEXP}	Foldback Term Delay		3.1		3.8		4.0		5.0		8.0	ns
t_{PEXP}	Cascade Logic Delay		0.9		1.1		0.8		0.8		1.0	ns
t_{LAD}	Logic Array Delay		2.6		3.2		3.0		5.0		6.0	ns
t_{LAC}	Logic Control Delay		2.5		3.2		3.0		5.0		6.0	ns
t_{IOE}	Internal Output Enable Delay		0.7		0.8		2.0		2.0		3.0	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		0.2		0.3		2.0		1.5		2.5	ns

AC Characteristics[1] ATF1504SE(L) (Continued)

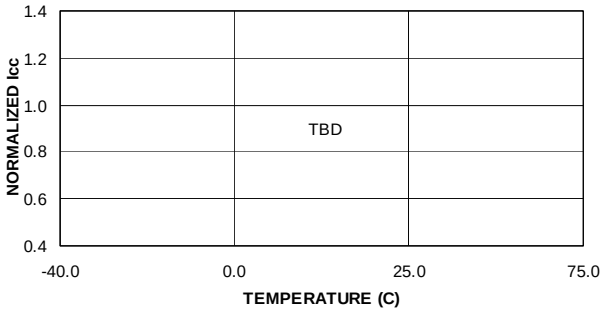
Symbol	Parameter	SE -5		SE -6		SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		0.7		0.8		2.5		2.0		3.0	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		5.2		5.3		7.0		5.5		6.0	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		4.0		4.0		4.0		5.0		7.0	ns
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		4.5		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		9.0		9.0		9.0		9.0		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5 pF)		4.0		4.0		4.0		5.0		6.0	ns
t_{SU}	Register Setup Time	0.8		1.0		3.0		2.0		5.0		ns
t_H	Register Hold Time	1.7		2.0		2.0		3.0		4.0		ns
t_{FSU}	Register Setup Time of Fast Input	1.9		1.8		3.0		3.0		5.0		ns
t_{FH}	Register Hold Time of Fast Input	0.6		0.7		0.5		0.5		2.0		ns
t_{RD}	Register Delay		1.2		1.6		1.0		2.0		2.0	ns
t_{COMB}	Combinatorial Delay		0.9		1.0		1.0		2.0		2.0	ns
t_{IC}	Array Clock Delay		2.7		3.3		3.0		5.0		6.0	ns
t_{EN}	Register Enable Time		2.6		3.2		3.0		5.0		6.0	ns
t_{GLOB}	Global Control Delay		1.6		1.9		1.0		1.0		2.0	ns
t_{PRE}	Register Preset Time		2.0		2.4		2.0		3.0		4.0	ns
t_{CLR}	Register Clear Time		2.0		2.4		2.0		3.0		4.0	ns
t_{UIM}	Switch Matrix Delay		1.1		1.3		1.0		1.0		2.0	ns
t_{RPA}[2]	Reduced Power Adder		8.0		9.0		1.0		11		13	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipelined data.
6. For clocked applications and frequencies above $f_{CRITICAL}$, OR, non-clocked applications with dormant times less than $1/f_{CRITICAL}$, the device will achieve the speeds of the –10 column. See “Input Transition Detection/ Automatic Power Down” on page 8.

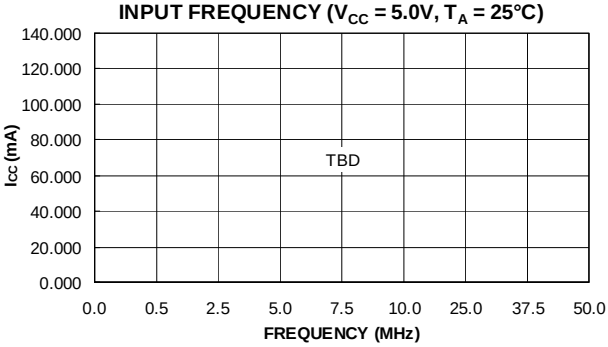
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



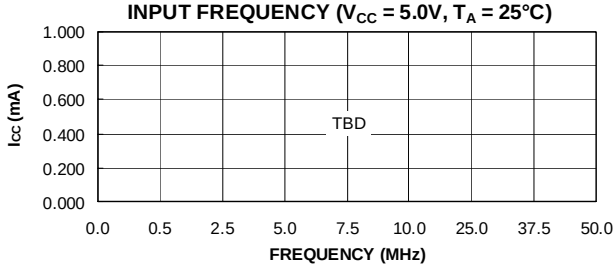
NORMALIZED I_{CC} VS. TEMP



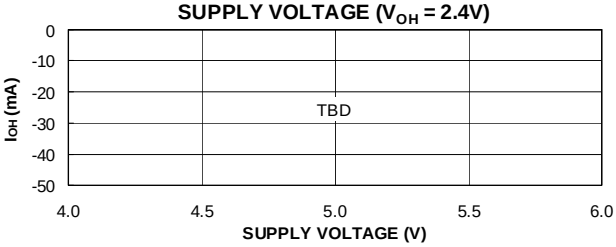
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



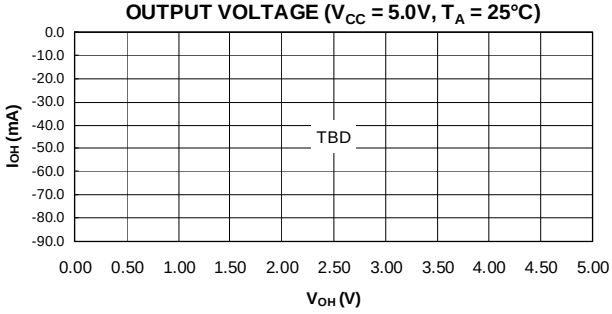
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



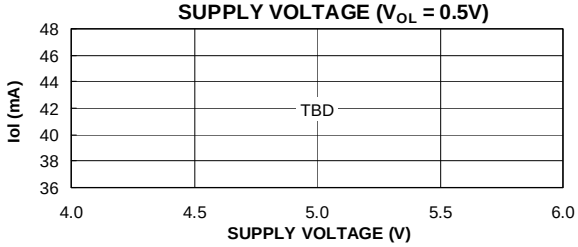
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



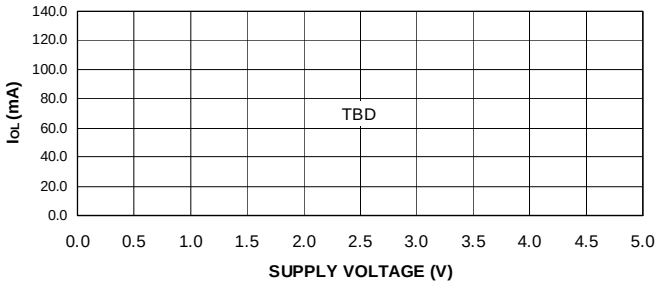
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



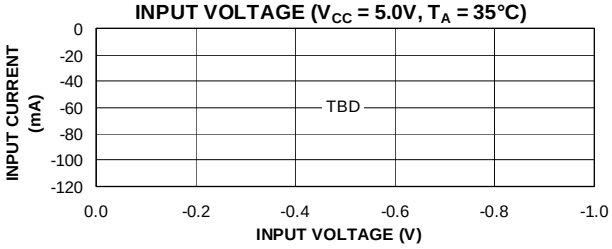
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



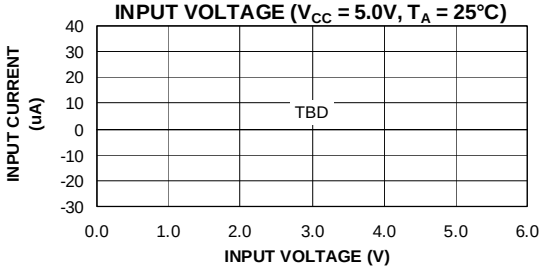
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



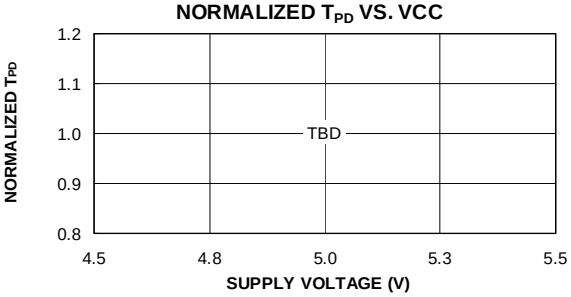
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



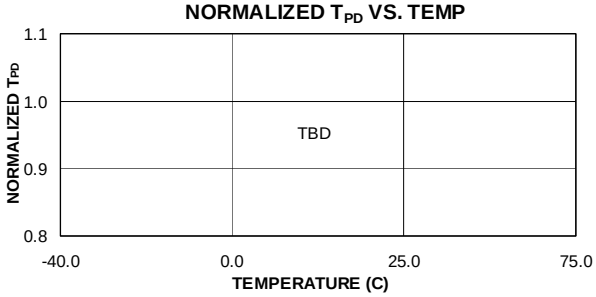
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



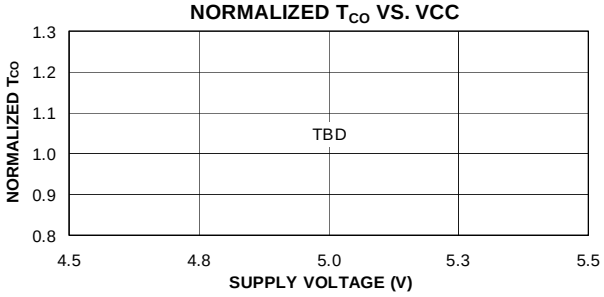
NORMALIZED T_{PD} VS. VCC



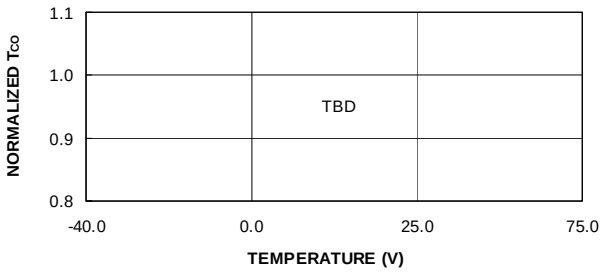
NORMALIZED T_{PD} VS. TEMP



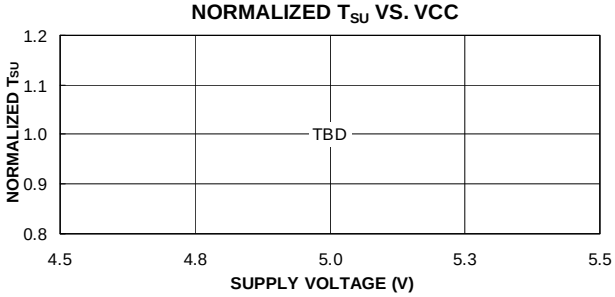
NORMALIZED T_{CO} VS. VCC



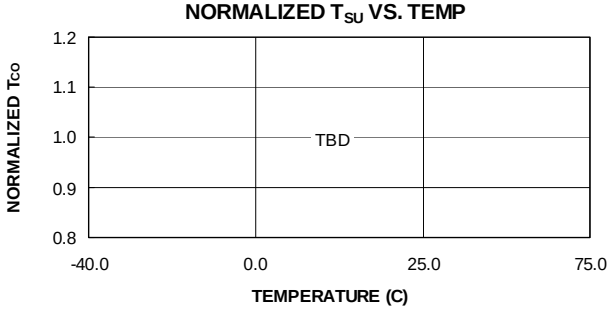
NORMALIZED T_{CO} VS. TEMP

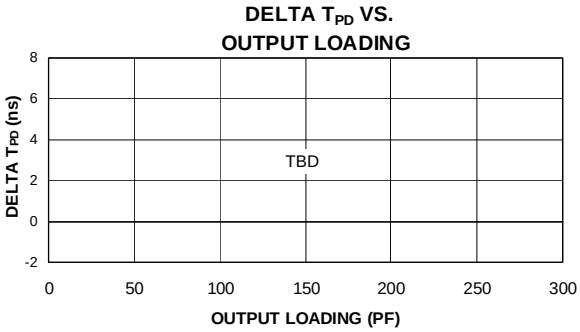


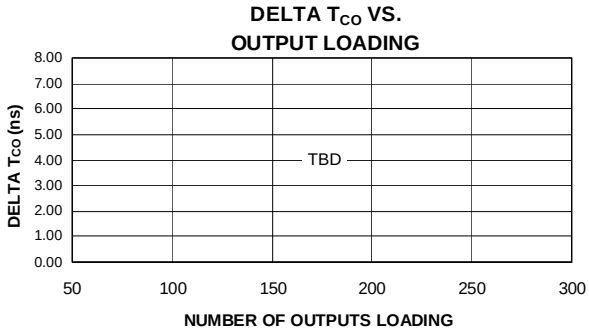
NORMALIZED T_{SU} VS. VCC

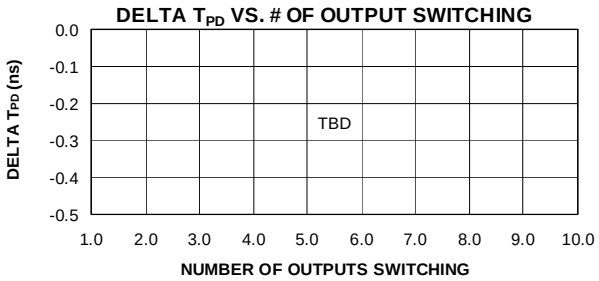


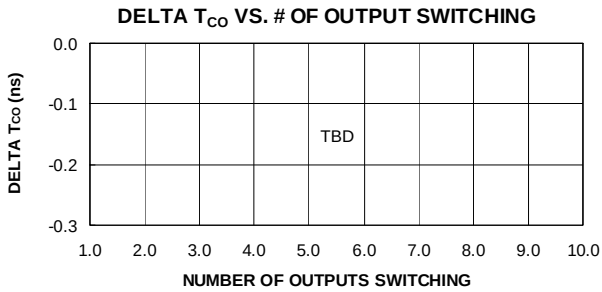
NORMALIZED T_{SU} VS. TEMP




DELTA T_{PD} VS.
OUTPUT LOADING
DELTA T_{PD} (ns)
8
6
4
2
0
-2
TBD
0
50
100
150
200
250
300
OUTPUT LOADING (PF)

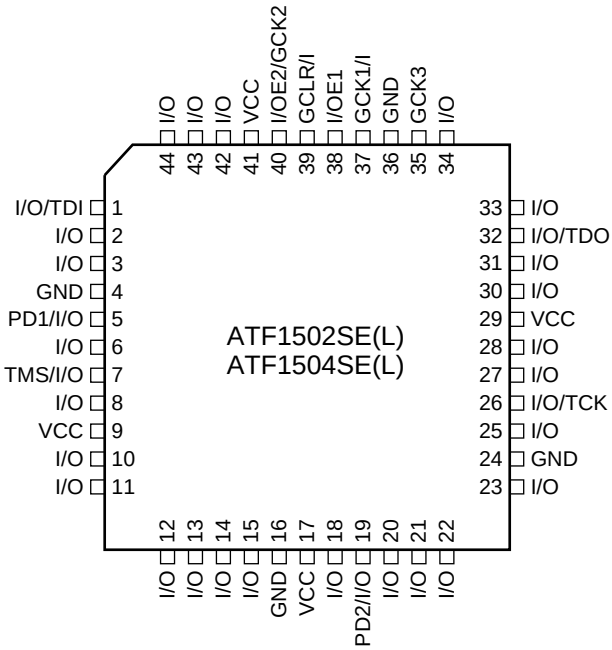

DELTA T_{CO} VS.
OUTPUT LOADING
DELTA T_{CO} (ns)
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
TBD
50
100
150
200
250
300
NUMBER OF OUTPUTS LOADING


DELTA T_{PD} VS. # OF OUTPUT SWITCHING
DELTA T_{PD} (ns)
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

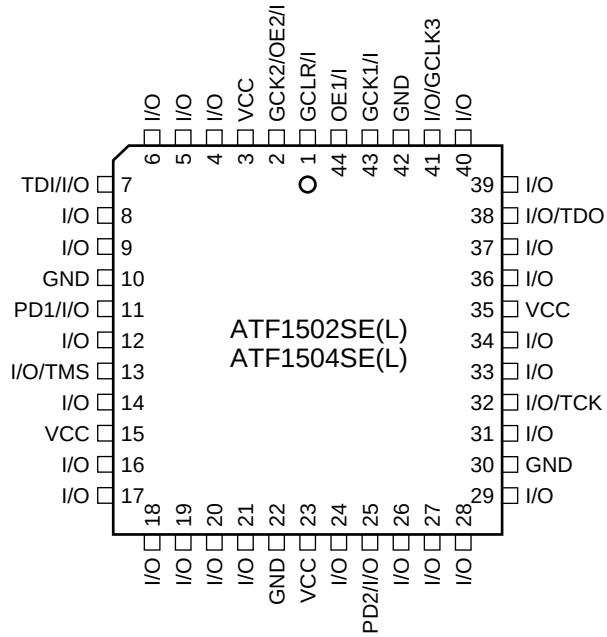

DELTA T_{CO} VS. # OF OUTPUT SWITCHING
DELTA T_{CO} (ns)
0.0
-0.1
-0.2
-0.3
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

ATF1504SE(L) Pinouts

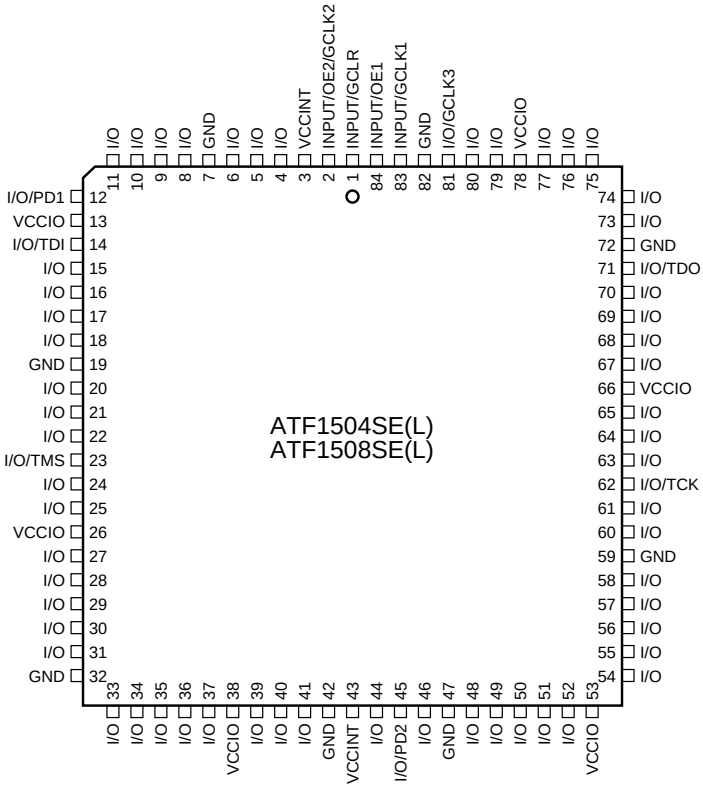
44-lead TQFP – Top View



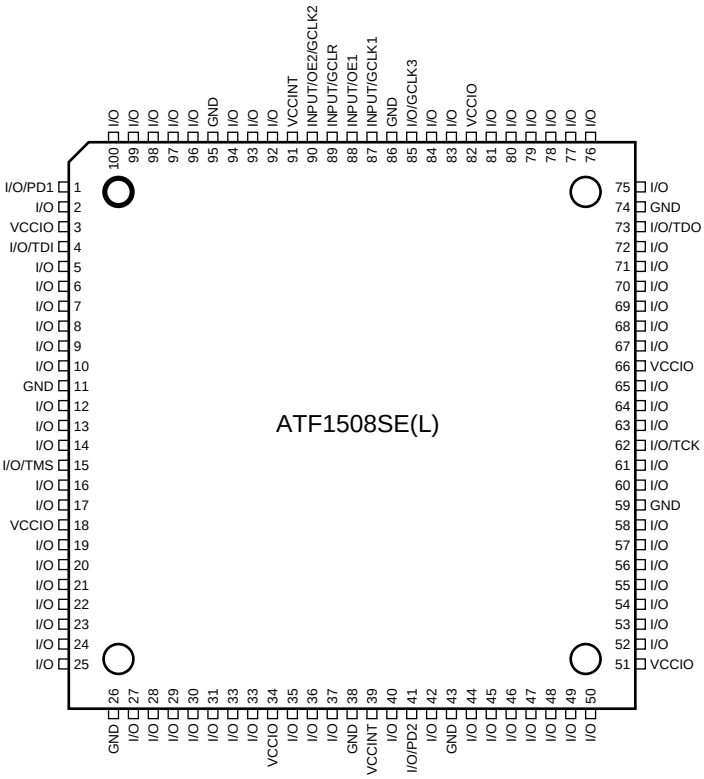
44-lead PLCC – Top View



84-lead PLCC – Top View



100-lead TQFP – Top View



ATF1504SE(L) Dedicated Pinouts

Dedicated Pin	44-lead TQFP	44-lead PLCC	84-lead PLCC	100-lead TQFP
INPUT/GCLK1	37	43	83	87
INPUT/GCLR	39	1	1	89
INPUT/OE1	38	44	84	88
INPUT/OE2/GCLK2	40	2	2	90
I/O /GCLK3	35	41	81	85
I/O/PD (1,2)	5, 19	11, 25	20, 46	12, 42
I/O/TDI (JTAG)	1	7	14	4
I/O/TMS (JTAG)	7	13	23	15
I/O/TCK (JTAG)	26	32	62	62
I/O/TDO (JTAG)	32	38	71	73
GNDINT	16, 36	22, 44	42, 82	38, 86
GNDIO	4, 24	10, 30	7, 18, 32,47, 69, 72	11, 26, 43, 59, 74, 95
VCCINT	17, 41	3, 23	3, 43	39, 91
VCCIO	9, 29	15, 35	13, 26, 33, 53, 66, 78	3, 18, 34, 51, 66, 82
N/C	-	-	-	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	68	68
# User I/O Pins	32	32	64	64

OE (1, 2) Global OE pins
GCLR Global Clear pin
GCLK (1, 2, 3) Global Clock pins
PD (1, 2) Power-down pins
TDI, TMS, TCK, TDO JTAG pins used for boundary-scan testing or in-system programming
GNDINT Ground pins for the internal device logic
GNDIO Ground pins for the I/O pins
VCCINT VCC pins for the internal device logic
VCCIO VCC for the I/O drivers

ATF1504SE(L) I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP	84-lead PLCC	100-lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	84-lead PLCC	100-lead TQFP
1	A	12	6	22	14	33	C	24	18	44	40
2	A	-	-	21	13	34	C	-	-	45	41
3	A/ **PD1**	11	5	20	12	35	C/ **PD2**	25	19	46	42
4	A	9	3	18	10	36	C	26	20	48	44
5	A	8	2	17	9	37	C	27	21	49	45
6	A	-	-	16	8	38	C	-	-	50	46
7	A	-	-	15	6	39	C	-	-	51	47
8/ **TDI**	A	7	1	14	4	40	C	28	22	52	48
9	A	-	-	12	100	41	C	29	23	54	52
10	A	-	-	11	99	42	C	-	-	55	54
11	A	6	44	10	98	43	C	-	-	56	56
12	A	-	-	9	97	44	C	-	-	57	57
13	A	-	-	8	96	45	C	-	-	58	58
14	A	5	43	6	94	46	C	31	25	60	60
15	A	-	-	5	93	47	C	-	-	61	61
16	A	4	42	4	92	48/ **TCK**	C	32	26	62	62
17	B	21	15	41	37	49	D	33	27	63	63
18	B	-	-	40	36	50	D	-	-	64	64
19	B	20	14	39	35	51	D	34	28	65	65
20	B	19	13	37	33	52	D	36	30	67	67
21	B	18	12	36	32	53	D	37	31	68	68
22	B	-	-	35	31	54	D	-	-	69	69
23	B	-	-	34	30	55	D	-	-	70	71
24	B	17	11	33	29	56/ **TDO**	D	38	32	71	73
25	B	16	10	31	25	57	D	39	33	73	75
26	B	-	-	30	23	58	D	-	-	74	76
27	B	-	-	29	21	59	D	-	-	75	79
28	B	-	-	28	20	60	D	-	-	76	80
29	B	-	-	27	19	61	D	-	-	77	81
30	B	14	8	25	17	62	D	40	34	79	83
31	B	-	-	24	16	63	D	-	-	80	84
32/ **TMS**	B	13	7	23	15	64	D/ **GCLK3**	41	35	81	85

ATF1504SE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
5.0	3.2	250	ATF1504SE-5 AC44 ATF1504SE-5 JC44 ATF1504SE-5 JC84 ATF1504SE-5 AC100	44A 44J 84J 100A	Commercial (0°C to 70°C)
6.0	4.0	200	ATF1504SE-6 AC44 ATF1504SE-6 JC44 ATF1504SE-6 JC84 ATF1504SE-6 AC100	44A 44J 84J 100A	Commercial (0°C to 70°C)
7.5	4.5	167	ATF1504SE-7 AC44 ATF1504SE-7 JC44 ATF1504SE-7 JC84 ATF1504SE-7 AC100	44A 44J 84J 100A	Commercial (0°C to 70°C)
			ATF1504SE-7 AI44 ATF1504SE-7 JI44 ATF1504SE-7 J84 ATF1504SE-7 AI100	44A 44J 84J 100A	Industrial (-40°C to +85°C)
10	5.0	125	ATF1504SE-10 AC44 ATF1504SE-10 JC44 ATF1504SE-10 JC84 ATF1504SE-10 AC100	44A 44J 84J 100A	Commercial (0°C to 70°C)
			ATF1504SE-10 AI44 ATF1504SE-10 JI44 ATF1504SE-10 JI84 ATF1504SE-10 AI100	44A 44J 84J 100A	Industrial (-40°C to +85°C)
15	9.0	77	ATF1504SEL-15 AC44 ATF1504SEL-15 JC44 ATF1504SEL-15 JC84 ATF1504SEL-15 AC100	44A 44J 84J 100A	Commercial (0°C to 70°C)

Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, down grade one speed grade from the “I” to the “C” device, and de-rate power by 30%.

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flatpack (TQFP)

AC Characteristics[1] ATF1508SE(L)

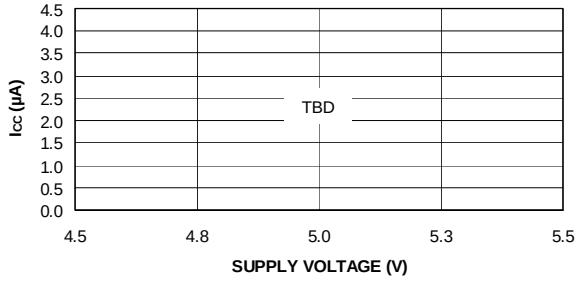
Symbol	Parameter	SE -6		SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		6		7.5		10	15		ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		6		7.5		10	15		ns
t_{SU}	Global Clock Setup Time	3.4		6.0		7.0		11		ns
t_{H}	Global Clock Hold Time	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		3.0		3.0		3.0		ns
t_{FH}	Global Clock Hold of Fast Input	0		0.5		0.5		1		ns
t_{CO1}	Global Clock to Output Delay		4.0		4.5		5.0		8.0	ns
t_{CH}	Global Clock High Time	3		3.0		4.0		5.0		ns
t_{CL}	Global Clock Low Time	3		3.0		4.0		5.0		ns
t_{ASU}	Array Clock Setup Time	0.9		3.0		2.0		4.0		ns
t_{AH}	Array Clock Hold Time	1.8		2.0		5.0		4.0		ns
t_{ACO1}	Array Clock Output Delay		6.5		7.5		10		15	ns
t_{ACH}	Array Clock High Time	3.0		3		4.0		6.0		ns
t_{ACL}	Array Clock Low Time	3.0		3		4.0		6.0		ns
t_{CNT}	Minimum Clock Global Period		6.8		8.0		10		13	ns
f_{CNT}[3]	Maximum Internal Global Clock Frequency	150		125		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		6.8		8.0		10		13	ns
f_{ACNT}[4]	Maximum Internal Array Clock Frequency	150		125		100		77		MHz
f_{MAX}[5]	Maximum Clock Frequency	167		167		125		100		MHz
t_{IN}	Input Pad and Buffer Delay		0.2		0.5		0.5		2.0	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.2		0.5		0.5		2.0	ns
t_{FIN}	Fast Input Delay		2.6		1.0		1.0		2.0	ns
t_{SEXP}	Foldback Term Delay		3.7		4.0		5.0		8.0	ns
t_{PEXP}	Cascade Logic Delay		1.1		0.8		0.0		1.0	ns
t_{LAD}	Logic Array Delay		3.0		3.0		5.0		6.0	ns
t_{LAC}	Logic Control Delay		3.0		3.0		5.0		6.0	ns
t_{IOE}	Internal Output Enable Delay		0.7		2.0		2.0		3.0	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		0.4		2.0		1.5		4.0	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		0.9		2.5		2.0		5.0	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		5.4		7.0		5.5		8.0	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		4.0		4.0		5		6.0	ns

AC Characteristics[1] ATF1508SE(L) (Continued)

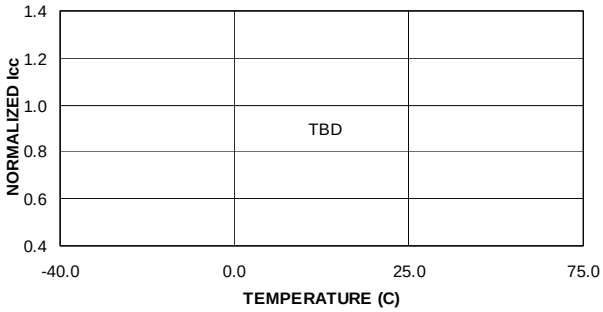
Symbol	Parameter	SE -6		SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		9		9		9		10.0	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5 pF)		4		4		5		6.0	ns
t_{SU}	Register Setup Time	1.0		3.0		2.0		4.0		ns
t_H	Register Hold Time	1.7		2.0		5.0		4.0		ns
t_{FSU}	Register Setup Time of Fast Input	1.9		3.0		3.0		2.0		ns
t_{FH}	Register Hold Time of Fast Input	0.6		0.5		0.5		1.0		ns
t_{RD}	Register Delay		1.4		1.0		2.0		1.0	ns
t_{COMB}	Combinatorial Delay		1.0		1.0		2.0		1.0	ns
t_{IC}	Array Clock Delay		3.1		3.0		5.0		6.0	ns
t_{EN}	Register Enable Time		3.0		3.0		5.0		6.0	ns
t_{GLOB}	Global Control Delay		2.0		1.0		1.0		1.0	ns
t_{PRE}	Register Preset Time		2.4		2.0		3.0		4.0	ns
t_{CLR}	Register Clear Time		2.4		2.0		3.0		4.0	ns
t_{UIM}	Switch Matrix Delay		1.4		1.0		1.0		2.0	ns
t_{RPA}[2]	Reduced Power Adder		10		10		11		13	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipelined data.
6. For clocked applications and frequencies above $f_{CRITICAL}$, OR, non-clocked applications with dormant times less than $1/f_{CRITICAL}$, the device will achieve the speeds of the –10 column. See “Input Transition Detection/ Automatic Power Down” on page 8.

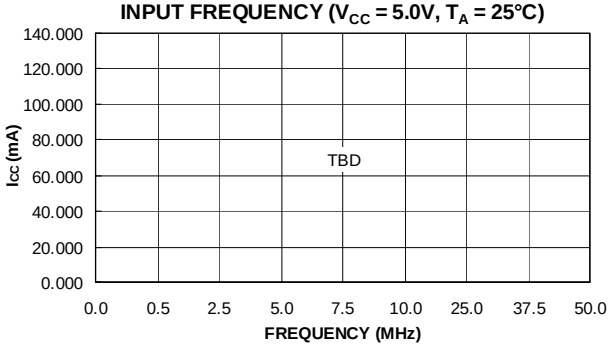
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



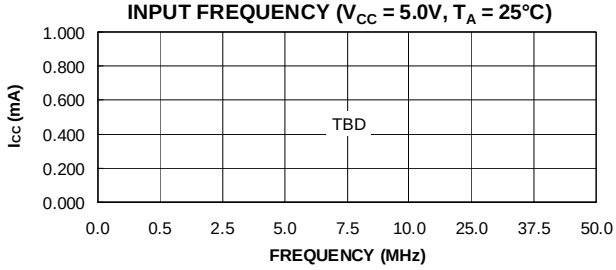
NORMALIZED I_{CC} VS. TEMP



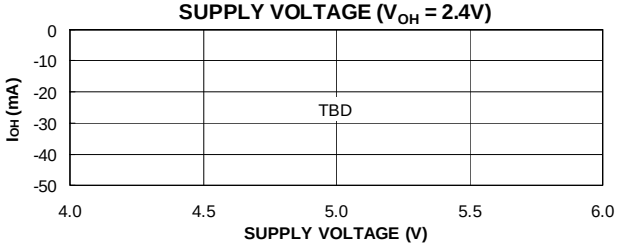
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



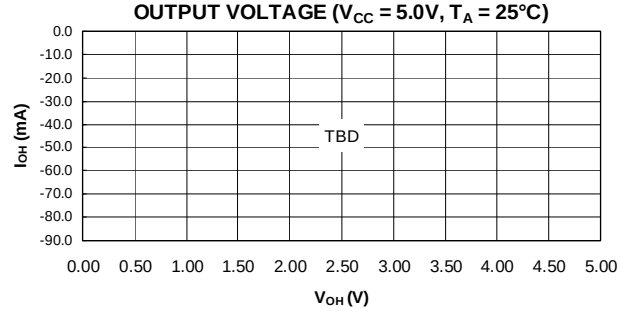
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



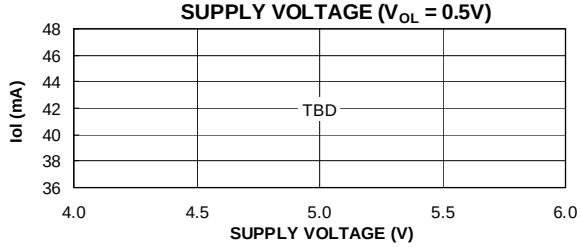
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



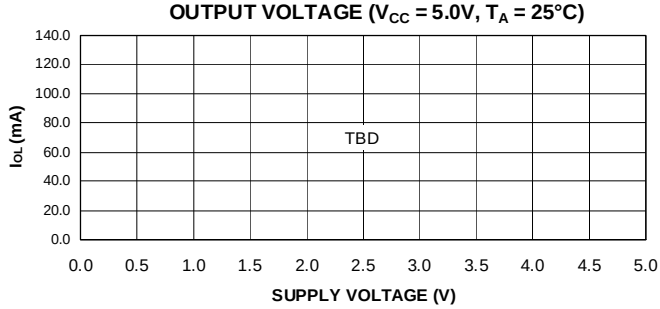
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



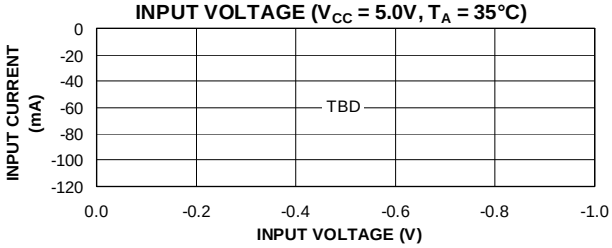
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



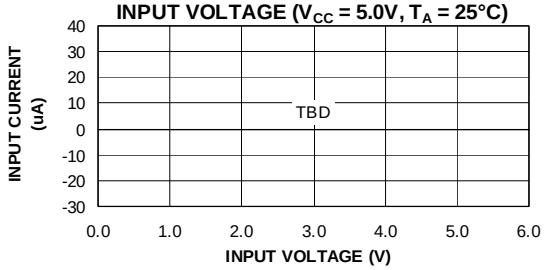
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



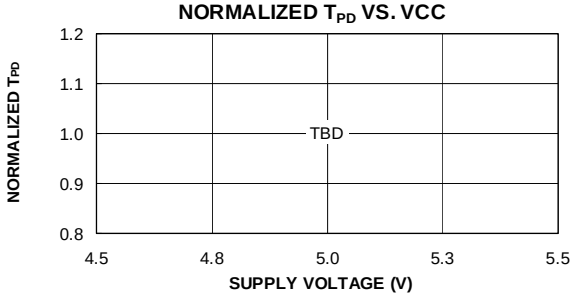
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



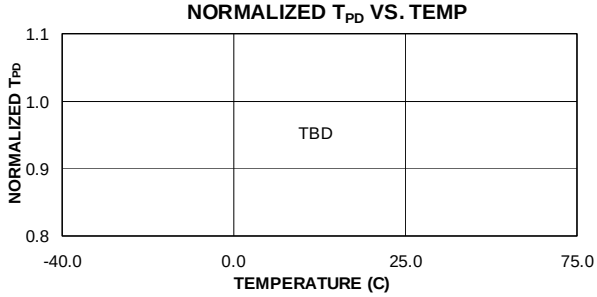
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



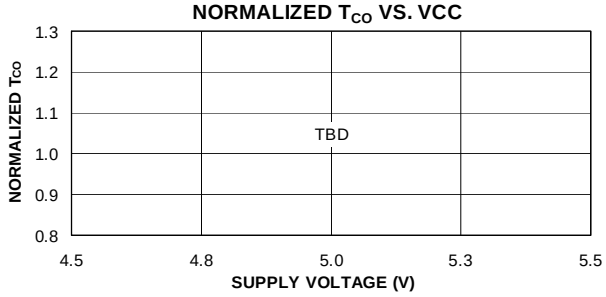
NORMALIZED T_{PD} VS. VCC



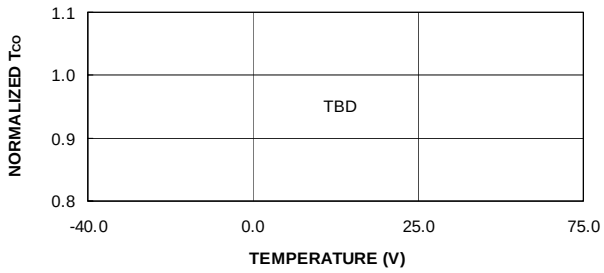
NORMALIZED T_{PD} VS. TEMP



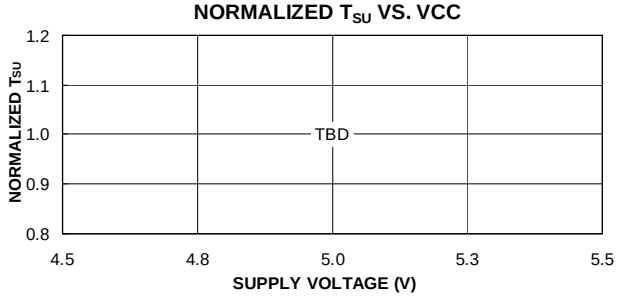
NORMALIZED T_{CO} VS. VCC



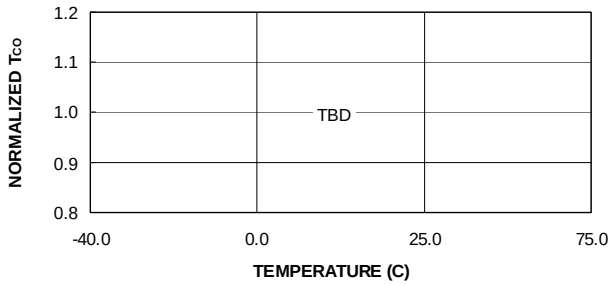
NORMALIZED T_{CO} VS. TEMP



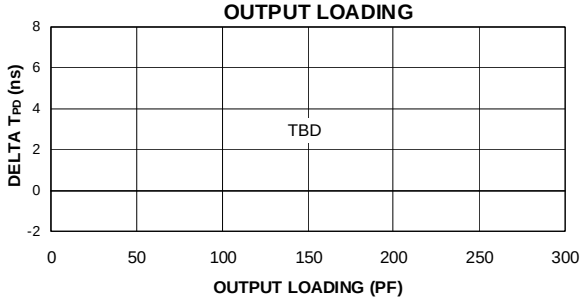
NORMALIZED T_{SU} VS. VCC



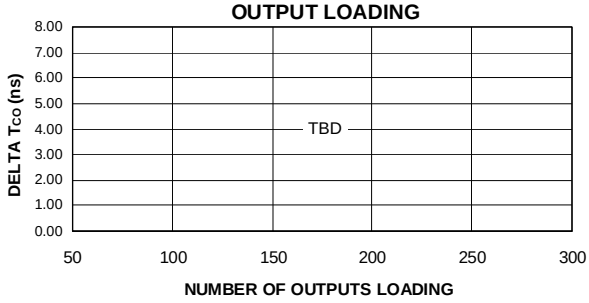
NORMALIZED T_{SU} VS. TEMP



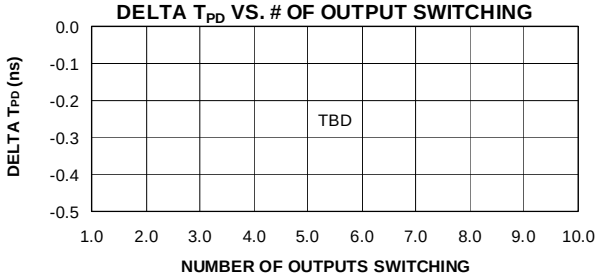
DELTA T_{PD} VS. OUTPUT LOADING



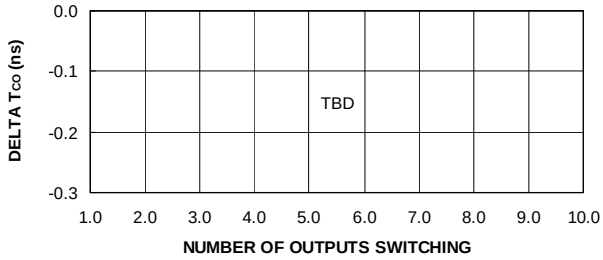
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING

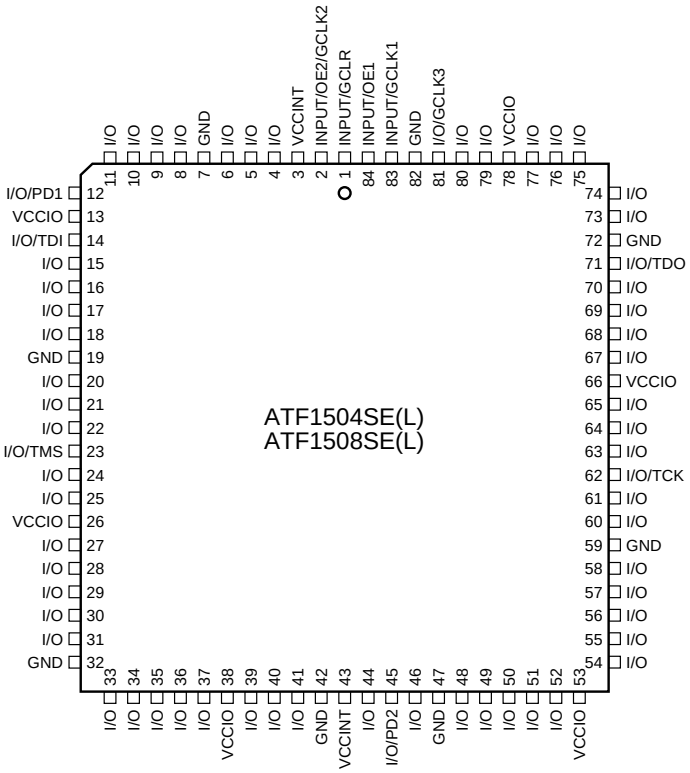


DELTA T_{CO} VS. # OF OUTPUT SWITCHING

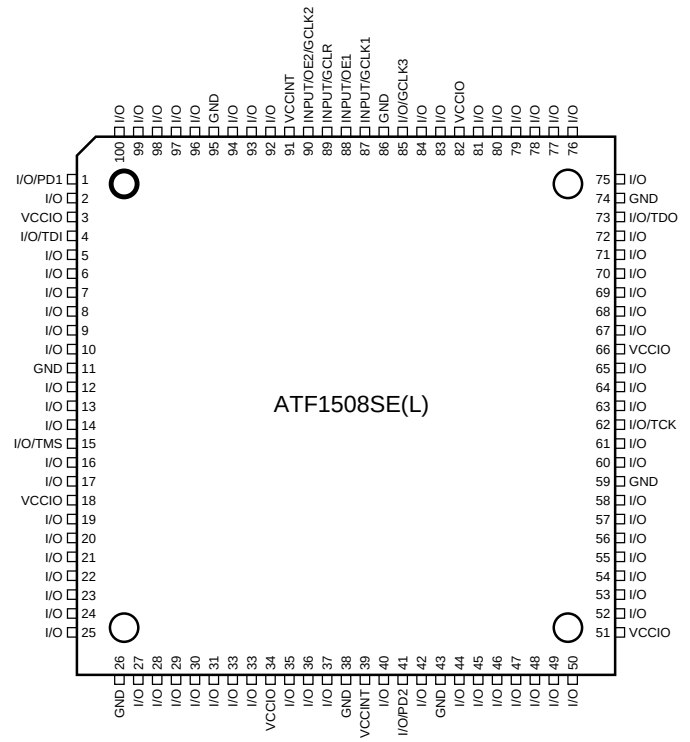


ATF1508SE(L) Pinouts

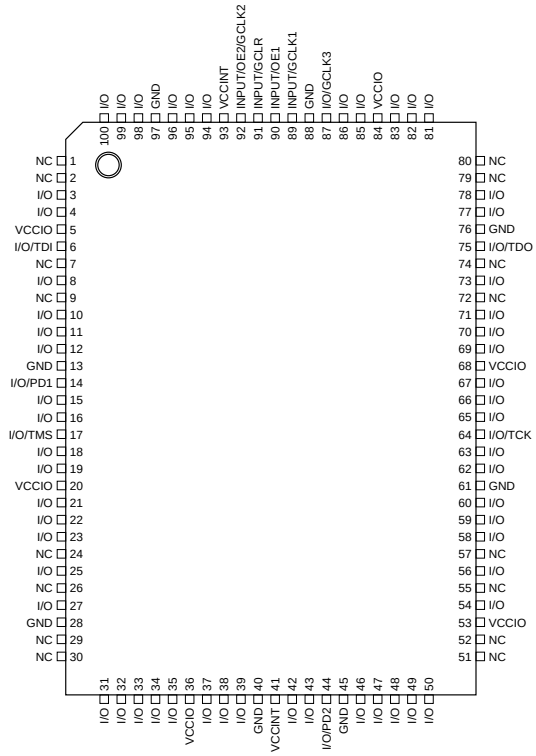
84-lead PLCC – Top View



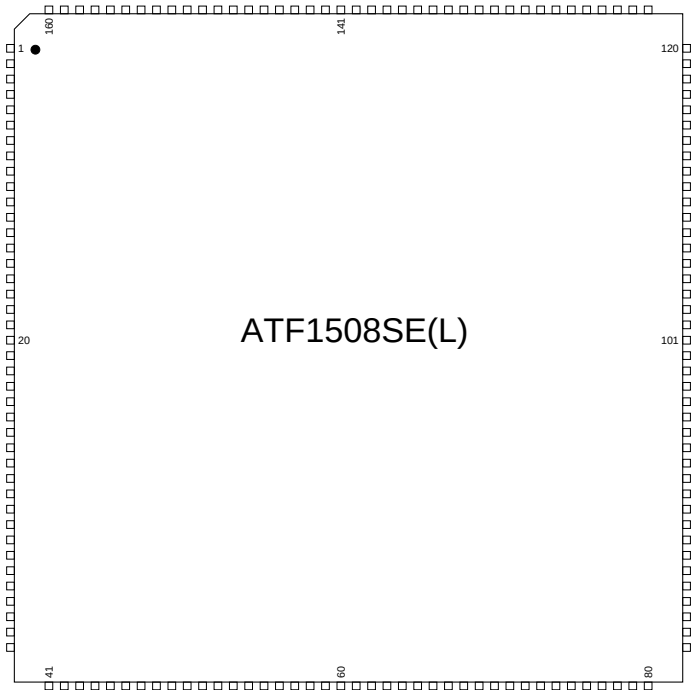
100-lead TQFP – Top View



100-lead PQFP – Top View



160-lead TQFP – Top View



ATF1508SE(L) Dedicated Pinouts

Dedicated Pin	84-PLCC J-Lead	100-pin TQFP	100-pin PQFP	160-lead PQFP
INPUT/GCLK1	83	87	89	139
INPUT/GCLR	1	89	91	141
INPUT/OE1	84	88	90	140
INPUT/OE2/GCK2	2	90	92	142
I/O/GCLK3	81	85	87	137
I/O PD (1,2)	12, 45	1,41	3, 43	63,159
TDI (JTAG)	14	4	6	9
TMS (JTAG)	23	15	17	22
TCK (JTAG)	62	62	64	99
TDO (JTAG)	71	73	75	112
GNDINT	42, 82	38,86	40,88	60,138
GNDIO	7, 19, 32, 47, 59, 72	11, 26, 43, 59, 74, 95	13, 28, 61, 76, 45, 97	17, 42,113, 66, 95,148
VCCINT	3, 43	39, 91	41,93	61,143
VCCIO	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	5,20,36,53,68,84	8,26,55,79,104,133
No Connect	-	-	–	1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157
# of Signal pins	68	84	84	100
# of User I/O pins	64	80	80	96

OE (1,2) Global OE pins.
GCLR Global Clear pin.
GCLK (1,2,3) Global Clock pins.
TDI, TMS, TCK, TDO JTAG pins used for In System Programming or Boundary-scan Testing.
GNDINT Ground pins for the internal device logic.
GNDIO Ground pins for the I/O drivers.
VCCINT VCC pins for the internal device logic.
VCCIO VCC pins for the I/O drivers.

ATF1508SE(L) I/O Pinouts

MC	PLB	84-PLCC J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-PLCC J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	–	4	2	160	33	C	–	27	25	41
2	A	–	–	–	–	34	C	–	–	–	–
3/**PD1**	A	12	3	1	159	35	C	31	26	24	33
4	A	–	–	–	158	36	C	–	–	–	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	–	–	–	–	39	C	–	–	–	–
8	A	9	100	98	151	40	C	28	23	21	29
9	A	–	99	97	150	41	C	–	22	20	28
10	A	–	–	–	–	42	C	–	–	–	–
11	A	8	98	96	149	43	C	27	21	19	27
12	A	–	–	–	147	44	C	–	–	–	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	–	–	–	–	47	C	–	–	–	–
16	A	4	94	92	144	48/**TMS**	C	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	–	–	–	–	50	D	–	–	–	–
19	B	21	15	13	20	51	D	40	38	36	58
20	B	–	–	–	19	52	D	–	–	–	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	–	12	10	16	54	D	–	35	33	54
23	B	–	–	–	–	55	D	–	–	–	–
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	–	–	–	–	58	D	–	–	–	–
27	B	16	9	7	13	59	D	35	32	30	51
28	B	–	–	–	12	60	D	–	–	–	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	–	7	5	10	62	D	–	30	28	48
31	B	–	–	–	–	63	D	–	–	–	–
32/ **TDI**	B/	14	6	4	9	64	D	33	29	27	43

ATF1508SE(L) I/O Pinouts (Continued)

MC	PLB	84-PLCC J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-PLCC J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
65	E	44	42	40	62	97	G	63	65	63	100
66	E	–	–	–	–	98	G	–	–	–	–
67/**PD2**	E	45	43	41	63	99	G	64	66	64	101
68	E	–	–	–	64	100	G	–	–	–	102
69	E	46	44	42	65	101	G	65	67	65	103
70	E	–	46	44	67	102	G	–	69	67	105
71	E	–	–	–	–	103	G	–	–	–	–
72	E	48	47	45	68	104	G	67	70	68	106
73	E	49	48	46	69	105	G	68	71	69	107
74	E	–	–	–	–	106	G	–	–	–	–
75	E	50	49	47	70	107	G	69	72	70	108
76	E	–	–	–	71	108	G	–	–	–	109
77	E	51	50	48	72	109	G	70	73	71	110
78	E	–	51	49	73	110	G	–	74	72	111
79	E	–	–	–	–	111	G	–	–	–	–
80	E	52	52	50	78	112/**TDO**	G	71	75	73	112
81	F	–	54	52	80	113	H	–	77	75	121
82	F	–	–	–	–	114	H	–	–	–	–
83	F	54	55	53	88	115	H	73	78	76	122
84	F	–	–	–	89	116	H	–	–	–	123
85	F	55	56	54	90	117	H	74	79	77	128
86	F	56	57	55	91	118	H	75	80	78	129
87	F	–	–	–	–	119	H	–	–	–	–
88	F	57	58	56	92	120	H	76	81	79	130
89	F	–	59	57	93	121	H	–	82	80	131
90	F	–	–	–	–	122	H	–	–	–	–
91	F	58	60	58	94	123	H	77	83	81	132
92	F	–	–	–	96	124	H	–	–	–	134
93	F	60	62	60	97	125	H	79	85	83	135
94	F	61	63	61	98	126	H	80	86	84	136
95	F	–	–	–	–	127	H	–	–	–	–
96	F/ **TCK**	62	64	62	99	128/**GCLK3**	H	81	87	85	137

ATF1508SE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
6.0	4.0	167	ATF1508SE-5 JC84 ATF1508SE-5 AC100 ATF1508SE-5 QC100 ATF1508SE-5 QC160	84J 100A 100Q4 160Q1	Commercial (0°C to 70°C)
7.5	4.5	167	ATF1508SE-7 JC84 ATF1508SE-7 AC100 ATF1508SE-7 QC100 ATF1508SE-7 QC160	84J 100A 100Q4 160Q1	Commercial (0°C to 70°C)
			ATF1508SE-7 JI84 ATF1508SE-7 AI100 ATF1508SE-7 QI100 ATF1508SE-7 QI160	84J 100A 100Q4 160Q1	Industrial (-40°C to +85°C)
10	5.0	125	ATF1508SE-10 JC84 ATF1508SE-10 AC100 ATF1508SE-10 QC100 ATF1508SE-10 QC160	84J 100A 100Q4 160Q1	Commercial (0°C to 70°C)
			ATF1508SE-10 JI84 ATF1508SE-10 AI100 ATF1508SE-10 QI100 ATF1508SE-10 QI160	84J 100A 100Q4 160Q1	Industrial (-40°C to +85°C)
15	8.0	100	ATF1508SEL-15 JC84 ATF1508SEL-15 AC100 ATF1508SEL-15 QC100 ATF1508SEL-15 QC160	84J 100A 100Q4 160Q1	Commercial (0°C to 70°C)

Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device and de-rate power by 30%.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flatpack (TQFP)
100Q4	100-lead, Plastic Quad Pin Flat Package (PQFP)
160Q1	160-lead, Plastic Quad Pin Flat Package (PQFP)

AC Characteristics[1] ATF1516SE(L)

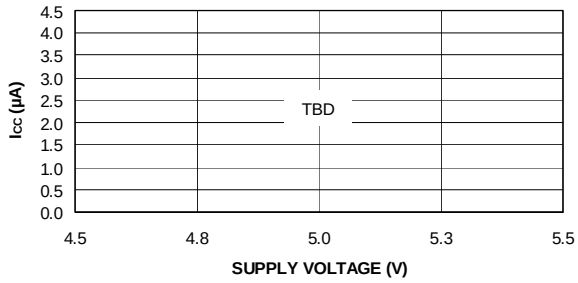
Symbol	Parameter	SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7.5		10		12	ns
t_{SU}	Global Clock Setup Time	3.9		7.0		11		ns
t_{H}	Global Clock Hold Time	0.0		0.0		0.0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3.9		3.0		3.0		ns
t_{FH}	Global Clock Hold of Fast Input	0.0		0.5		1		ns
t_{CO1}	Global Clock to Output Delay		4.7		5.0		8.0	ns
t_{CH}	Global Clock High Time	3.0		4.0		5.0		ns
t_{CL}	Global Clock Low Time	3.0		4.0		5		ns
t_{ASU}	Array Clock Setup Time	0.8		2.0		4.0		ns
t_{AH}	Array Clock Hold Time	1.9		3.0		4.0		ns
t_{ACO1}	Array Clock Output Delay		7.3	1	10		15	ns
t_{ACH}	Array Clock High Time	3.0		4		6		ns
t_{ACL}	Array Clock Low Time	3.0		4		6		ns
t_{CNT}	Minimum Clock Global Period		7.8		10		13	ns
f_{CNT}[3]	Maximum Internal Global Clock Frequency	130		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		7.8		10		13	ns
f_{ACNT}[4]	Maximum Internal Array Clock Frequency	130		100		77		MHz
f_{MAX}[5]	Maximum Clock Frequency	167		125		100		MHz
t_{IN}	Input Pad and Buffer Delay		0.3		0.5		2.0	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.3		0.5		2.0	ns
t_{FIN}	Fast Input Delay		3.4		1.0		2.0	ns
t_{SEXP}	Foldback Term Delay		3.9		5.0		8.0	ns
t_{PEXP}	Cascade Logic Delay		1.1		0.8		1.0	ns
t_{LAD}	Logic Array Delay		2.6		5.0		6.0	ns
t_{LAC}	Logic Control Delay		2.6		5.0		6.0	ns
t_{IOE}	Internal Output Enable Delay		0.8		2.0		3.0	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		0.5		1.5		4.0	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		1.0		2.0		5.0	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		5.5		5.5		8.0	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35 pF)		4.0		5.0		6.0	ns

AC Characteristics[1] ATF1516SE(L) (Continued)

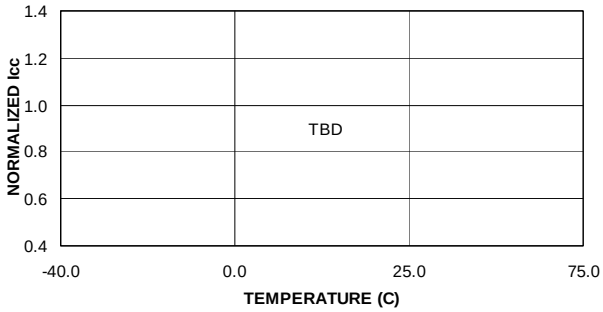
Symbol	Parameter	SE -7		SE -10		SEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35 pF)		4.5		5.5		7.0	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35 pF)		9.0		9.0		10.0	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5 pF)		4.0		5.0		6.0	ns
t_{SU}	Register Setup Time	1.1		2.0		4.0		ns
t_H	Register Hold Time	1.6		3.0		4.0		ns
t_{FSU}	Register Setup Time of Fast Input	2.4		3.0		2.0		ns
t_{FH}	Register Hold Time of Fast Input	0.6		0.5		1.0		ns
t_{RD}	Register Delay		1.1		2.0		1.0	ns
t_{COMB}	Combinatorial Delay		1.1		2.0		1.0	ns
t_{IC}	Array Clock Delay		2.9		5.0		6.0	ns
t_{EN}	Register Enable Time		2.6		5.0		6.0	ns
t_{GLOB}	Global Control Delay		2.8		1.0		1.0	ns
t_{PRE}	Register Preset Time		2.7		3.0		4.0	ns
t_{CLR}	Register Clear Time		2.7		3.0		4.0	ns
t_{UIM}	Switch Matrix Delay		3.0		1.0		2.0	ns
t_{RPA}	Reduced Power Adder[2]		10		11		13	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipelined data.
6. For clocked applications and frequencies above $f_{CRITICAL}$, OR, non-clocked applications with dormant times less than $1/f_{CRITICAL}$, the device will achieve the speeds of the –10 column. See “Input Transition Detection/ Automatic Power Down” on page 8.

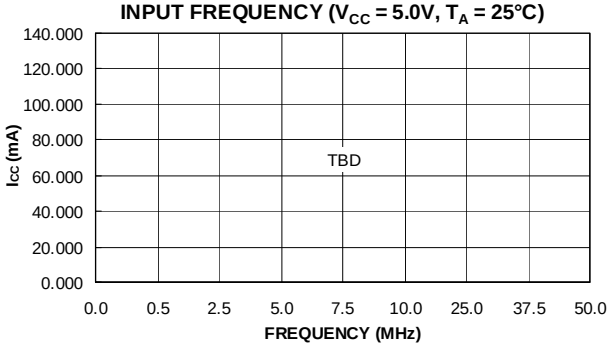
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



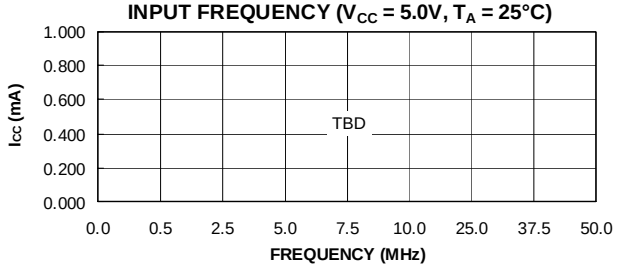
NORMALIZED I_{CC} VS. TEMP



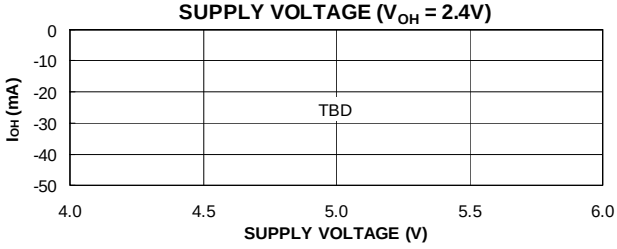
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



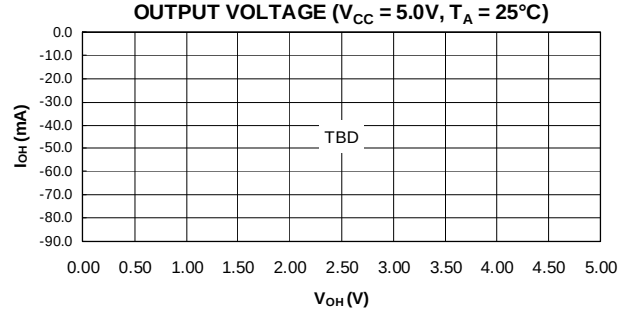
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



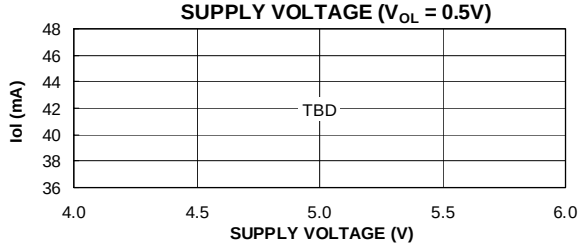
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



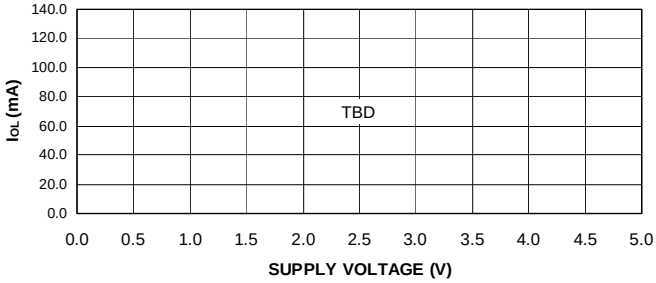
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



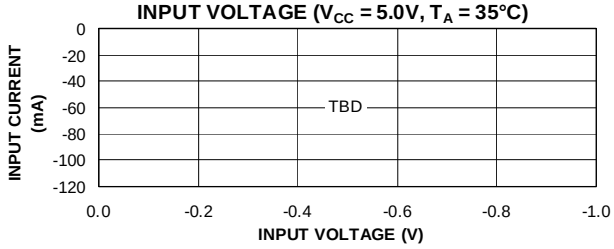
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



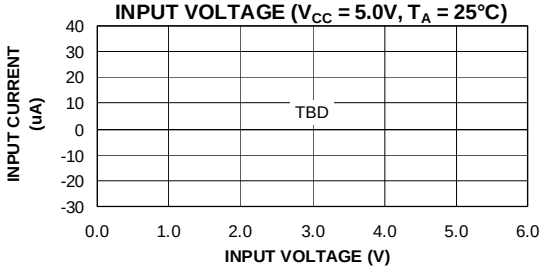
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



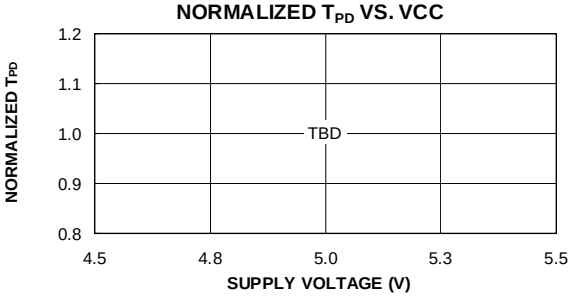
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



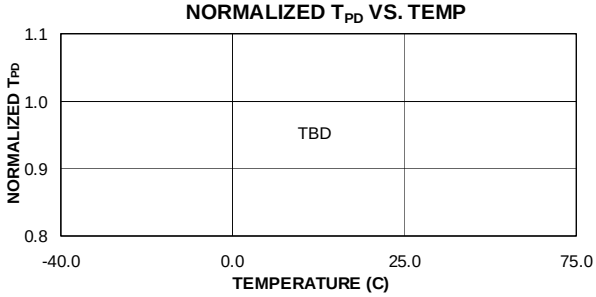
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



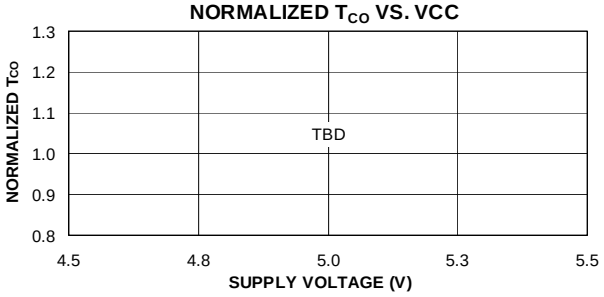
NORMALIZED T_{PD} VS. VCC



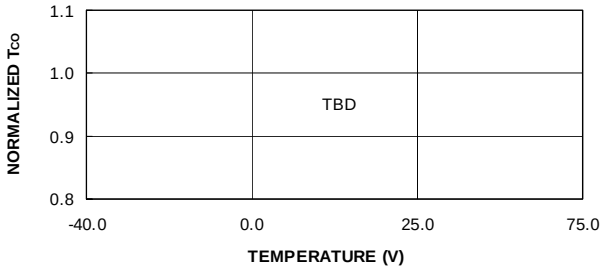
NORMALIZED T_{PD} VS. TEMP



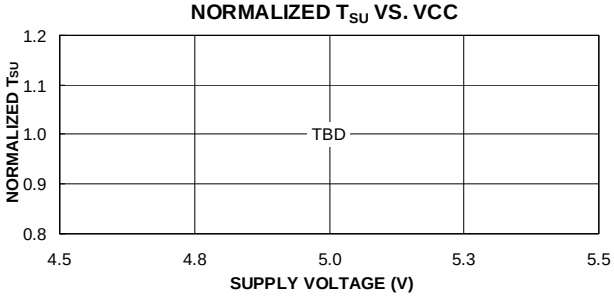
NORMALIZED T_{CO} VS. VCC



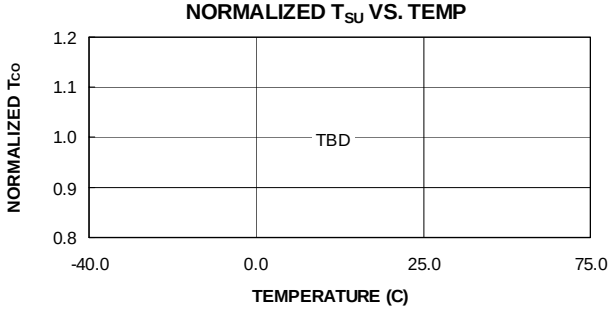
NORMALIZED T_{CO} VS. TEMP



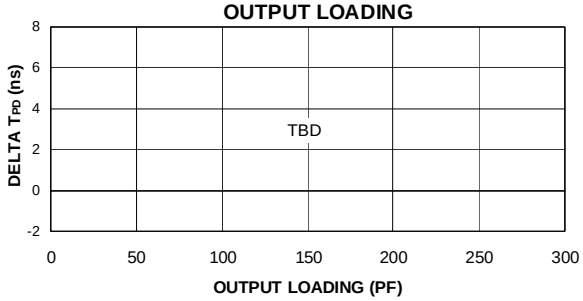
NORMALIZED T_{SU} VS. VCC



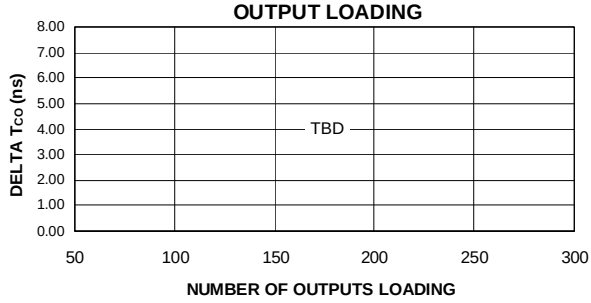
NORMALIZED T_{SU} VS. TEMP



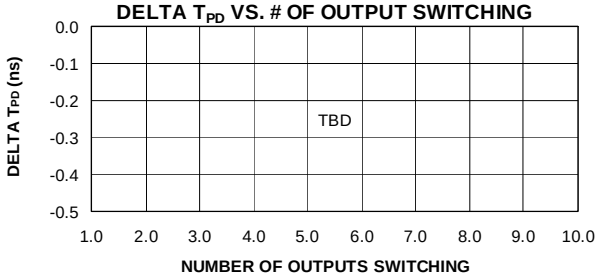
DELTA T_{PD} VS. OUTPUT LOADING



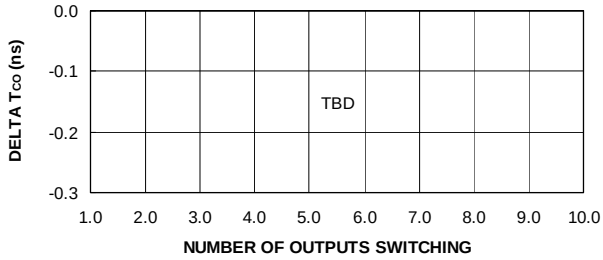
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING

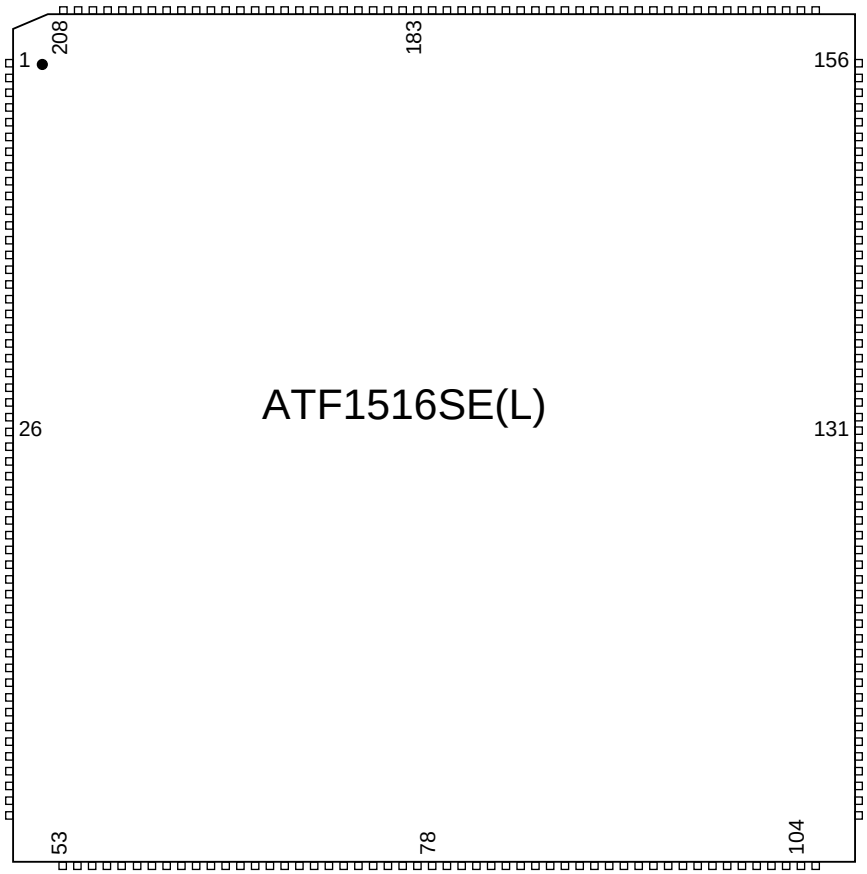


DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF1516SE(L) Dedicated Pinouts

208-lead PQFP and RQFP – Top View



ATF1516SE(L) Dedicated Pinouts

Dedicated Pin	208-pin PQFP	208-pin RQFP
INPUT/GCLK1	184	184
INPUT/GCLR	182	182
INPUT/OE1	183	183
INPUT/OE2/GCK2	181	181
I/O/GCLK3	TBD	TBD
I/O PD (1,2)	TBD	TBD
TDI (JTAG)	176	176
TMS (JTAG)	127	127
TCK (JTAG)	30	30
TDO (JTAG)	189	189
GNDINT	75, 82, 180, 185	75, 82, 180, 185
GNDIO	14, 32, 50, 72, 94, 116, 134, 152, 174, 200	14, 32, 50, 72, 94, 116, 134, 152, 174, 200
VCCINT	74, 83, 179, 186	74, 83, 179, 186
VCCIO	5, 23, 41, 63, 85, 107, 125, 143, 165, 191	5, 23, 41, 63, 85, 107, 125, 143, 165, 191
No Connect	1,2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208	1,2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208
# of Signal pins	164	164
# of User I/O pins	160	160

OE (1,2) Global OE pins.
GCLR Global Clear pin.
GCLK (1,2,3) Global Clock pins.
TDI, TMS, TCK, TDO JTAG pins used for In System Programming or Boundary-scan Testing.
GNDINT Ground pins for the internal device logic.
GNDIO Ground pins for the I/O drivers.
VCCINT VCC pins for the internal device logic.
VCCIO VCC pins for the I/O drivers.

ATF1516SE(L) I/O Pinouts

MC	PLB	208-pin PQFP	208-pin RQRP	MC	PLB	208-pin PQFP	208-pin RQFP
1	A	153	153	33	C	108	108
2	A	-	-	34	C	-	-
3	A	154	154	35	C	109	109
4	A	-	-	36	C	-	-
5	A	159	159	37	C	110	110
6	A	160	160	38	C	111	111
7	A	-	-	39	C	-	-
8	A	161	161	40	C	112	112
9	A	162	162	41	C	113	113
10	A	-	-	42	C	-	-
11	A	163	163	43	C	114	114
12	A	-	-	44	C	-	-
13	A	164	164	45	C	115	115
14	A	166	166	46	C	117	117
15	A	-	-	47	C	-	-
16	A	167	167	48	C	118	118
17	B	141	141	49	D	92	92
18	B	-	-	50	D	-	-
19	B	142	142	51	D	93	93
20	B	-	-	52	D	-	-
21	B	144	144	53	D	95	95
22	B	145	145	54	D	96	96
23	B	-	-	55	D	-	-
24	B	146	146	56	D	97	97
25	B	147	147	57	D	98	98
26	B	-	-	58	D	-	-
27	B	148	148	59	D	99	99
28	B	-	-	60	D	-	-
29	B	149	149	61	D	100	100
30	B	150	150	62	D	101	101
31	B	-	-	63	D	-	-
32	B	151	151	64	D	102	102

ATF1516SE(L) I/O Pinouts (Continued)

MC	PLB	208-pin PQFP	208-pin RQRP	MC	PLB	208-pin PQFP	208-pin RQFP
65	E	168	168	97	G	119	119
66	E	-	-	98	G	-	-
67	E	169	169	99	G	120	120
68	E	-	-	100	G	-	-
69	E	170	170	101	G	121	121
70	E	171	171	102	G	122	122
71	E	-	-	103	G	-	-
72	E	172	172	104	G	123	123
73	E	173	173	105	G	124	124
74	E	-	-	106	G	-	-
75	E	175	175	107	G	126	126
76	E	-	-	108	G	-	-
77	E	176	176	109	G	127	127
78	E	177	177	110	G	128	128
79	E	-	-	111	G	-	-
80	E	178	178	112	G	129	129
81	F	130	130	113	H	79	79
82	F	-	-	114	H	-	-
83	F	131	131	115	H	80	80
84	F	-	-	116	H	-	-
85	F	132	132	117	H	81	81
86	F	133	133	118	H	84	84
87	F	-	-	119	H	-	-
88	F	135	135	120	H	86	86
89	F	136	136	121	H	87	87
90	F	-	-	122	H	-	-
91	F	137	137	123	H	88	88
92	F	-	-	124	H	-	-
93	F	138	138	125	H	89	89
94	F	139	139	126	H	90	90
95	F	-	-	127	H	-	-
96	F	140	140	128	H	91	91

ATF1516SE(L) I/O Pinouts (Continued)

MC	PLB	208-pin PQFP	208-pin RQRP	MC	PLB	208-pin PQFP	208-pin RQFP
129	I	197	197	161	K	38	38
130	I	-	-	162	K	-	-
131	I	196	196	163	K	37	37
132	I	-	-	164	K	-	-
133	I	195	195	165	K	36	36
134	I	194	194	166	K	35	35
135	I	-	-	167	K	-	-
136	I	193	193	168	K	34	34
137	I	192	192	169	K	33	33
138	I	-	-	170	K	-	-
139	I	190	190	171	K	31	31
140	I	-	-	172	K	-	-
141	I	189	189	173	K	30	30
142	I	188	188	174	K	29	29
143	I	-	-	175	K	-	-
144	I	187	187	176	K	28	28
145	J	27	27	177	L	78	78
146	J	-	-	178	L	-	-
147	J	26	26	179	L	77	77
148	J	-	-	180	L	-	-
149	J	25	25	181	L	76	76
150	J	24	24	182	L	73	73
151	J	-	-	183	L	-	-
152	J	22	22	184	L	71	71
153	J	21	21	185	L	70	70
154	J	-	-	186	L	-	-
155	J	20	20	187	L	69	69
156	J	-	-	188	L	-	-
157	J	19	19	189	L	68	68
158	J	18	18	190	L	67	67
159	J	-	-	191	L	-	-
160	J	17	17	192	L	66	66

ATF1516SE(L) I/O Pinouts (Continued)

MC	PLB	208-pin PQFP	208-pin RQRP	MC	PLB	208-pin PQFP	208-pin RQFP
193	M	4	4	225	O	49	49
194	M	-	-	226	O	-	-
195	M	3	3	227	O	48	48
196	M	-	-	228	O	-	-
197	M	206	206	229	O	47	47
198	M	205	205	230	O	46	46
199	M	-	-	231	O	-	-
200	M	204	204	232	O	45	45
201	M	203	203	233	O	44	44
202	M	-	-	234	O	-	-
203	M	202	202	235	O	43	43
204	M	-	-	236	O	-	-
205	M	201	201	237	O	42	42
206	M	199	199	238	O	40	40
207	M	-	-	239	O	-	-
208	M	198	198	240	O	39	39
209	N	16	16	241	P	65	65
210	N	-	-	242	P	-	-
211	N	15	15	243	P	64	64
212	N	-	-	244	P	-	-
213	N	13	13	245	P	62	62
214	N	12	12	246	P	61	61
215	N	-	-	247	P	-	-
216	N	11	11	248	P	60	60
217	N	10	10	249	P	59	59
218	N	-	-	250	P	-	-
219	N	9	9	251	P	58	58
220	N	-	-	252	P	-	-
221	N	8	8	253	P	57	57
222	N	7	7	254	P	56	56
223	N	-	-	255	P	-	-
224	N	6	6	256	P	55	55

ATF1516SE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.7	167	ATF1516SE-7 QC208 ATF1516SE-7 RC208	208Q1 208Q2	Commercial (0°C to 70°C)
			ATF1516SE-7 QI208 ATF1516SE-7 RI208	208Q1 208Q2	Industrial (-40°C to +85°C)
10	5.0	125	ATF1516SE-10 QC208 ATF1516SE-10 RC208	208Q1 208Q2	Commercial (0°C to 70°C)
			ATF1516SE-10 QI208 ATF1516SE-10 RI208	208Q1 208Q2	Industrial (-40°C to +85°C)
15	8.0	100	ATF1516SEL-15 QC208 ATF1516SEL-15 RC208	208Q1 208Q2	Commercial (0°C to 70°C)

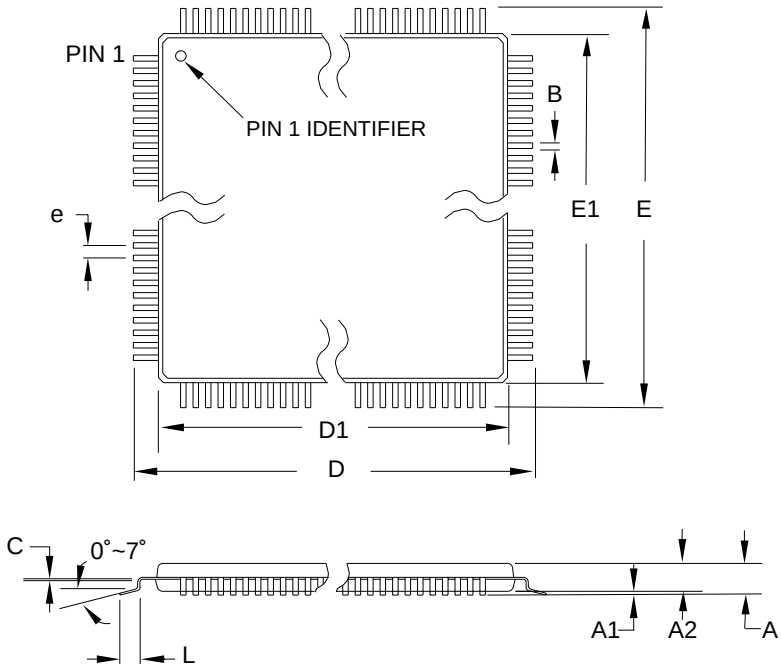
Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device, and de-rate power by 30%.

Package Type	
208Q1	208-lead, 28 x 28 mm Body, 2.6 Form Opt., Plastic Quad Flatpack (PQFP)
208Q2	208-lead, 28 x 28 mm Body, 2.6 Form Opt., Plastic Quad Flatpack with Heat Spreader (PQFP)

Package Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

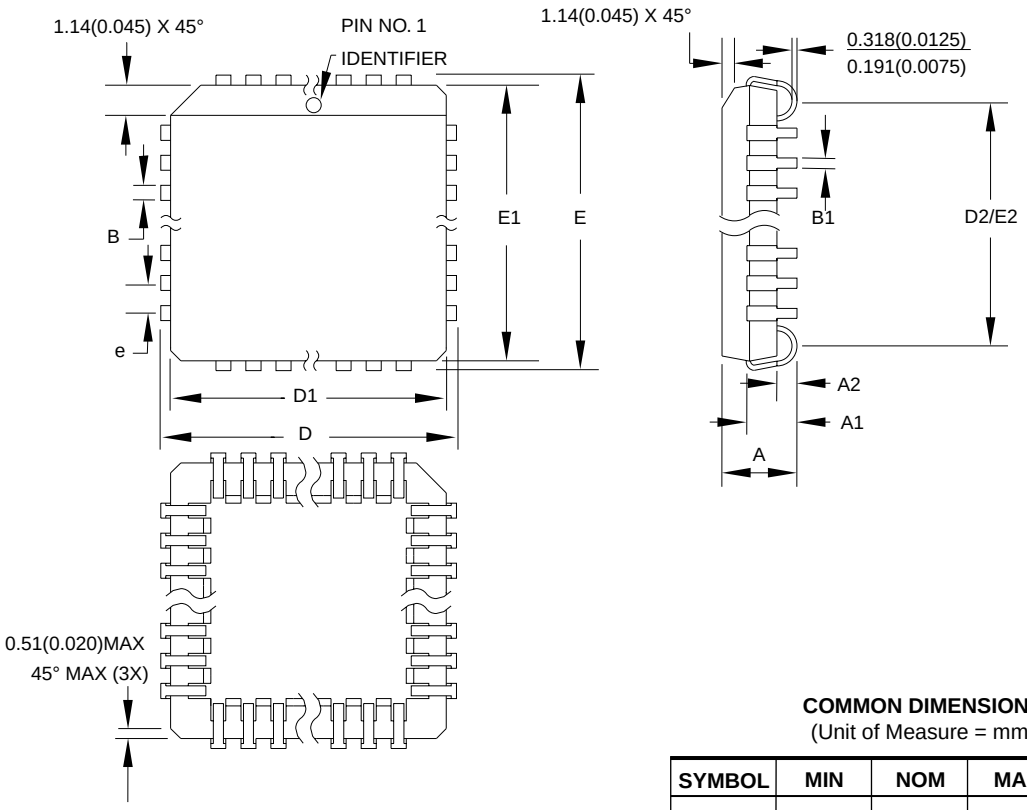
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

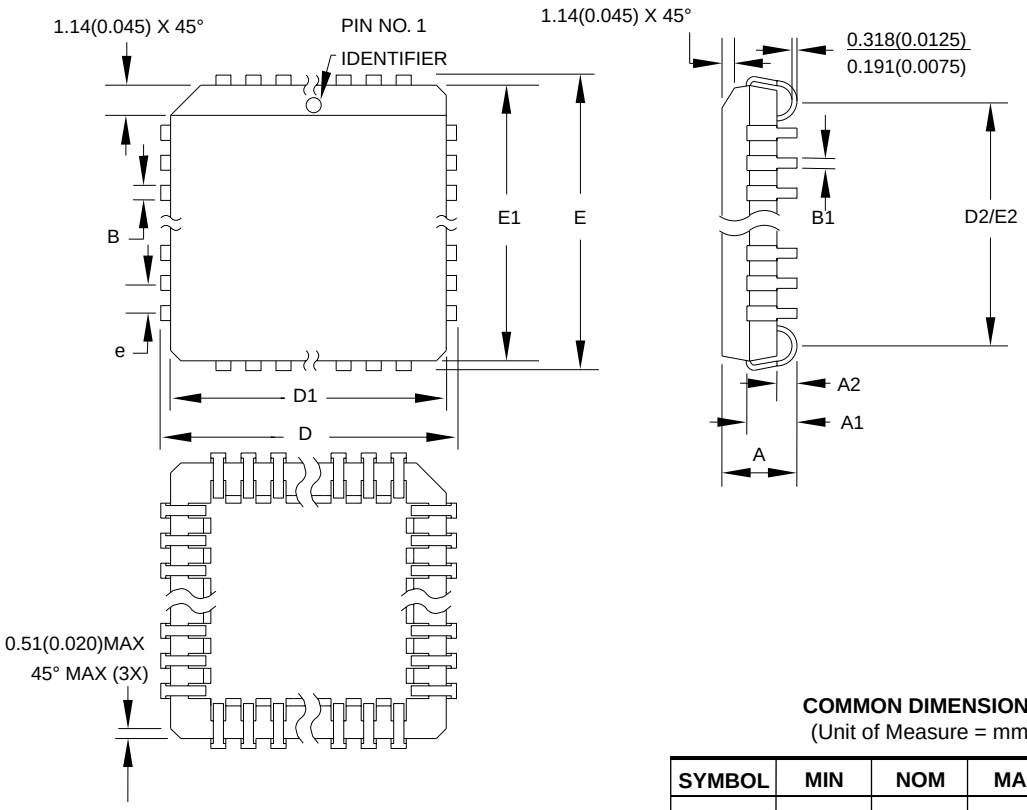
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

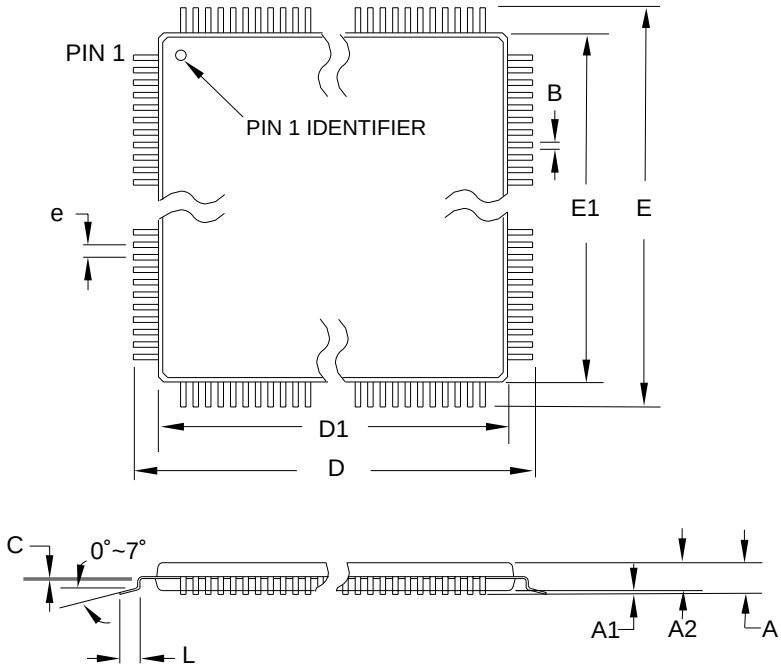
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

100A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

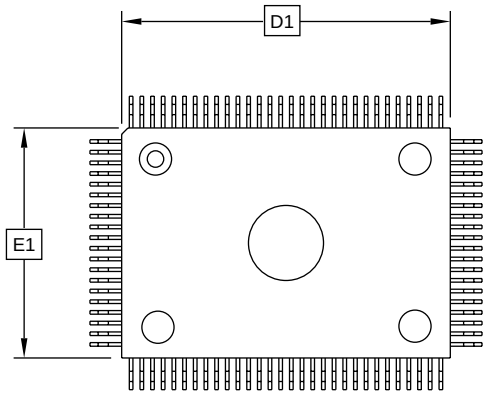
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

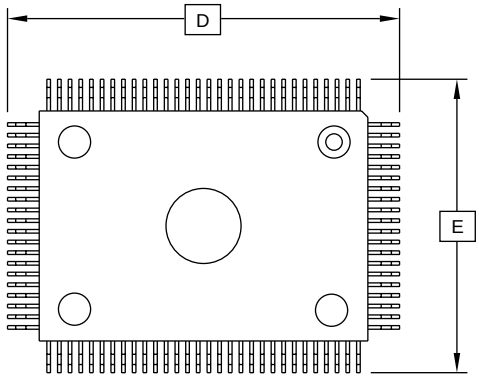
10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C

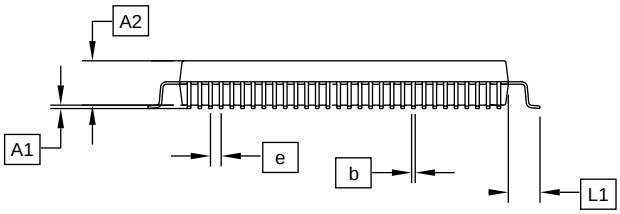
100Q4 – PQFP



Top View



Bottom View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-022, Variation GC-1, for additional information.
2. To be determined at seating plane.
3. Regardless of the relative size of the upper and lower body sections, dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold Flash and gate burrs, but including any mismatch between the upper and lower sections of the molded body.
4. Dimension b does not include Dambar protrusion. The Dambar protrusion(s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
5. A1 is defined as the distance from the seating plane to the lowest point of the package body.

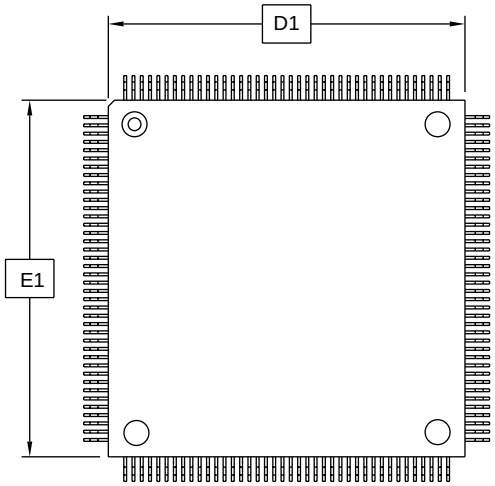
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	5
A2	2.50	2.70	2.90	
D		23.20 BSC		2
D1		20.00 BSC		3
E		17.20 BSC		2
E1		14.00 BSC		3
e		0.65 BSC		
b	0.22		0.40	4
L1		1.60 REF		

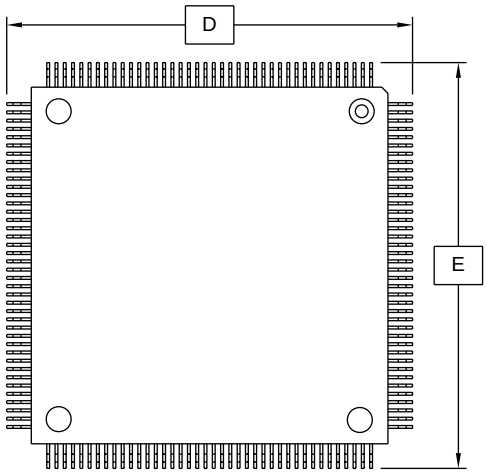
3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100Q4,** 100-lead, 14 x 20 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	100Q4	A

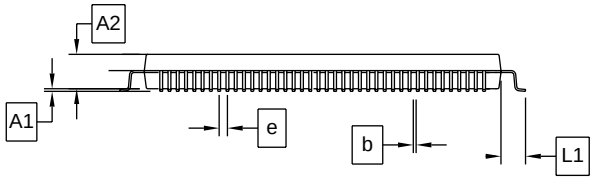
160Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

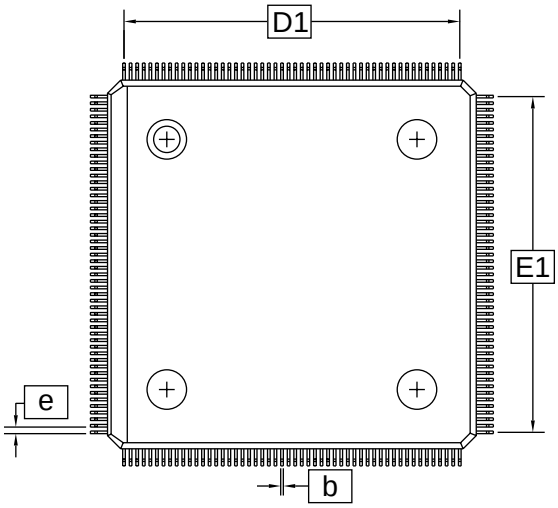
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	5
A2	3.20	3.40	3.60	
D	31.20 BSC			2
D1	28.00 BSC			3
E	31.20 BSC			2
E1	28.00 BSC			3
e	0.65 BSC			
b	0.22	–	0.40	4
L1	1.60 REF			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-022, Variation DD-1, for additional information.
2. To be determined at seating plane.
3. Regardless of the relative size of the upper and lower body sections, dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold Flash and gate burrs, but including any mismatch between the upper and lower sections of the molded body.
4. Dimension b does not include Dambar protrusion. The Dambar protrusion(s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
5. A1 is defined as the distance from the seating plane to the lowest point of the package body.

3/28/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**160Q1,** 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	160Q1	A

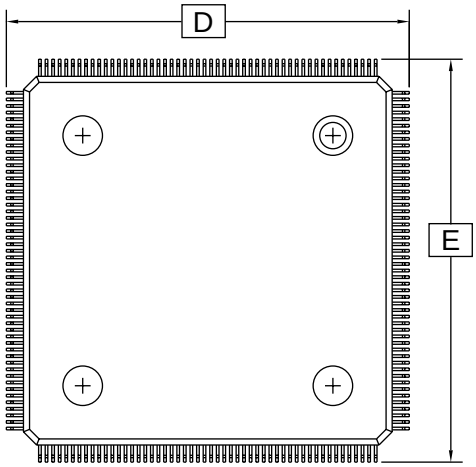
208Q1 – PQFP



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

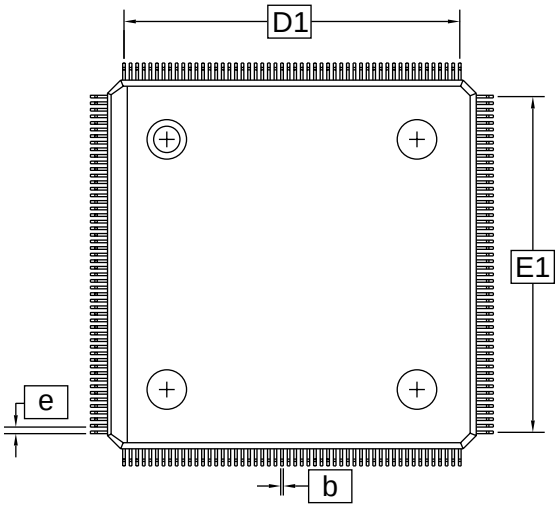
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		30.60 BSC		
D1		28.00 BSC		2, 3
E		30.60 BSC		
E1		28.00 BSC		2, 3
e		0.50 BSC		
b	0.17	–	0.27	4
L1		1.30 REF		

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

07/23/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	208Q1	B

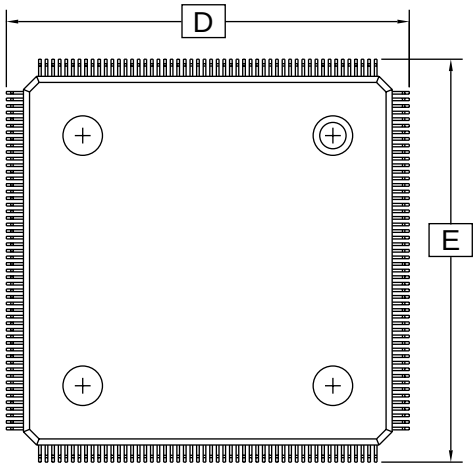
208Q2 – PQFP



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05	–	0.25	
A2	3.20	3.40	3.60	
D	30.60 BSC			
D1	28.00 BSC			2, 3
E	30.60 BSC			
E1	28.00 BSC			2, 3
e	0.50 BSC			
b	0.17	–	0.27	4
L1	1.30 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-2, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

07/23/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**208Q2**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	208Q2	A

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