Features

- ATA6833 Temperature Range T_A = 125°C, T_J = 150°C
- ATA6834 Extended Temperature Range T_A = 150°C, T_J = 200°C
- Direct Driving of 6 External NMOS Transistors with a Maximum Switching Frequency of 50 kHz
- Integrated Charge Pump to Provide Gate Voltages for High-side Drivers and to Supply the Gate of the External Battery Reverse Protection NMOS
- Built-in 5V/3.3V Voltage Regulator with Current Limitation
- Reset Signal for the Microcontroller
- Sleep Mode with Supply Current of typically < 45 µA
- Wake-up via LIN Bus or High Voltage Input
- Programmable Window Watchdog
- Battery Overvoltage Protection and Battery Undervoltage Management
- Overtemperature Warning and Protection (Shutdown)
- 200 mA Peak Current for Each Output Driver
- LIN Transceiver Conformal to LIN 2.1 and SAEJ2602-2 with Outstanding EMC and ESD Performance
- QFN48 Package 7 mm × 7 mm

1. Description

The ATA6833 and ATA6834 are system basis chips for three-phase brushless DC motor controllers designed in Atmel®'s state-of-the-art 0.8 µm SOI technology SMART-I.S.™1. In combination with a microcontroller and six discrete power MOSFETs, the system basis chip forms a BLDC motor control unit for automotive applications. In addition, the circuits provide a 3.3V/5V linear regulator and a window watchdog.

The circuit includes various control and protection functions like overvoltage and overtemperature protection, short circuit detection, and undervoltage management. Thanks to these function blocks, the driver fulfils a maximum of safety requirements and offers a high integration level to save cost and space in various applications. The target applications are most suitable for the automotive market due to the robust technology and the high qualification level. ATA6834, in particular, is designed for applications in a high-temperature environment.

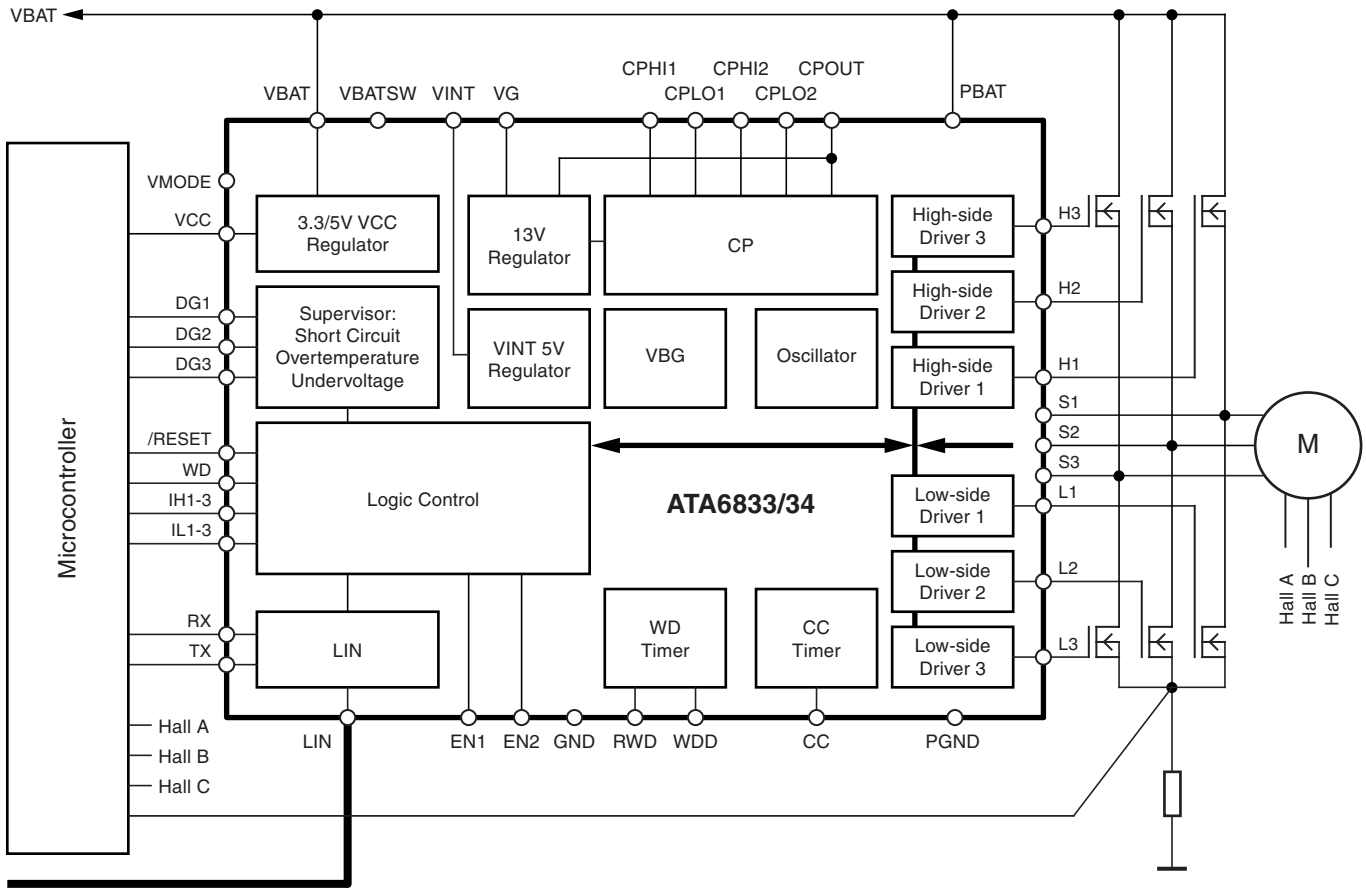
BLDC Motor Driver and LIN System Basis Chip

ATA6833
ATA6834

Preliminary

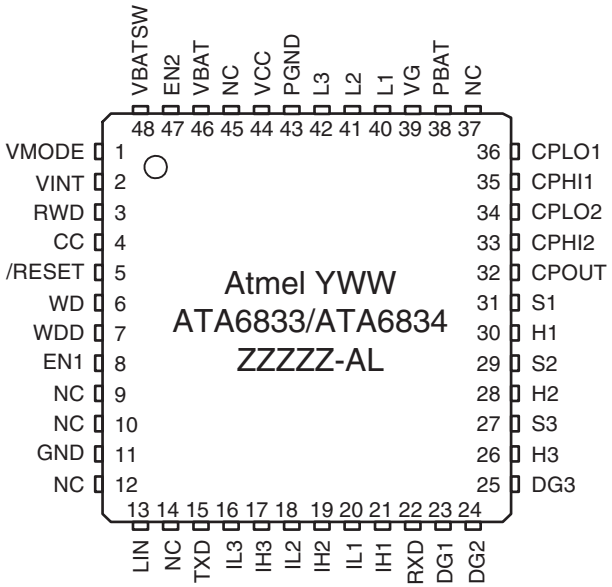
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Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN48



Note:

YWW	Date code (Y = Year - above 2000, WW = week number)
ATA683x	Product name
ZZZZZ	Wafer lot number
AL	Assembly sub-lot number

Table 2-1. Pin Description

Pin	Symbol	I/O	Function
1	VMODE	I	Selector for V_{CC} and interface logic voltage level
2	VINT	I/O	Blocking capacitor
3	RWD	I	Resistor defining the watchdog interval
4	CC	I/O	RC combination to adjust cross conduction time
5	/RESET	O	Reset signal for microcontroller
6	WD	I	Watchdog trigger signal
7	WDD	I	Enable and disable the watchdog
8	EN1	I	Microcontroller output to switch system in Sleep Mode
9	N.C.		Connect to GND
10	N.C.		Connect to GND
11	GND	I	Ground
12	NC		Connect to GND
13	LIN	I/O	LIN-bus terminal
14	NC		Connect to GND
15	TXD	I	Transmit signal to LIN bus from microcontroller
16	IL3	I	Control Input for output L3
17	IH3	I	Control Input for output H3

Table 2-1. Pin Description

Pin	Symbol	I/O	Function
18	IL2	I	Control Input for output L2
19	IH2	I	Control Input for output H2
20	IL1	I	Control Input for output L1
21	IH1	I	Control Input for output H1
22	RXD	O	Receive signal from LIN bus for microcontroller
23	DG1	O	Diagnostic output 1
24	DG2	O	Diagnostic output 2
25	DG3	O	Diagnostic output 3
26	H3	O	Gate voltage high-side 3
27	S3	I/O	Voltage at half bridge 3
28	H2	O	Gate voltage high-side 2
29	S2	I/O	Voltage at half bridge 2
30	H1	O	Gate voltage high-side 1
31	S1	I/O	Voltage at half bridge 1
32	CPOUT	I/O	Charge pump output capacitor
33	CPHI2	I	Charge pump capacitor 2
34	CPLO2	O	Charge pump capacitor 2
35	CPHI1	I	Charge pump capacitor 1
36	CPLO1	O	Charge pump capacitor 1
37	NC		Connect to GND
38	PBAT	I	Power supply (after reverse protection) for charge pump and gate drivers
39	VG	I/O	Blocking capacitor
40	L1	O	Gate voltage H-bridge, low-side 1
41	L2	O	Gate voltage H-bridge, low-side 2
42	L3	O	Gate voltage H-bridge, low-side 3
43	PGND	I	Power ground for H-bridge and charge pump
44	VCC	O	5V/100 mA supply for microcontroller
45	NC		Connect to GND
46	VBAT	I	Supply voltage for IC core (after reverse protection)
47	EN2	I	High voltage enable input
48	VBATSW	O	100Ω PMOS switch from V_{BAT}

3. Functional Description

3.1 Power Supply Unit with Supervisor Functions

3.1.1 Power Supply

The IC has to be supplied by a reverse-protected battery voltage. To prevent damage to the IC, proper external protection circuitry has to be added. It is recommended to use at least one capacitor combination of storage and RF capacitors behind the reverse protection circuitry, which is connected close to the VBAT and GND pins of the IC.

A fully integrated low-power and low-drop regulator (VINT regulator), stabilized by an external blocking capacitor, provides the necessary low-voltage supply needed for the wake-up process. A trimmed low-power band gap is used as reference for the VINT regulator as well as for the VCC regulator. All internal blocks are supplied by VINT regulator. VINT regulator must not be used for any external supply purposes.

Nothing inside the IC except the logic interface to the external microcontroller is supplied by the 5V/3.3V VCC regulator.

Both voltage regulators are checked by a “power-good comparator”, which keeps the whole chip in reset as long as the internal supply voltage (VINT regulator output) is too low and generates a reset for the external microcontroller if the output voltage of the VCC regulator is not sufficient.

3.1.2 VBatt Switch

This high-voltage switch provides the battery voltage at pin VBATSW for various purposes. It is switched ON after power on reset when the IC transits to Active Mode and it will only turn OFF when the IC changes to Sleep Mode. Watchdog resets do not have an effect on the switch. The switch can be used for measuring purposes as well as to switch on external voltage regulators.

3.1.3 Voltage Supervisor

This function is implemented to protect the IC and the external power MOS transistors from damage due to overvoltage on PBAT input. In the event of overvoltage (V_{THOV}) or undervoltage (V_{THUV}), the external NMOS motor driver transistors will be switched off. The failure state will be flagged on DG2 pin. It is recommended to block PBAT with an external RF capacitor to suppress high frequency disturbances.

3.1.4 Temperature Supervisor

An integrated temperature sensor prevents the IC from overheating. If the temperature is above the overtemperature pre-warning threshold $T_{JPW\ set}$, the diagnostic pin DG3 will be switched to HIGH to signal this event to the external microcontroller. The microcontroller should take actions to reduce the power dissipation in the IC. If the temperature rises above the overtemperature shutdown threshold $T_{J\ switch\ off}$, the VCC regulator and all output drivers together with the LIN transceiver will be switched OFF immediately and the /RESET signal will go LOW. Both thresholds have a built-in hysteresis to avoid oscillations. The IC will return to normal operation (Active Mode) when it has cooled down below the shutdown threshold. When the junction temperature drops below the pre-warning threshold, bit DG3 will be switched LOW.

3.2 Active Mode and Sleep Mode

The IC has two modes: Sleep Mode and Active Mode. Switching between the modes is described below. By default the IC starts in Active Mode (which means normal operation) after power-on. A *Go to Sleep* procedure switches the IC from Active Mode to Sleep Mode (standby). A *Go to Active* procedure brings the IC back from Sleep Mode to Active Mode. When in Sleep Mode the internal 5V supply (VINT regulator), the EN2 pin input structure, and a certain part of the LIN receiver remain active to ensure a proper startup of the system. The VCC regulator is turned off.

The *Go to Sleep* and *Go to Active* procedures are implemented as follows:

Go to Sleep:

Pin EN1 is a low-voltage input supplied by the VCC regulator. It is ESD protected by diodes against VCC and GND. Thus the input voltage at pin EN1 must not go below GND or exceed the output voltage of the VCC regulator. A transition from HIGH to LOW followed by a permanent LOW signal for a minimum time period $t_{gotosleep}$ (typical 10 µs) at pin EN1 switches the IC to Sleep Mode as the EN1 is edge triggered. V_{CC} is switched off in Sleep Mode. It is recommended to keep EN1 LOW during normal operation.

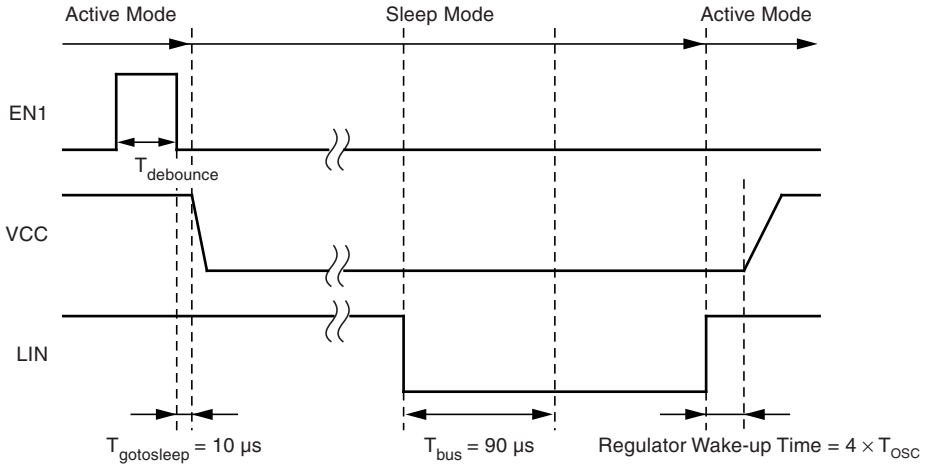
Go to Active Using Pin EN2:

Pin EN2 is a high-voltage input for external wake-up signals. Its input structure consists of a comparator with a built-in hysteresis. It is ESD-protected by diodes against GND and V_{BAT}, B, and for this reason the applied input voltage must not go below GND or exceed V_{BAT}. Pulling EN2 up to V_{BAT} switches the IC to Active Mode. EN2 is debounced and edge triggered.

Go to Active Using the LIN Interface:

Using the LIN interface provides a second possibility to wake-up the IC (see Figure 3-1). A falling edge at pin LIN followed by a dominant bus level maintained for a minimum time period (T_{bus}) and ending with a rising edge leads to a remote wake-up request. The device switches from Sleep Mode to Active Mode. The VCC regulator is activated and the internal LIN slave termination resistor is switched on.

Figure 3-1. Wake-up Using the LIN Interface



3.3 5V/3.3V VCC Regulator

The 5V/3.3V regulator is fully integrated. It requires an external electrolytic capacitor in the range of 2.2 µF up to 10 µF and with an ESR in the range from 2Ω to 15Ω for stability (see Figure 3-2). The output voltage can be configured as either 5V or 3.3V by connecting pin VMODE to either pin VINT or GND. Since the regulator is not designed to be switched between both output voltages during operation, it is advisable to hard-wire VMODE pin. The logic levels of the microcontroller interface are adapted to the VCC regulator output voltage. The maximum output current (I_{OS1}) of the regulator is 100 mA. For T_J > 150°C the I_{OS1} of ATA6834 is reduced to 80 mA. The VCC regulator has a built-in short circuit protection. A comparator checks the output voltage of the VCC regulator and keeps the external microcontroller in reset as long as the voltage is below the lower operation minimum (shown in Figure 3-33).

Figure 3-2. ESR versus Load Current for External Capacitors with Different Values

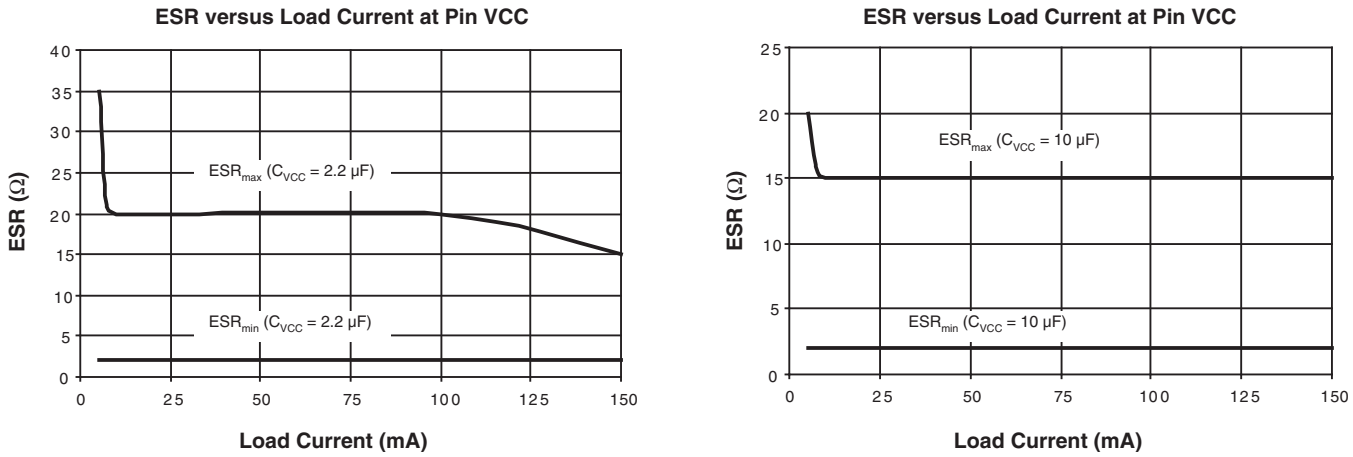
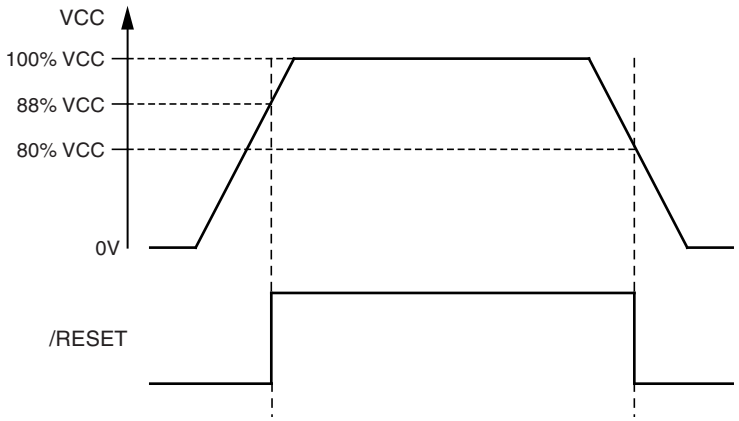


Figure 3-3. /RESET as Function of the VCC Output Voltage

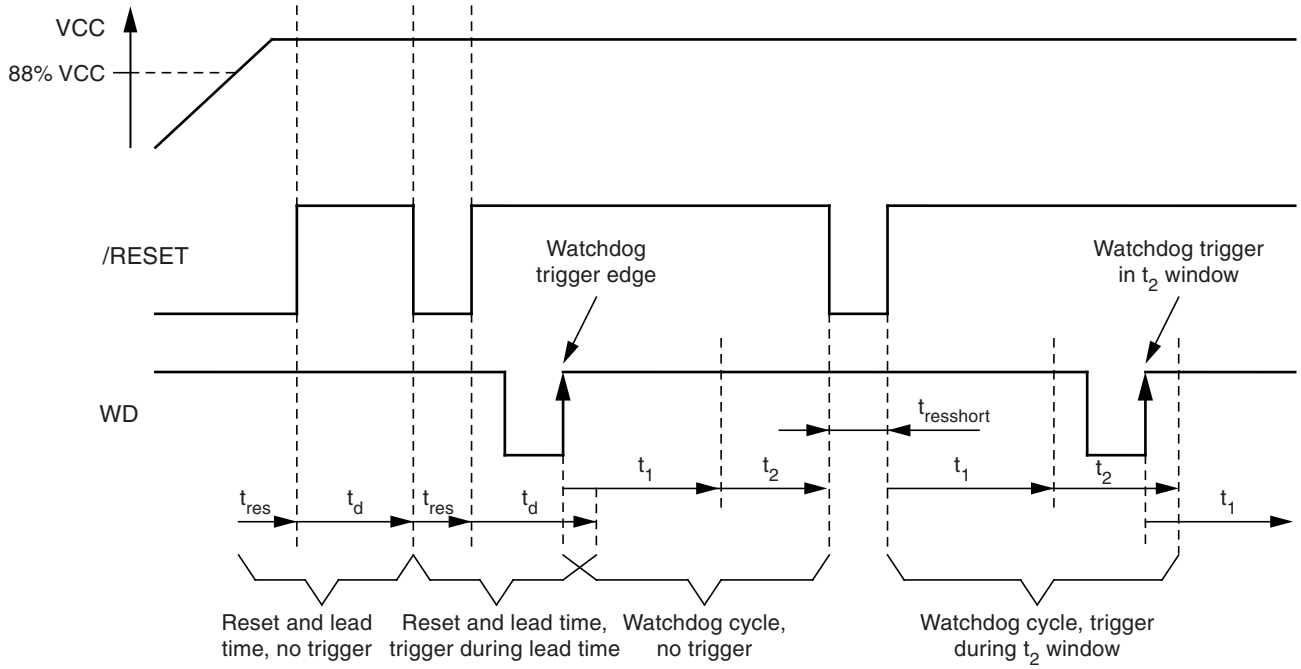


3.4 Reset and Watchdog Management

The watchdog timing is based on the trimmed internal watchdog oscillator. Its period time T_{OSC} is determined by the external resistor R_{WD}. A HIGH signal on WDD pin enables the watchdog function; a LOW signal disables it. Since WDD pin is equipped with an internal pull-up resistor the watchdog is enabled by default. In order to keep the current consumption as low as possible the watchdog is switched off during Sleep Mode.

The timing diagram in Figure 3-4 shows the watchdog and external reset timing.

Figure 3-4. Timing Diagram of the Watchdog in Conjunction with the /RESET Signal



After power-up of the VCC regulator (VCC output exceeds 88% of its nominal value) /RESET output stays LOW for the timeout period t_{res} (typical 10 ms). Subsequently /RESET output switches to HIGH. During the following time t_d (typical 500 ms) a rising edge at the input WD is expected otherwise another external reset will be triggered.

When the watchdog has been correctly triggered for the first time, normal watch-dog operation begins. A normal watchdog cycle consists of two time sections t_1 and t_2 followed by a short pulse for the time $t_{resshort}$ at /RESET if no valid trigger has been applied at pin WD during t_2. Rising edges on WD pin during t_1 also cause a short pulse on /RESET. Start for such a cycle is always the time of the last rising edge either on WD pin or on /RESET pin.

If the watchdog is disabled (WDD = LOW), only the initial reset for the time t_{res} after power-up will be generated.

Additional resets will be generated if the VCC output voltage drops below 80% of its nominal value.

The following example demonstrates how to calculate the timing scheme for valid watchdog trigger pulses, which the external microcontroller has to provide in order to prevent undesired resets.

Example:

Using an external resistor R_{WD} = 33 kΩ ±1% results in typical parameters as follows:

T_{OSC} = 12.32 µs

$t_1 = 980 \times T_{OSC}$ = 12.07 ms ±10%

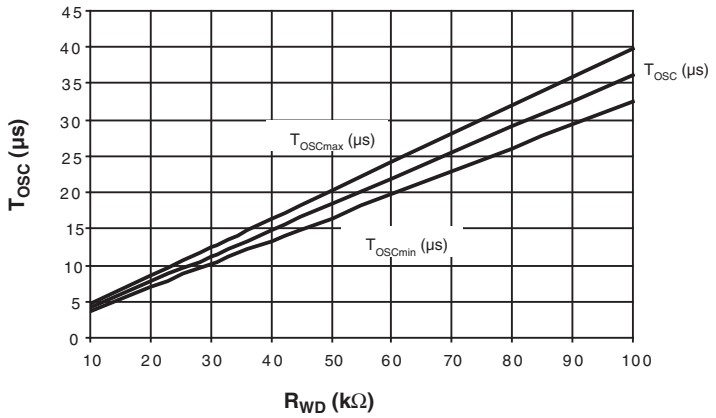
$t_2 = 780 \times T_{OSC}$ = 9.609 ms ±10%

$t_1 + t_2$ = 21.68 ms ±10%

Hence, the minimum time the external microcontroller has to wait before pin WD can be triggered is in worst case $t_{min} = 1.1 \times t_1$ = 13.28 ms. The maximum time for the watchdog trigger on WD pin is $t_{max} = 0.9 \times (t_1 + t_2)$ = 19.51 ms. Thus watchdog trigger input must remain within $t_{max} - t_{min}$ = 6.23 ms.

Other values can be set up by picking a different resistor value for R_{WD}. The dependency of T_{OSC} on the value of R_{WD} is shown in Figure 3-5.

Figure 3-5. T_{OSC} versus R_{WD}



3.5 Charge Pump

A charge pump has been implemented in order to provide sufficient voltage to operate the external high-side power-NMOS transistors and the VG regulator, which drives the low-side Power-NMOS transistors. The charge pump output voltage at CPOUT pin is controlled to settle typically about 15V above the voltage at pin PBAT. A built-in supervisor circuit checks if the output voltage is sufficient to operate the VG regulator and external Power-NMOS transistors. The output voltage is accepted as good when it rises above VCP_{CPGOOD}. A charge pump failure is flagged at DG2 if this minimum can not be reached or if the output voltage drops below the lower threshold of VCP_{CPGOOD} due to overloading.

The two shuffle capacitors should have the same value. The value of the reservoir capacitor should be at least twice the value of one shuffle capacitor. Two external shuffle capacitors and an external reservoir capacitor have to be provided. The typical values for the two shuffle capacitor is 100F, and for the reservoir capacitor is 470 nF. All capacitors should be ceramic. It is advisable to pick a reservoir capacitor with twice or three-times the size of the two equally-sized shuffle capacitors. The greater the capacitors, the greater the output current capability.

3.6 VG Regulator

The VG regulator provides a stable voltage to supply the low-side gate drivers and to deliver sufficient voltage for the external low-side Power-NMOS transistors. Typically the output voltage is 12V. In order to guarantee reliable operation even with a low battery voltage, the VG regulator is supplied by the charge pump output. For stability, an external ceramic capacitor of typically 470 nF has to be provided. There is no internal supervision of the VG output voltage.

3.7 Output Drivers and Control Inputs IL1-IL3, IH1-IH3

This IC offers six push-pull output drivers for the external low-side and high-side power-NMOS transistors. To guarantee reliable operation, the low-side drivers are supplied by the VG regulator while the high-side drivers are supplied directly by the charge pump. All drivers are designed to operate at switching frequencies in the range of DC up to 50 kHz. The maximum gate charge that can be delivered to each external Power-NMOS transistor at 50 kHz is 100 nC.

The output drivers are directly controlled by the digital input pins IL1 to IL3 and IH1 to IH3 (see Table 3-1). All pins are equipped with an internal pull-down resistor. To operate the output drivers properly the following requirements have to be fulfilled:

1. Device is in Active Mode.
2. In case of watchdog is enabled, at least one valid watchdog trigger has been accepted.
3. The voltage at pin PBAT lies within its operation range. Neither undervoltage nor overvoltage is present.
4. The charge pump output voltage has been accepted as good, thus it exceeded VCP_{CPGOOD}.
5. No overtemperature shutdown has occurred.

If a short circuit is detected by one of the sense inputs S1 to S3, the output drivers will be switched off after a debounce time of 6 µs and the output DG1 will be flagged (see also Section 3.8 “Short Circuit Detection” on page 11). The output drivers will be enabled again and DG1 will be cleared with a rising edge at one of the control inputs (IL1 to IL3, IH1 to IH3).

Additional logic prevents short circuits due to switching on one power-NMOS transistor while the opposite one in the same branch is switched on already.

Table 3-1. Status of the Output Drivers Depending on the Control Inputs

Mode	Control Inputs IL[1..3]	Control Inputs IH[1..3]	Driver Stage for External Power MOS L[1..3], H[1..3]	Comments
Sleep	X	X	OFF	Sleep Mode
Active	0	0	OFF	
Active	1	0	L[1..3] ON, H[1..3] OFF	
Active	0	1	H[1..3] ON, L[1..3] OFF	
Active	1	1	OFF	Shoot-through protection

3.8 Short Circuit Detection

Short circuits in the motor bridge circuitry are sensed by S1 to S3 inputs. Internal comparators monitor the voltage differences between the drain and the source terminals of the external power-NMOS transistors. If one transistor switches on and the voltage drop from its drain to source stays higher than the threshold V_{SC} (typical 4V) for a longer time than t_{SC} (typically 6 µs), a short circuit in this branch is detected. In this case, all output drivers are switched off immediately and DG1 pin will be set to HIGH. With a rising edge at any of the pins IL1 to IL3 or IH1 to IH3, the diagnostic output DG1will be reset and the drivers can be switched on again.

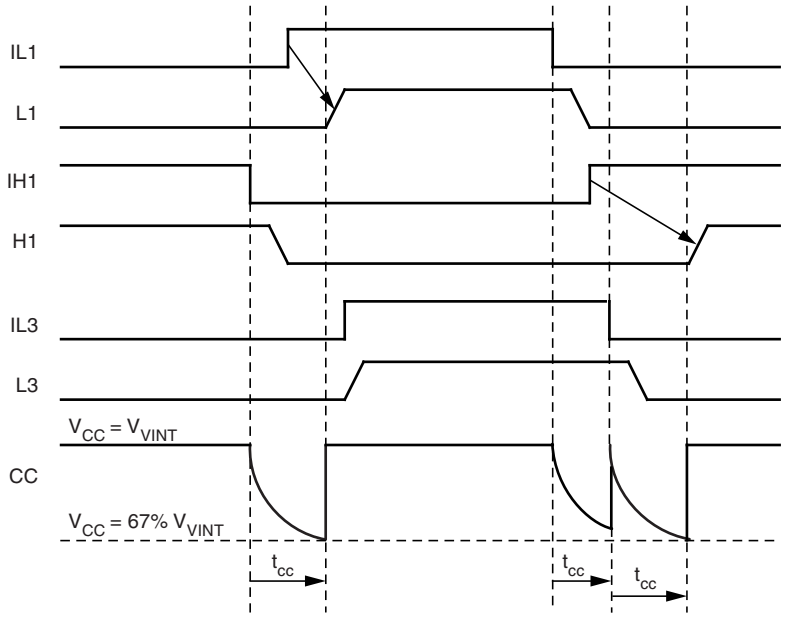
3.9 Cross Conduction Timer

In order to prevent damage of the motor bridge due to peak currents a non-overlapping phase for switching the power-NMOS transistors is mandatory. Therefore, a cross conduction timer has been implemented to prevent switching on any output driver for a time t_{CC} after any other driver has been switched off. This also accounts for toggling any other driver after a short circuit was detected. An external RC parallel combination defines the value for t_{CC} and can be estimated as follows:

$t_{CC} = K_{CC} \times R_{CC}$ [kΩ] $\times C_{CC}$ [nF], K_{CC} is specified in Section 8. “Electrical Characteristics” on page 15.

The RC combination is connected between CC and GND pins. When one of the drivers has been switched off the RC combination is charged to 5V (VINT) and discharged with its time constant. Any low to high transition at the control inputs will be masked out at the driver outputs until the voltage at CC pin drops below 67% of its initial value (VINT). The timer will be re-triggered at any time by any falling edge at the control inputs. This is shown in the following figure.

Figure 3-6. Timing Scheme of the Cross Conduction Timer



At least 5 kΩ minimum and 5 nF at maximum should be used as values for the RC combination. 10 kΩ is recommended. If the non-overlapping phase is controlled by the external microcontroller, it is possible to do without the external capacitor. The minimum time t_{CC} is defined by the parasitic capacitance at CC pin.

3.10 Diagnostic Outputs D1 - D3

As mentioned in the sections above, the diagnostic outputs DG1 to DG3 are used to signal failures. This is summarized in the following table.

Table 3-2. Status of the Diagnostic Outputs (Normal Operation)

Device Status					Diagnostic Outputs			Comments
CPOK	OT1	OV	UV	SC	DG1	DG2	DG3	
0	X	X	X	X	–	1	–	Charge pump failure
X	1	X	X	X	–	–	1	Overtemperature prewarning
X	X	1	X	X	–	1	–	Overvoltage
X	X	X	1	X	–	1	–	Undervoltage
X	X	X	X	1	1	–	–	Short circuit

Note: X represents: no effect)
OT1: overtemperature warning
OV: overvoltage of PBAT
UV: undervoltage of PBAT
SC: short circuit
CPOK: charge pump OK

In order to differentiate between LIN and EN2 wake-up, DG1 output will be set to LOW or HIGH respectively. LOW indicates wake-up by LIN, HIGH indicates wake-up by EN2. DG1 output will be cleared by the first valid watchdog trigger after wake-up or by the first rising edge at one of the control inputs (IL1 to IL3 and IH1 toIH3) if the watchdog is disabled.

Table 3-3. Indicating Wake-up Source

Diagnostic Outputs			Wake-up Source
DG1	DG2	DG3	
1	–	–	EN2
0	–	–	LIN

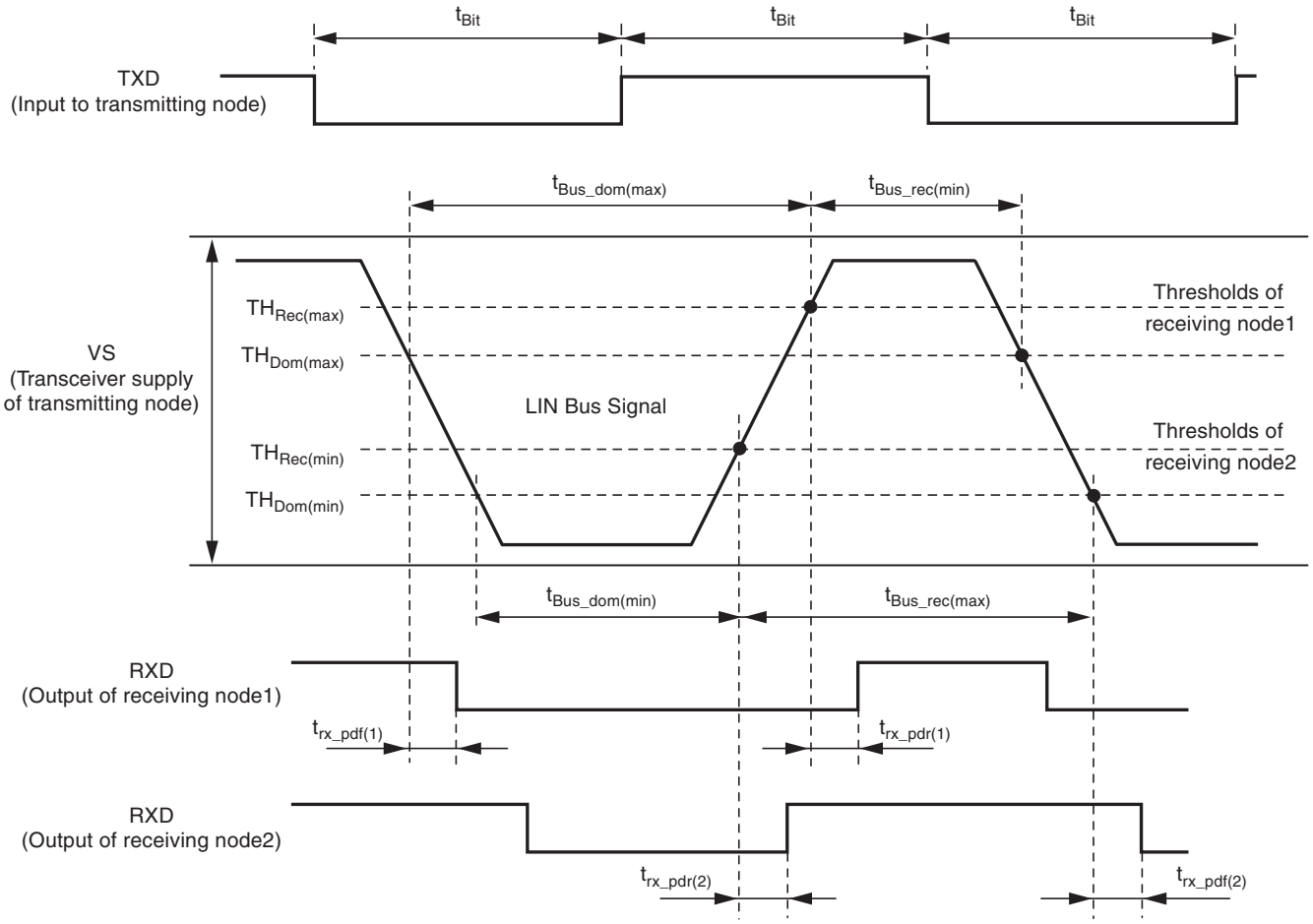
3.11 LIN Transceiver

ATA6833 and ATA6834 include a fully integrated LIN transceiver complying with LIN specification 2.1 and SAEJ2602 2. The transceiver consists of a low-side driver with slew rate control, wave shaping, current limiting, and a high voltage comparator followed by a debouncing unit in the receiver.

During transmission, the data applied at pin TXD will be transferred to the bus driver to generate a bus signal on LIN pin. TXD input has an internal pull-up resistor.

To minimize the electromagnetic emission of the bus line, the bus driver has a built-in slew rate control and wave-shaping unit. The transmission will be aborted by a thermal shutdown or by a transition to Sleep Mode.

Figure 3-7. Definition of Bus Timing Parameters



The recessive BUS level is generated from the integrated 30 kΩ pull-up resistor in series with an active diode. This diode protects against reverse currents on the bus line in case of a voltage difference between the bus line and VSUP ($V_{BUS} > V_{SUP}$). No additional termination resistor is necessary to use the IC as a LIN slave. If this IC is used as a LIN master, the LIN pin is terminated by an external 1 kΩ resistor in series with a diode to VBAT.

As PWM communication directly over the LIN transceiver in both directions is possible, there is no TXD timeout feature implemented in the LIN transceiver.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are referenced to pin GND. [xxx] Values for the ATA6834.

Parameters	Pin	Symbol	Min.	Max.	Unit
Input voltage	PGND	V_{PGND}	–0.3	+0.3	V
Negative input current	VBAT	IVBAT	TBD	TBD	mA
Negative input current	PBAT	IPBAT	TBD	TBD	mA
Supply voltage	VBAT	V_{VBAT}	–0.3	+40 (500 ms)	V
Supply voltage	PBAT	V_{PBAT}	–0.3	+40 (500 ms)	V
Logic output voltage	/RESET, DG1, DG2, DG3, RXD	$V_{/RESET}$, V_{DG1}, V_{DG2}, V_{DG3}, V_{RXD}	–0.3	V_{VCC} + 0.3	V
Logic input voltage	IL1-3, IH1-3, WD, WDD, EN1, TXD	V_{IL1-3}, V_{IH1-3}, V_{WD}, V_{EN1}, V_{TXD}	–0.3	V_{VCC} + 0.3	V
Output voltage	VINT, VCC	V_{INT}, V_{VVCC}	–0.3	+5.5	V
Analog input voltage	RWD, CC	V_{RWD}	–0.3	V_{VCC} + 0.3	V
Digital input voltage	EN2	V_{EN2}	–0.3	V_{VBAT} + 0.3	V
Digital input voltage	VMODE	V_{VMODE}	–0.3	V_{VINT} + 0.3	V
Output voltage	VG	V_{VG}	–0.3	+16	V
Input voltage	LIN	V_{VLIN}	–27	V_{VBAT} + 2	V
Output voltage	S1, S2, S3	V_{S1}, V_{S2}, V_{S3}	–6	+30	V
Output voltage	L1, L2, L3	V_{L1}, V_{L2}, V_{L3}	V_{PGND} – 0.3	V_{VG} + 0.3	V
Output voltage	H1, H2, L3	V_{H1}, V_{H2}, V_{H3}	$V_{S1, 2, 3}$ – 1	$V_{S1, 2, 3}$ + 16	V
Charge pump	CPLO1, 2	V_{CPLO1}, V_{CPLO2}	–0.3	V_{PBAT} + 0.3	V
Charge pump	CPHI1, 2	V_{CPHO1}, V_{CPHO2}	–0.3	V_{CPOUT} + 0.3	V
Output voltage	CPOUT	V_{CPOUT}	–0.3	+40	V
Output voltage	VBATSW	V_{VBATSW}	–0.3	V_{VBAT} + 0.3	V
Storage temperature		$T_{Storage}$	–55	+150	°C

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction to heat slug	R_{thjc}	< 5	K/W
Thermal resistance junction to ambient when heat slug is soldered to PCB	R_{thja}	25	K/W

6. Operating Range

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied unless otherwise stated explicitly. [xxx] Values for the ATA6834

Parameters	Symbol	Min	Max	Unit
Operating supply voltage(1)	V_{VBAT}	5.5	V_{THOV}(4)	V
Operating supply voltage(2)	V_{VBAT}	4.3	5.5	V
Operating supply voltage(3) (t = 500 ms)	V_{VBAT}	V_{THOV}(4)	40	V
Ambient temperature range	T_A	–40	+150	°C
Junction temperature range	T_J	–40	+150 (200)	°C

Notes: 1. Full functionality
2. Output drivers are switched off, extended range for parameters for voltage regulators
3. Output drivers and charge pump are switched off
4. Voltages higher V_{THOV} for maximum 500 ms

7. Noise and Surge Immunity

Parameters	Standard and Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Conducted disturbances	CISP25	Level 5
ESD (Human Body Model)	ESD S 5.1	±2 kV
ESD (Human Body Model)	DIN EN61000-4-2, Pin LIN, VBAT, PBAT to GND	±6 kV
Latch-up immunity	JESD78, AEL-Q100 (004)	Class II, level A

Note: 1. Test pulse 5: $V_{bat\ max}$ = 40V

8. Electrical Characteristics

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply and Supervisor Functions**								
1.1	Current consumption V_{VBAT}	V_{VBAT} = 13.5V(1)	VBAT	I_{VBAT}			7	mA	A
1.3	Current consumption V_{VBAT} in Standby Mode	V_{VBAT} = 13.5V	VBAT	I_{VBAT}			65	µA	A
1.4	Current consumption V_{VBAT} in Standby Mode	V_{PBAT} = 13.5V	PBAT	I_{VPBAT}			TBD	µA	A
1.5	Internal power supply	V_{VBAT} > 7V	VINT	V_{VINT}	4.7	5.0	5.3	V	A
1.6	Overvoltage threshold		PBAT	V_{THOV}	19.8		22.3	V	A
1.7	Overvoltage threshold hysteresis		PBAT	V_{TOVhys}	1		1.5	V	A
1.8	Undervoltage threshold		PBAT	V_{THUV}	5.0		5.5	V	A
1.9	Undervoltage threshold hysteresis		PBAT	V_{TUVhys}	0.2		0.4	V	A
1.10	R_{DSON} VBAT-Switch switch	V_{VBAT} = 13.5V, I_{VBATSW} = –15 mA	VBATSW	R_{ON_VBATSW}			100	Ω	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.11	Thermal prewarning set			$T_{JPW\ set}$	120 (170)	145 (195)	170 (220)	°C	B
1.12	Thermal prewarning reset			$T_{JPW\ reset}$	105 (155)	130 (180)	155 (205)	°C	B
1.13	Thermal prewarning hysteresis			ΔT_{JPW}		15		°C	B
1.14	Thermal shutdown off			$T_{J\ switch\ off}$	150 (200)	175 (225)	200 (250)	°C	B
1.15	Thermal shutdown on			$T_{J\ switch\ on}$	135 (185)	160 (210)	185 (235)	°C	B
1.16	Thermal shutdown hysteresis			$\Delta T_{J\ switch\ off}$		15		°C	B
1.17	Ratio thermal shutdown off/thermal prewarning set			$T_{J\ switch\ off}$/ $T_{JPW\ set}$	1.05	1.15			B
1.18	Ratio thermal shutdown on/thermal prewarning reset			$T_{J\ switch\ on}$/ $T_{JPW\ reset}$	1.05	1.15			B
2	**5V/3.3V Regulator**								
2.1	Regulated output voltage	$V_{MODE} = V_{INT}$, 7V < V_{BAT} < 40V V_{MODE} = GND, 5.5V < V_{BAT} < 40V I_{Load} = 0 to 100 mA	V_{CC}	V_{VCC}	4.85 3.20		5.15 3.40	V	A
2.2	Regulated output voltage	$V_{MODE} = V_{INT}$, 7V < V_{BAT} < 40V V_{MODE} = GND, 5.5V < V_{BAT} < 40V I_{Load} = 0 to 80 mA 150°C < T_J < 200°C	V_{CC}	V_{VCC}	4.85 3.20		5.15 3.40	V	A
2.3	Regulated output voltage	$V_{MODE} = V_{INT}$, 5.5V < V_{BAT} < 7V V_{MODE} = GND, 5V < V_{BAT} < 5.5V I_{Load} = 0 to 60 mA	V_{CC}	V_{VCC}	4.50 2.97		5.15 3.40	V	A
2.4	Regulated output voltage	$V_{MODE} = V_{INT}$, 5.5V < V_{BAT} < 7V V_{MODE} = GND, 5V < V_{BAT} < 5.5V I_{Load} = 0 to 50 mA 150°C < T_J < 200°C	V_{CC}	V_{VCC}	4.50 2.97		5.15 3.40	V	A
2.5	Line regulation	$V_{MODE} = V_{INT}$, 7V < V_{BAT} < 40V V_{MODE} = GND, 5.5V < V_{BAT} < 40V I_{Load} = 50 mA, –40°C < T_J < 150°C	V_{CC}				50 50	mV	A
2.6	Load regulation	$V_{MODE} = V_{INT}$, V_{BAT} > 7V V_{MODE} = GND, V_{BAT} > 5.5V I_{Load} = 0 to 100 mA I_{Load} = 0 to 80 mA, 150°C < T_J < 200°C	V_{CC}				50 50	mV	A
2.7	Output current limit	$V_{MODE} = V_{INT}$, V_{BAT} > 7V V_{MODE} = GND, V_{BAT} > 5.5V I_{Load} @ RESET	V_{CC}	I_{OS1}	100 100		320 320	mA	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.8	Output current limit	V_{MODE} = V_{INT}, V_{BAT} > 7V V_{MODE} = GND, V_{BAT} > 5.5V I_{Load} @ RESET, 150°C < T_J < 200°C	VCC	I_{OS1}	70 70		320 320	mA	C
2.12	HIGH threshold VMODE			$V_{VMODE\ H}$			4.0	V	A
2.13	LOW threshold VMODE			$V_{VMODE\ L}$	0.7			V	A
3	**Reset and Watchdog**								
3.1	V_{CC} threshold voltage level for /RESET	VMODE = VINT (VMODE = GND)		V_{tHRESH}	4.1 (2.7)		4.7 (3.0)	V	A
3.2	Hysteresis of /RESET level			HYS_{RESth}		0.2		V	A
3.3	Length of pulse at /RESET			t_{res}	8		12	ms	A
3.4	Length of short pulse at /RESET			$t_{resshort}$	1.8		2.2	ms	A
3.5	Wait for the first WD trigger			t_d	400		600	ms	A
3.6	Time for VCC < V_{tHRESL} before activating /RESET			$t_{delayRESL}$			2	µs	C
3.8	Watchdog oscillator period	R_{RWD} = 33 kΩ		T_{OSC}	11.09		13.55	µs	A
3.12	Close window			t1		980 × T_{OSC}			A
3.13	Open window			t2		780 × T_{OSC}			A
3.14	Output low-level at pin /RESET	I_{OLRES} = 1 mA		V_{OLRES}			0.4	V	A
3.15	Internal pull-up resistor at pin /RESET			R_{PURES}	5	10	15	kΩ	D
4	**LIN Transceiver**								
4.1	Low-level output current	Normal mode; V_{LIN} = 0V, V_{RXD} = 0.4V		IL_{RXD}	2			mA	D
4.2	High-level output current	Normal mode; V_{LIN} = V_{BAT} V_{RXD} = V_{CC} – 0.4V		IH_{RXD}			–2	mA	D
4.3	Driver recessive output voltage	V_{TXD} = V_{CC}; I_{LIN} = 0 mA		V_{BUSrec}	0.9 × VBAT			V	A
4.4	Driver dominant voltage $V_{BUSdom_DRV_LoSUP}$	V_{VBAT} = 7.3V R_{load} = 500Ω		$V_{_LoSUP}$			1.2	V	A
4.5	Driver dominant voltage $V_{BUSdom_DRV_HiSUP}$	V_{VBAT} = 18V R_{load} = 500Ω		$V_{_HiSUP}$			2	V	A
4.6	Driver dominant voltage $V_{BUSdom_DRV_LoSUP}$	V_{VBAT} = 7.3V R_{load} = 1000Ω		$V_{_LoSUP_1k}$	0.6			V	A
4.7	Driver dominant voltage $V_{BUSdom_DRV_HiSUP}$	V_{VBAT} = 18V R_{load} = 1000Ω		$V_{_HiSUP_1k_}$	0.8			V	A
4.8	Pull up resistor to VS	serial diode required		R_{LIN}	20		47	kΩ	A
4.9	Current limitation	V_{BUS} = V_{BAT_max}		I_{BUS_LIM}	50		200	mA	A

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8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.10	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V V_{BAT} = 12V		$I_{BUS_PAS_dom}$	–1			mA	A
4.11	Leakage current LIN recessive	Driver off 8V < V_{BAT} < 18V 8V < V_{BUS} < 18V V_{BUS} = V_{BAT}		$I_{BUS_PAS_rec}$			20	µA	A
4.12	Leakage current at ground loss Control unit disconnected from ground Loss of local ground must not affect communication in the residual network	GND_{Device} = VS V_{BAT} = 12V 0V < V_{BUS} < 18V		$I_{BUS_NO_gnd}$	–1		+1	mA	A
4.13	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition	V_{BAT} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V		I_{BUS}			100	µA	A
4.14	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2		V_{BUS_CNT}	0.475 × V_{VBAT}	0.5 × V_{VBAT}	0.525 × V_{VBAT}	V	A
4.15	Receiver dominant state	V_{EN} = 5V		V_{BUSdom}			0.4 × V_{VBAT}	V	A
4.16	Receiver recessive state	V_{EN} = 5V		V_{BUSrec}	0.6 × V_{VBAT}			V	A
4.17	Receiver input hysteresis	V_{HYS} = V_{th_rec} – V_{th_dom}		V_{BUShys}			0.175 × V_{VBAT}	V	A
4.18	Duty cycle 1	7V < V_{VBAT} < 18V $TH_{rec(max)}$ = 0.744 × V_{VBAT} $TH_{Dom(max)}$ = 0.581 × V_{VBAT} t_{Bit} = 50 µs D1 = $t_{Bus_rec(min)}$/(2 × t_{Bit}) Load1: 1 nF + 1 kΩ Load2: 10 nF + 500Ω		D1	0.396				A
4.19	Duty cycle 2	7V < V_{VBAT} < 18V $TH_{rec(min)}$ = 0.422 × V_{VBAT} $TH_{Dom(min)}$ = 0.284 × V_{VBAT} t_{Bit} = 50 µs D2 = $t_{Bus_rec(max)}$/(2×t_{Bit}) Load1: 1 nF + 1 kΩ Load2: 10 nF + 500Ω		D2			0.581		A
4.20	Receiver propagation delay	7V < V_{VBAT} < 18V t_{rec_pd} = max(t_{rx_pdr}, t_{rx_pdf})		t_{rx_pd}			6	µs	A
4.21	Symmetry of receiver propagation delay rising edge minus falling edge	7V < V_{VBAT} < 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}		t_{rx_sym}	–2		+2	µs	

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.22	Dominant time for wake-up via LIN-bus	V_{LIN} = 0V		T_{BUS}	30	90	150	µs	A
5	**Control Inputs EN1, IL1-3, IH1-3, WD, TX, WDD**								
5.1	Input low-level threshold			V_{IL}			0.3 × V_{VCC}	V	A
5.2	Input high-level threshold			V_{IH}	0.7 × V_{VCC}			V	A
5.3	Hysteresis			HYS	0.3				C
5.4	Pull-down resistor	EN1, IL1-3, IH1-3, WD		R_{PD}	25	50	100	kΩ	A
5.5	Pull-up resistor	TXD, WDD		R_{PU}	25	50	100	kΩ	A
5.7	Debounce time EN1			$t_{gotosleep}$	9	10	11	µs	A
6	**Charge Pump**								
6.1	Charge pump voltage	V_{VBAT} > 7V $I_{LoadCPOUT}$ = 0A I_{LoadVG} = 0A $C_{CP1,2}$ = 47 nF C_{CPOUT} = 220 nF	CPOUT	V_{CPOUT}	V_{VBAT} + 11V		V_{VBAT} + 18	V	A
6.2	Charge pump voltage	V_{VBAT} > 7V $I_{LoadCPOUT}$ = 7.5 mA, I_{LoadVG} = 0A $C_{CP1,2}$ = 47 nF C_{CPOUT} = 220 nF	CPOUT	V_{CPOUT}	V_{VBAT} +10V			V	A
6.3	Period charge pump oscillator			T_{CP}		2.5		µs	B
6.4	Charge pump output voltage for active drivers		CPOUT	VCP_{CPGOOD}	TBD	7.5	TBD	V	A
7	**VG Regulator**								
7.1	VG Regulator Output Voltage	V_{BAT} = 13.5V V_{CPOUT} = 20V I_{LoadVG} = 7.5 mA	VG	V_{VG}	11	12.5	14	V	A
7.2	VG Regulator Line Regulation	V_{BAT} = 13.5V V_{CPOUT1} = 20V, V_{CPOUT2} = 35V I_{LoadVG} = 7.5 mA	VG	ΔV_{VG_Line}			100	mV	A
7.3	VG Regulator Load Regulation	V_{BAT} = 13.5V V_{CPOUT} = 25V $I_{LoadVG1}$ = 1 mA, $I_{LoadVG2}$ = 60 mA	VG	ΔV_{VG_Load}			100	mV	A
8	**H-bridge Driver**								
8.1	Low-side driver HIGH output voltage			V_{LxH}			V_{VG}	V	D
8.2	ON-resistance of sink stage of pins Lx	ILX = 100 mA		R_{DSON_LxL}			20	Ω	A
8.3	ON-resistance of source stage of pins Lx	ILX = 100 mA		R_{DSON_LxH}			20	Ω	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.4	Output peak current at pins Lx switched to LOW	V_{Lx} = 3V		I_{LxL}	–100			mA	D
8.5	Output peak current at pins Lx switched to HIGH	V_{Lx} = 3V		I_{LxH}			100	mA	D
8.6	Sink resistance between Lx and GND		Lx to GND	R_{Lxsink}	45	75	115	kΩ	A
8.7	ON-resistance of sink stage of pins Hx	V_{Sx} = 0V		R_{DSON_HxL}			20	Ω	A
8.8	ON-resistance of source stage of pins Hx	$V_{Sx} = V_{VBAT}$ I_{Hx} = 100 mA		R_{DSON_HxH}			20	Ω	A
8.9	Output peak current at pins Hx (switched from low to high	$V_{Hx} – V_{Sx}$ = 0V; V_{VBAT} = 7V – 20V C = 10 nF R = 1Ω		$I_{HxH,}$			–200	mA	C
8.10	Output peak current at pins Hx (switched from high to low)	$V_{Hx} – V_{Sx}$ = 10V; V_{VBAT} = 7 – 20V C = 10 nF R = 1Ω		I_{HxL}	200			mA	C
8.11	Output peak current at pins Hx (switched from low to high	V_{Lx} = 0V; V_{VBAT} = 7 – 20V C = 10 nF R = 1Ω		$I_{LxH,}$			–200	mA	C
8.12	Output peak current at pins Hx (switched from high to low)	V_{LX} = 10V; V_{VBAT} = 7 – 20V C = 10 nF R = 1Ω		I_{LxL}	200			mA	C
8.13	Output voltage low level pins Hx	V_{Sx} = 0V I_{Hx} = 1 mA		V_{HxL}			0.3	V	A
8.14	Output voltage high level pins Hx	I_{Hx} = –100 µA		$V_{HxHstat}$	V_{VCPOUT} – 1V		V_{VCPOUT}	V	A
8.15	Sink resistance between Hx and Sx			R_{Hxsink}	45	75	115	kΩ	A
8.16	Sink resistance between Sx and GND		Sx to GND	R_{Sxsink}		1		MΩ	D
	Dynamic Parameters								
8.17	Propagation delay time, low-side driver from high to low			t_{LxHL}			0.9	µs	A
8.18	Propagation delay time, low-side driver from low to high			t_{LxLH}			0.9	µs	A
8.19	Fall time low-side driver	V_{VBAT} = 13.5V C_{Gx} = 5 nF		t_{Lxf}			TBD	µs	A
8.20	Rise time low-side driver	V_{VBAT} = 13.5V C_{Gx} = 5 nF		t_{Lxr}			TBD	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

All parameters given are valid for 5.5V ≤ V_{VBAT} ≤ 18V and for –40°C ≤ T_J ≤ 150°C (200°C) unless stated otherwise. All values refer to PIN GND. [xxx] Values for the ATA6834.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.21	Propagation delay time, high-side driver from high to low			t_{HxHL}			0.9	µs	A
8.22	Propagation delay time, high-side driver from low to high			t_{HxLH}			0.9	µs	A
8.23	Fall time high-side driver	V_{VBAT} = 13.5V, C_{Gx} = 5 nF		t_{Hxf}			TBD	µs	A
8.24	Rise time high-side driver	V_{VBAT} = 13.5V, C_{Gx} = 5 nF		t_{Hxr}			TBD	µs	A
8.25	Short circuit detection voltage			V_{SC}	3.5	4	4.5	V	A
8.26	Short circuit detection time			t_{SC}	5.4	6	6.6	µs	A
	Cross Conduction Timer								
8.27	Cross conduction time constant			K_{CC}	TBD	0.41	TBD		B
9	**Input EN2**								
9.1	Input low level threshold			V_{IL}	2.3		3.6	V	A
9.2	Input high level threshold			V_{IH}	2.8		4.0	V	A
9.3	Hysteresis			HYS		0.47		V	C
9.4	Pull-down resistor			R_{PD}	50	100	200	kΩ	A
9.5	Debounce time			t_{db}	10	20	25	µs	A
10	**Diagnostic Outputs DG1, DG2, DG3**								
10.1	Low level output current	V_{DG} = 0.4V		IL	2			mA	A
10.2	High level output current	V_{DG} = VCC – 0.4V		IH			–2	mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

9. Application

This section describes the principal application for which the ATA6833/ATA6834 was designed.

Figure 9-1. Typical Application

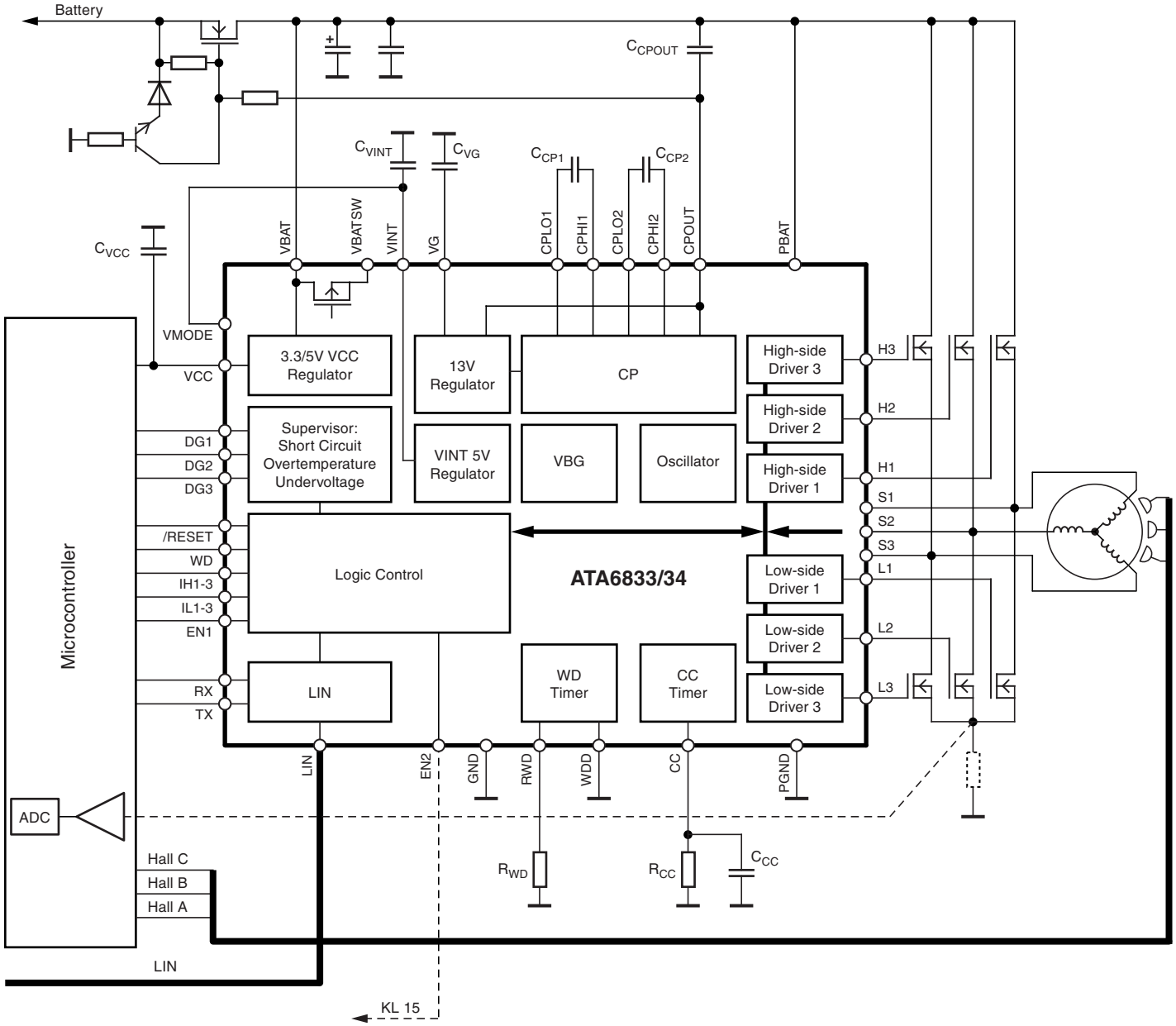


Table 9-1. Typical External Components

Component	Function	Min.	Typical	Max.
CVINT	Blocking capacitor at VINT	100 nF	220 nF/10V	470 nF
C_{VCC}	Blocking capacitor at VCC	1.5 µF		10 µF
ESL (C_{VCC})	Serial inductance to C_{VCC} including PCB	1 nH		20 nH
ESR (C_{VCC})	Serial resistance to C_{VCC} including PCB	2Ω		15Ω
CVG	Blocking capacitor at VG	220 nF	470 nF, 25V	1 µF
CCP1	Charge pump shuffle capacitor	47 nF	220 nF/25V	470 nF
CCP2	Charge pump shuffle capacitor	47 nF	220 nF/25V	470 nF
CCPOUT	Charge pump reservoir capacitor	220 nF	470 nF, 25V	1 µF
RRWD	Resistor defining internal bias currents for watchdog oscillator	10 kΩ	33 kΩ	91 kΩ
RCC	Cross conduction time definition resistor	5 kΩ	10 kΩ	
CCC	Cross conduction time definition capacitor		330 pF	5 nF

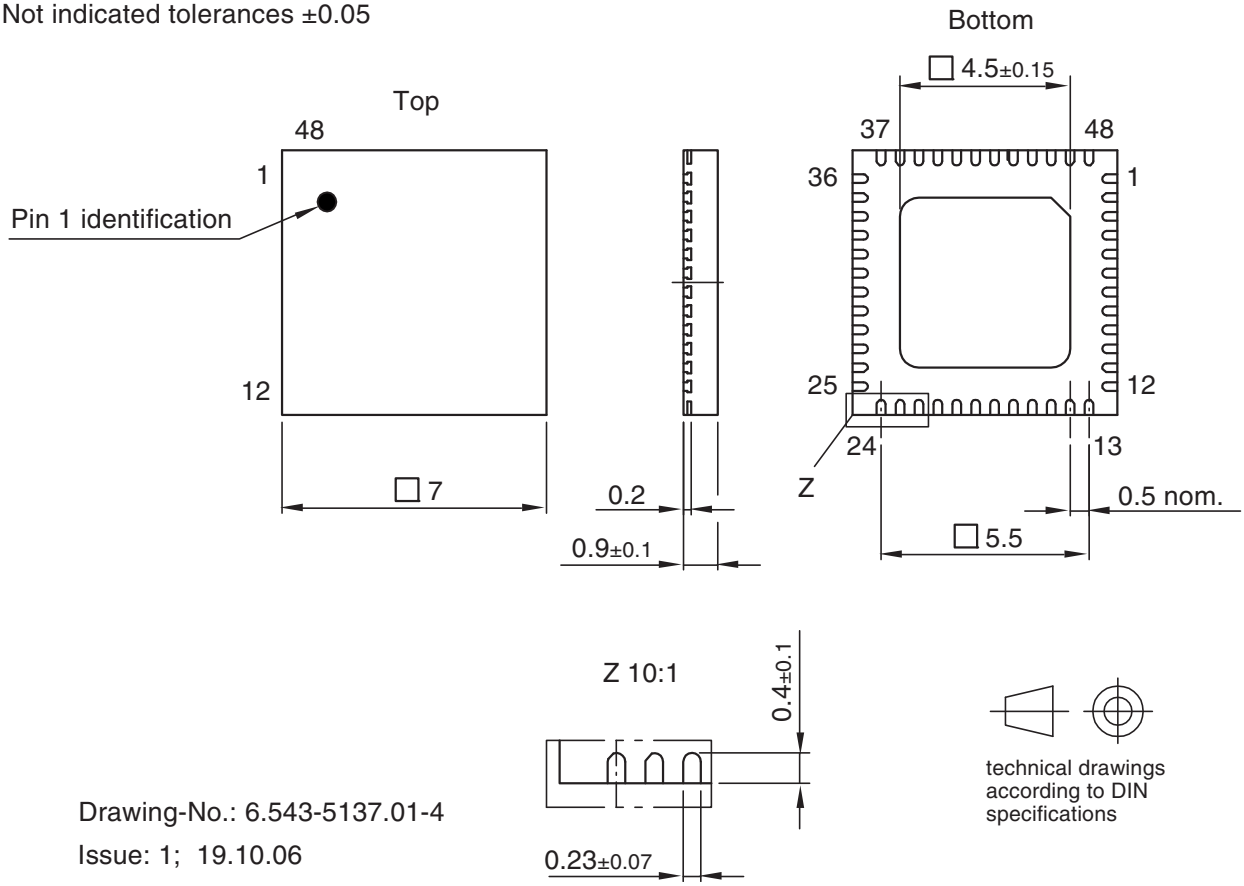
10. Ordering Information

Extended Type Number	Package	Remarks
ATA6833-PLQW	QFN48	
ATA6834-PLQW	QFN48	

11. Package Information

Package: VQFN_7 x 7_48L
Exposed pad 4.5 x 4.5
Dimensions in mm

Not indicated tolerances ±0.05



Drawing-No.: 6.543-5137.01-4

Issue: 1; 19.10.06

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9122B-AUTO-10/08	• Put datasheet in the latest template • Section 8 “Electrical Characteristics” on pages 15 to 21 changed

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