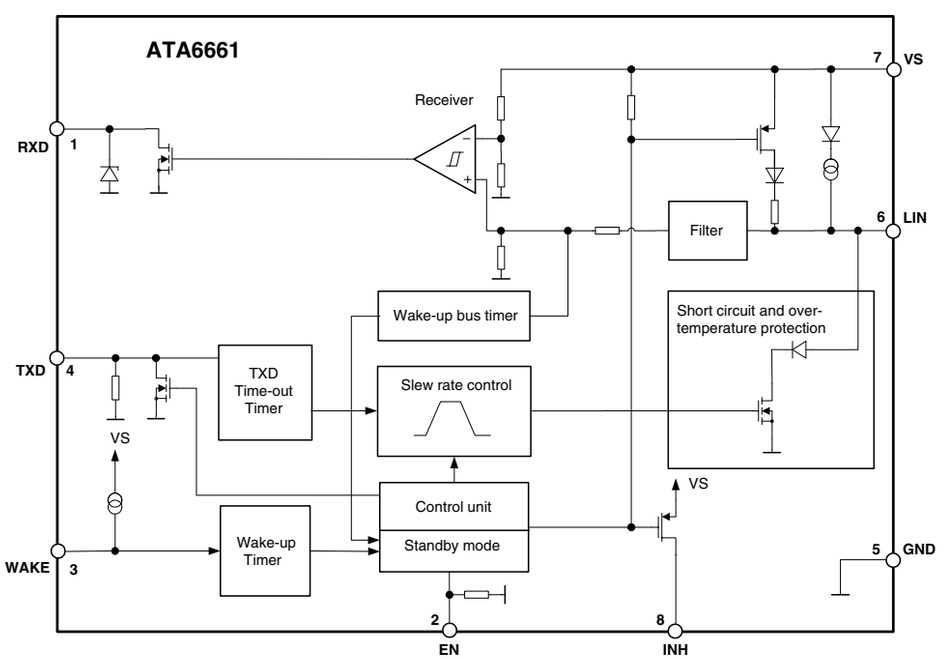
## Features

- **Operating Range from 5 V to 18 V**
- **Baud Rate up to 20 Kbaud**
- **Improved Slew Rate Control According to LIN Specification 2.0**
- **Fully Compatible with 3.3 V and 5 V Devices**
- **Dominant Time-out Function at Transmit Data (TXD)**
- **Normal and Sleep Mode**
- **Wake-up Capability via LIN Bus (90 µs Dominant)**
- **External Wake-up via WAKE Pin (130 µs Low Level)**
- **Control of External Voltage Regulator via INH Pin**
- **Very Low Standby Current During Sleep Mode (10 µA)**
- **60 V Load Dump Protection at LIN Pin (42-V Power Net)**
- **Wake-up Source Recognition**
- **Bus Pin Short-circuit Protected versus GND and Battery**
- **LIN Input Current <3 µA if $V_{BAT}$ Is Disconnected**
- **Overtemperature Protection**
- **High EMC Level**
- **Interference and Damage Protection According to ISO/CD 7637**
- **ESD HBM 6 kV at LIN Bus Pin and Supply VS Pin**

## Description

The ATA6661 is a fully integrated LIN transceiver according to the LIN specification 2.0. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, e.g., in convenience electronics. Improved slope control at the LIN bus ensures secure data communication up to 20 kBaud with an RC-oscillator for protocol handling. In order to comply with the 42-V power net requirements, the bus output is capable of withstanding high voltages. Sleep mode guarantees minimal current consumption.

**Figure 1.** Block Diagram



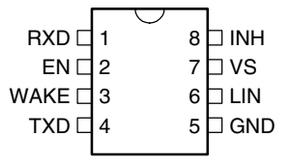

# LIN Transceiver

# ATA6661

Rev. 4729D–AUTO–10/04

## Pin Configuration

**Figure 2.** Pinning SO8




## Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1 | RXD | Receive data output (open drain) |
| 2 | EN | Enables normal mode, when the input is open or low, the device is in sleep mode |
| 3 | WAKE | High voltage input for local wake-up request |
| 4 | TXD | Transmit data input; active low output (strong pull-down) after a local wake-up request |
| 5 | GND | Ground |
| 6 | LIN | LIN bus line input/output |
| 7 | VS | Battery supply |
| 8 | INH | Battery related inhibit output for controlling an external voltage regulator; active high after a wake-up request |

## Functional Description

### Supply Pin ($V_S$)

Undervoltage detection is implemented to disable transmission if $V_S$ is falling to a value below 5 V to avoid false bus messages. After switching on $V_S$ the IC switches to pre-normal mode and INHIBIT is switched on. The supply current in sleep mode is typically 10 µA.

### Ground Pin (GND)

The ATA6661 is neutral on the LIN pin in case of a GND disconnection. It is able to handle a ground shift up to 3 V for $V_S$ > 9 V.

### Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.0 are implemented. The voltage range is from -27 V to +60 V. This pin exhibits no reverse current from the LIN bus to $V_S$, even in case of a GND shift or $V_{Batt}$ disconnection. The LIN receiver thresholds are compatible to the LIN protocol specification.The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled. The output has a short circuit limitation. This is a self adapting current limitation; i.e., during current limitation as the chip temperature increases so the current reduces.

### Input Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD is low to bring LIN low. If TXD is high, the LIN output transistor is turned off. In this case, the bus is in recessive mode via the internal pull-up resistor. The TXD pin is compatible to a 3.3 V and 5 V supply.

### TXD Dominant Time-out Function

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced low longer than $t_{dom}$ > 4 ms, the pin LIN will be switched off to recessive mode. To reset this mode switch TXD to high (>10 µs) before switching LIN to dominant again.

### Output Pin (RXD)

This pin reports to the microcontroller the state of the LIN bus. LIN high (recessive) is reported by a high level at RXD, LIN low (dominant) is reported by a low voltage at RXD. The output is an open drain, therefore, it is compatible to a 3.3 V or 5 V power supply. The AC characteristics are defined with a pull-up resistor of 5 kΩ to 5 V and a load capacitor of 20 pF. The output is short-current protected. In unpowered mode ($V_S$ = 0 V), RXD is switched off. For ESD protection a Zener diode is implemented with $V_Z$ = 6.1 V.

### Enable Input Pin (EN)

This pin controls the operation mode of the interface. If EN = 1, the interface is in normal mode, with the transmission path from TXD to LIN and from LIN to Rx both active. If EN = 0, the device is switched to sleep mode and no transmission is possible. In sleep mode, the LIN bus pin is connected to $V_S$ with a weak pull-up current source. The device can transmit only after being woken up (see “Inhibit Output Pin (INH)” on page 3).

During sleep mode the device is still supplied from the battery voltage. The supply current is typically 10 µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep mode in case the pin is disconnected.

### Inhibit Output Pin (INH)

This pin is used to control an external switchable voltage regulator having a wake-up input. The inhibit pin provides an internal switch towards pin $V_S$. If the device is in normal mode, the inhibit high-side switch is turned on and the external voltage regulator is activated. When the device is in sleep mode, the inhibit switch is turned off and disables the voltage regulator.

A wake-up event on the LIN bus or at pin WAKE will switch the INH pin to the $V_S$ level. After a system power-up ($V_S$ rises from zero), the pin INH switches automatically to the $V_S$ level. The $R_{DSon}$ of the highside output is <1 kΩ.

### Wake-up Input Pin (WAKE)

This pin is a high-voltage input used to wake-up the device from sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If you do not need a local wake-up in your application, connect pin WAKE directly to pin VS. A pull-up current source with typically -10 µA is implemented. The voltage threshold for a wake-up signal is 3 V below the VS voltage with an output current of typival -3 µA.

Wake-up events from sleep mode:

- LIN bus
- EN pin
- WAKE pin

Figure 3 on page 5, Figure 4 on page 6 and Figure 5 on page 6 show details of wake-up operations.

## Mode of Operation

1. Normal mode
   This is the normal transmitting and receiving mode. All features are available.
2. Sleep mode
   In this mode the transmission path is disabled and the device is in low power mode. Supply current from $V_{Batt}$ is typically 10 µA. A wake-up signal from the LIN bus or via pin WAKE will be detected and switches the device to pre-normal mode. If EN, then switches to high, normal mode is activated. Input debounce timers at pin WAKE ($T_{WAKE}$), LIN ($T_{BUS}$) and EN ($T_{sleep}$,$T_{nom}$) prevent unwanted wake-up events due to automotive transients or EMI. In sleep mode the INH pin is floating. The internal termination between pin LIN and pin $V_S$ is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typical 10 µA) between pin LIN and pin $V_S$ is present.
3. Pre-normal mode
   At system power-up, the device automatically switches to pre-normal mode. It switches the INH pin to a high state, to the $V_S$ level. The microcontroller of the application will then confirm the normal mode by setting the EN pin to high.

## Remote Wake-up via Dominant Bus State

A falling edge at pin LIN, followed by a dominant bus level maintained for a certain time period ($T_{BUS}$), results in a remote wake-up request. The device switches to pre-normal mode. Pin INH is activated (switches to $V_S$) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 4 on page 6). The voltage threshold for a wake-up signal is 3 V below the VS voltage with an output current of typival -3 µA.

## Local Wake-up via Pin WAKE

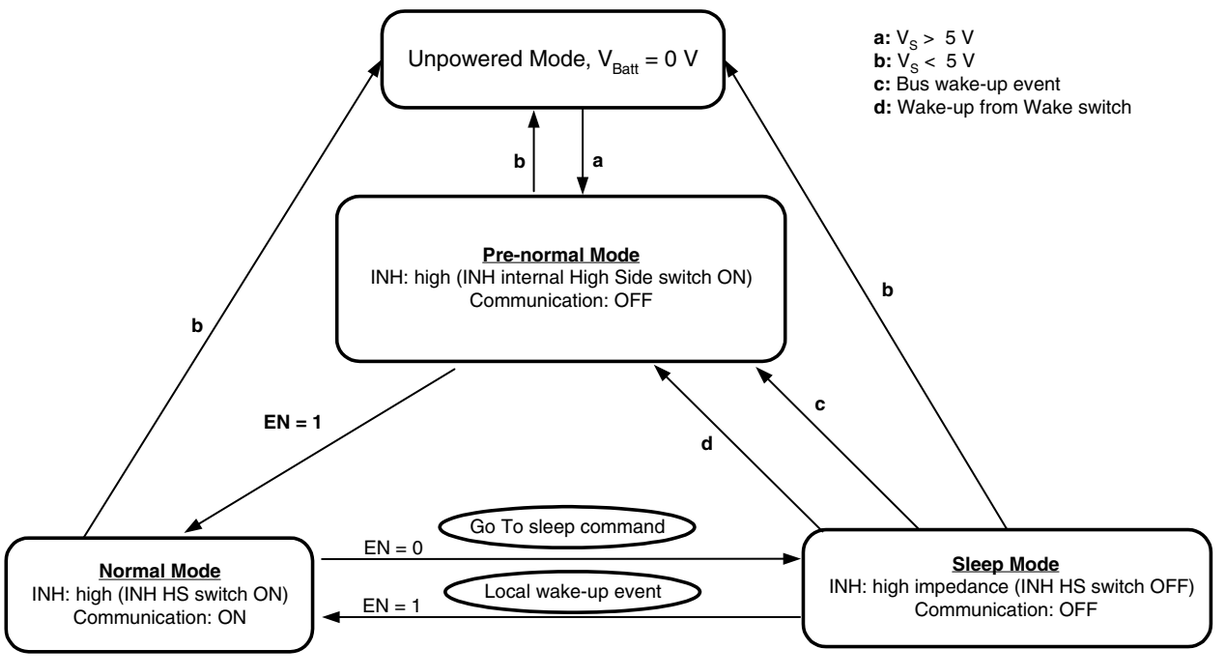
A falling edge at pin WAKE, followed by a low level maintained for a certain time period ($T_{WAKE}$), results in a local wake-up request. The extra long wake-up time ($T_{WAKE}$) ensures that no transient, according to ISO7637, creates a wake-up. The device switches to pre-normal mode. Pin INH is activated (switches to $V_S$) and the internal termination resistor is switched on. The local wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller and a strong pull-down at pin TXD (see Figure 5 on page 6).

## Wake-up Source Recognition

The device can distinguish between a local wake-up request (pin WAKE) and a remote wake-up request (dominant LIN bus). The wake-up source can be read on pin TXD in pre-normal mode. If an external pull-up resistor (typically 5 kΩ) on pin TXD to the power supply of the microcontroller has been added, a high level indicates a remote wake-up request (weak pull-down at pin TXD) and a low level indicates a local wake-up request (strong pull-down at pin TXD).

The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately, if the microcontroller sets pin EN to high (see Figure 4 on page 6 and Figure 5 on page 6).

**Figure 3.** Mode of Operation




## Fail-safe Features

- There are now reverse currents <3 µA at pin LIN during loss of $V_{BAT}$ or GND. Optimal behavior for bus systems where some slave modes supplied from battery or ignition.
- Pin EN provides pull-down resistor to force the transceiver into sleep mode if EN is disconnected.
- Pin RXD is set floating if $V_{BAT}$ is disconnected.
- Pin TXD provides a pull-down resistor to provide a static low if TXD is disconnected.
- The LIN output driver has a current limitation and if the junction temperature $T_j$ exceeds the thermal shut-down temperature $T_{off}$ the output driver switches off.
- The implemented hysteresis $T_{hys}$ enables the LIN output again after the temperature has been decreased.

**Figure 4.** LIN Wake-up Waveform Diagram

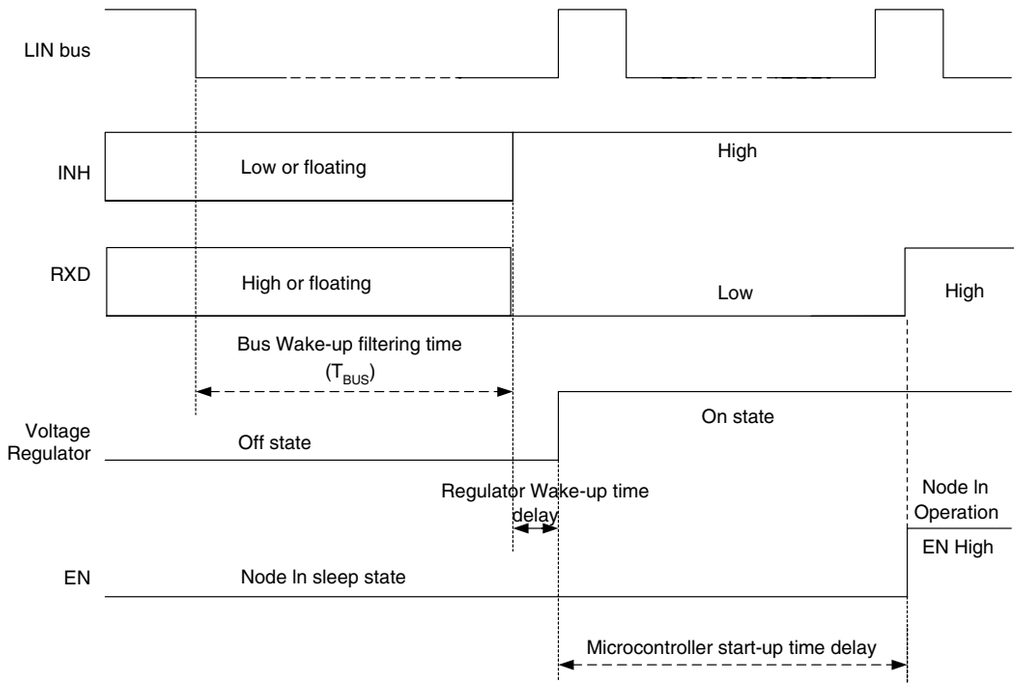
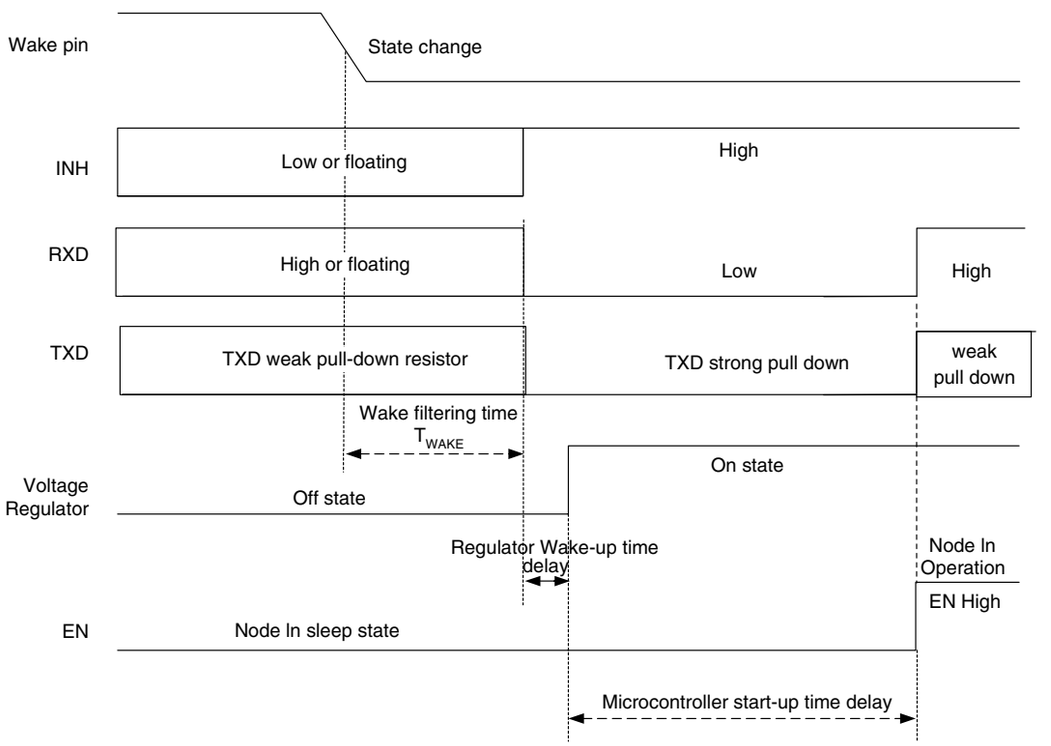



**Figure 5.** LIN Wake-up from Wake-up Switch



## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_S$<br>- Continuous supply voltage | | -0.3 | | +40 | V |
| Wake DC and transient voltage (with 33 kΩ serial resistor)<br>- Transient voltage due to ISO7637 (coupling 1 nF) | | -40<br>-150 | | +40<br>+100 | V<br>V |
| Logic pins (RXD, TXD, EN) | | -0.3 | | +6 | V |
| LIN<br>- DC voltage<br>- Transient voltage due to ISO7637 (coupling 1 nF) | | <br>-40<br>-150 | | <br>+60<br>+100 | <br>V<br>V |
| INH<br>- DC voltage | | <br>-0.3 | | <br>+40 | <br>V |
| ESD HBM (DIN EN 61000-4-2)<br>According LIN EMC Test Specification V1.3<br>- Pin VS, LIN<br>- Pin Wake (with 33 kΩ serial resistor) | | <br><br>-6000<br>-5000 | | <br><br>+6000<br>+5000 | <br><br>V<br>V |
| HBM ESD S5.1 - All pins | | -3000 | | +3000 | V |
| CDM ESD STM 5.3.1-1999 - All pins<br>FCDM ESD STM 5.3.1- All pins<br>MM JEDEC A115A - All pins | | -500<br>-1000<br>-200 | | +500<br>+1000<br>+200 | V<br>V<br>V |
| Junction temperature | $T_j$ | -40 | | +150 | °C |
| Storage temperature | $T_{stg}$ | -55 | | +150 | °C |
| Operating ambient temperature | $T_{amb}$ | -40 | | +125 | °C |
| Thermal shutdown | $T_{off}$ | 150 | 165 | 180 | °C |
| Thermal shutdown hysteresis | $T_{hys}$ | 5 | 10 | 20 | °C |

## Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Thermal resistance junction ambient | $R_{thJA}$ | 160 | K/W |

## Electrical Characteristics

5 V < $V_S$ < 18 V, $T_{amb}$ = -40°C to +125°C

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| **1** | **$V_S$ Pin** | | | | | | | | |
| 1.1 | Nominal DC voltage range | | 7 | $V_S$ | 5 | 13.5 | 18 | V | A |
| 1.2 | Supply current in sleep mode | Sleep mode<br>$V_{lin} > V_{Batt}$ - 0.5 V<br>$V_{Batt}$ < 14 V | 7 | $I_{VSstby}$ | | 10 | 20 | µA | A |
| 1.3 | Supply current in normal mode | Bus recessive | 7 | $I_{VSrec}$ | | 1.6 | 3 | mA | A |
| 1.4 | | Bus dominant<br>Total bus load > 500 Ω | 7 | $I_{VSdom}$ | | 1.6 | 3 | mA | A |
| 1.5 | $V_S$ undervoltage threshold | | | $V_{Sth}$ | 4 | 4.6 | 5 | V | A |
| 1.6 | $V_S$ undervoltage threshold hysteresis | | 7 | $V_{Sth_hys}$ | | 0.2 | | V | A |
| **2** | **RXD Output Pin (Open Drain)** | | | | | | | | |
| 2.1 | Low level input current | Normal mode<br>$V_{LIN}$ = 0 V, $V_{RXD}$ = 0.4 V | 1 | $I_{RXDL}$ | 2 | 5 | 8 | mA | A |
| 2.2 | RXD saturation voltage | 5 kΩ pull-up resistor to 5 V | 1 | $Vsat_{RXD}$ | | | 0.4 | V | A |
| 2.3 | High level leakage current | Normal mode<br>$V_{LIN}$ = $V_{BAT}$, $V_{RXD}$ = 5 V | 1 | $I_{RXDH}$ | -3 | | +3 | µA | A |
| 2.4 | ESD zener diode | $I_{RXD}$ = 100 µA | 1 | $VZ_{RXD}$ | 6.1 | | 8.6 | V | A |
| **3** | **TXD Input Pin** | | | | | | | | |
| 3.1 | Low level voltage input | | 4 | $V_{TXDL}$ | -0.3 | | +0.8 | V | A |
| 3.2 | High level voltage input | | 4 | $V_{TXDH}$ | 2 | | 7 | V | A |
| 3.3 | Pull-down resistor | $V_{TXD}$ = 5 V | 4 | $R_{TXD}$ | 125 | 250 | 600 | kΩ | A |
| 3.4 | Low level leakage current | $V_{TXD}$ = 0 V | 4 | $I_{TXD}$ | -3 | | +3 | µA | A |
| 3.5 | Low-level input current at local wake-up request | Pre-normal mode<br>$V_{LIN}$ = $V_{BAT}$; $V_{WAKE}$ = 0 V | 4 | $I_{TXDwake}$ | 2 | 5 | 8 | mA | A |
| **4** | **EN Input Pin** | | | | | | | | |
| 4.1 | Low level voltage input | | 2 | $V_{ENL}$ | -0.3 | | +0.8 | V | A |
| 4.2 | High level voltage input | | 2 | $V_{ENH}$ | 2 | | 7 | V | A |
| 4.3 | Pull-down resistor | $V_{EN}$ = 5 V | 2 | $R_{EN}$ | 125 | 250 | 600 | kΩ | A |
| 4.4 | Low level input current | $V_{EN}$ = 0 V | 2 | $I_{EN}$ | -3 | | +3 | µA | A |
| **5** | **INH Output Pin** | | | | | | | | |
| 5.1 | High level voltage | Normal mode<br>$I_{INH}$ = -200 µA | 8 | $V_{INHH}$ | $V_S$ - 0.8 | | $V_S$ | V | A |
| 5.2 | High level leakage current | Sleep mode<br>$V_{INH}$ = 27 V, $V_{Batt}$ = 27 V | 8 | $I_{INHL}$ | -3 | | +3 | µA | A |
| **6** | **WAKE Pin** | | | | | | | | |
| 6.1 | High level input voltage | | 3 | $V_{WAKEH}$ | $V_S$ - 1 V | | $V_S$ + 0.3 V | V | A |
| 6.2 | Low level input voltage | $I_{WAKE}$ = Typically -3 µA | 3 | $V_{WAKEL}$ | -27 V | | $V_S$ - 3 V | V | A |
| 6.3 | Wake pull-up current | $V_S$ < 27 V | 3 | $I_{WAKE}$ | -30 | -10 | | µA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## Electrical Characteristics (Continued)

5 V < $V_S$ < 18 V, $T_{amb}$ = -40°C to +125°C

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 6.4 | High level leakage current | $V_S$ = 27 V, $V_{WAKE}$ = 27 V | 3 | $I_{WAKE}$ | -5 | | +5 | µA | A |
| **7** | **LIN Bus Driver** | | | | | | | | |
| 7.1 | Driver recessive output voltage | $V_{TXD}$ = 0 V, $I_{LIN}$ = 0 mA | 6 | $V_{BUSrec}$ | 0.9 × $V_S$ | | $V_S$ | V | A |
| 7.2 | Driver dominant voltage $V_{BUSdom_DRV_LoSUP}$ | $V_{VS}$ = 7.3 V, $R_{load}$ = 500 Ω | 6 | $V_{_LoSUP}$ | | | 1.2 | V | A |
| 7.3 | Driver dominant voltage $V_{BUSdom_DRV_HiSUP}$ | $V_{VS}$ = 18 V, $R_{load}$ = 500 Ω | 6 | $V_{_HiSUP}$ | | | 2 | V | A |
| 7.4 | Driver dominant voltage $V_{BUSdom_DRV_LoSUP}$ | $V_{VS}$ = 7.3 V, $R_{load}$ = 1000 Ω | 6 | $V_{_LoSUP_1k}$ | 0.6 | | | V | A |
| 7.5 | Driver dominant voltage $V_{BUSdom_DRV_HiSUP}$ | $V_{VS}$ = 18 V, $R_{load}$ = 1000 Ω | 6 | $V_{_HiSUP_1k_}$ | 0.8 | | | V | A |
| 7.6 | Pull-up resistor to $V_S$ | The serial diode is mandatory | 6 | $R_{LIN}$ | 20 | 30 | 60 | kΩ | A |
| 7.7 | Self-adapting current limitation $V_{BUS}$ = $V_{BAT_max}$ | $T_j$ = 125°C<br>$T_j$ = 27°C<br>$T_j$ = -40°C | 6 | $I_{BUS_LIM}$ | 52<br>100<br>150 | | 110<br>170<br>230 | mA<br>mA<br>mA | A |
| 7.8 | Input leakage current at the receiver, inclusive pull-up resistor as specified | Input leakage current<br>Driver off<br>$V_{BUS}$ = 0 V, $V_{Batt}$ = 12 V | 6 | $I_{BUS_PAS_dom}$ | -1 | | | mA | A |
| 7.9 | Leakage current LIN recessive | Driver off<br>8 V < $V_{BAT}$ < 18 V<br>8 V < $V_{BUS}$ < 18 V<br>$V_{BUS} \geq V_{BAT}$ | 6 | $I_{BUS_PAS_rec}$ | | 15 | 20 | µA | A |
| 7.10 | Leakage current at ground loss, Control unit disconnected from ground,<br>Loss of local ground must not affect communication in the residual network | $GND_{Device}$ = $V_S$<br>$V_{BAT}$ =12 V<br>0 V < $V_{BUS}$ < 18 V | 6 | $I_{BUS_NO_gnd}$ | -10 | +0.5 | +10 | µA | A |
| 7.11 | Node has to sustain the current that can flow under this condition, bus must remain operational under this condition | $V_{BAT}$ disconnected<br>$V_{SUP_Device}$ = GND<br>0 V < $V_{BUS}$ < 18 V | 6 | $I_{BUS}$ | | 0.5 | 3 | µA | A |
| **8** | **LIN Bus Receiver** | | | | | | | | |
| 8.1 | Center of receiver threshold | $V_{BUS_CNT}$ = ($V_{th_dom}$ + $V_{th_rec}$)/2 | 6 | $V_{BUS_CNT}$ | 0.475 × $V_S$ | 0.5 × $V_S$ | 0.525 × $V_S$ | V | A |
| 8.2 | Receiver dominant state | $V_{EN}$ = 5 V | 6 | $V_{BUSdom}$ | -27 | | 0.4 × $V_S$ | V | A |
| 8.3 | Receiver recessive state | $V_{EN}$ = 5 V | 6 | $V_{BUSrec}$ | 0.6 × $V_S$ | | 40 | V | A |
| 8.4 | Receiver input hysteresis | $V_{HYS}$ = $V_{th_rec}$ - $V_{th_dom}$ | 6 | $V_{BUShys}$ | 0.028 × $V_S$ | 0.1 × $V_S$ | 0.175 × $V_S$ | V | A |
| 8.5 | Wake detection LIN<br>High level input voltage | | 6 | $V_{ZINH}$ | $V_S$ - 1 V | | $V_S$ + 0.3 V | V | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## Electrical Characteristics (Continued)

5 V < $V_S$ < 18 V, $T_{amb}$ = -40°C to +125°C

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 8.6 | Wake detection LIN<br>Low level input voltage | $I_{LIN}$ = Typically -3 µA | 6 | $V_{LINL}$ | -27 V | | $V_S$ -<br>3 V | V | A |
| 8.7 | LIN pull-up current | $V_S$ < 27 V | 6 | $I_{LIN}$ | -30 | -10 | | µA | A |
| **9** | **Internal Timers** | | | | | | | | |
| 9.1 | Dominant time for wake-up via LIN bus | $V_{LIN}$ = 0 V | 6 | $T_{BUS}$ | 30 | 90 | 150 | µs | A |
| 9.2 | Time of low pulse for wake-up via pin WAKE | $V_{WAKE}$ = 0 V | 3 | $T_{WAKE}$ | 60 | 130 | 200 | µs | A |
| 9.3 | Time delay for mode change from pre-normal mode to normal mode via pin EN | $V_{EN}$ = 5 V | 2 | $T_{norm}$ | 4 | 10 | 15 | µs | A |
| 9.4 | Time delay for mode change from normal mode into sleep mode via pin EN | $V_{EN}$ = 0 V | 2 | $T_{sleep}$ | 2 | 10 | 12 | µs | A |
| 9.5 | TXD dominant time out timer | $V_{TXD}$ = 0 V | 4 | $T_{dom}$ | 4 | 9 | 20 | ms | A |
| 9.6 | Power-up delay between $V_S$ = 5 V until INH switches to high | $V_{VS}$ = 5 V | | $T_{VS}$ | | | 200 | µs | A |
| **10** | **LIN Bus Driver (see Figure 6 on page 11)**<br>Bus load conditions: Load1 small 1 nF 1 kΩ, Load2 big 10 nF 500 Ω, $R_{RXD}$ = 5 kΩ, $C_{RXD}$ = 20 pF;<br>The following two rows specifies the timing parameters for proper operation at 20.0 kBit/s. | | | | | | | | |
| 10.1 | Duty cycle 1 | $TH_{Rec(max)} = 0.744 \times V_S$<br>$TH_{Dom(max)} = 0.581 \times V_S$<br>$V_S$ = 7.0 V to 18 V<br>$t_{Bit}$ = 50 µs<br>D1 = $t_{bus_rec(min)}/(2 \times t_{Bit})$ | | D1 | 0.396 | | | | A |
| 10.2 | Duty cycle 1 | $TH_{Rec(min)} = 0.422 \times V_S$<br>$TH_{Dom(min)} = 0.284 \times V_S$<br>$V_S$ = 7.0 V to 18 V<br>$t_{Bit}$ = 50 µs<br>D2 = $t_{bus_rec(max)}/(2 \times t_{Bit})$ | | D2 | | | 0.581 | | A |
| **11** | **Receiver Electrical AC Parameters of the LIN Physical Layer**<br>LIN receiver, RXD load conditions ($C_{RXD}$): 20 pF, $R_{pull-up}$ = 5 kΩ | | | | | | | | |
| 11.1 | Propagation delay of receiver (see Figure 6 on page 11) | $t_{rec_pd} = \max(t_{rx_pdr}, t_{rx_pdf})$ | | $t_{rx_pd}$ | | | 6 | µs | A |
| 11.2 | Symmetry of receiver propagation delay rising edge minus falling edge | $t_{rx_sym} = t_{rx_pdr} - t_{rx_pdf}$ | | $t_{rx_sym}$ | -2 | | 2 | µs | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

**Figure 6.** Definition of Bus Timing Parameter

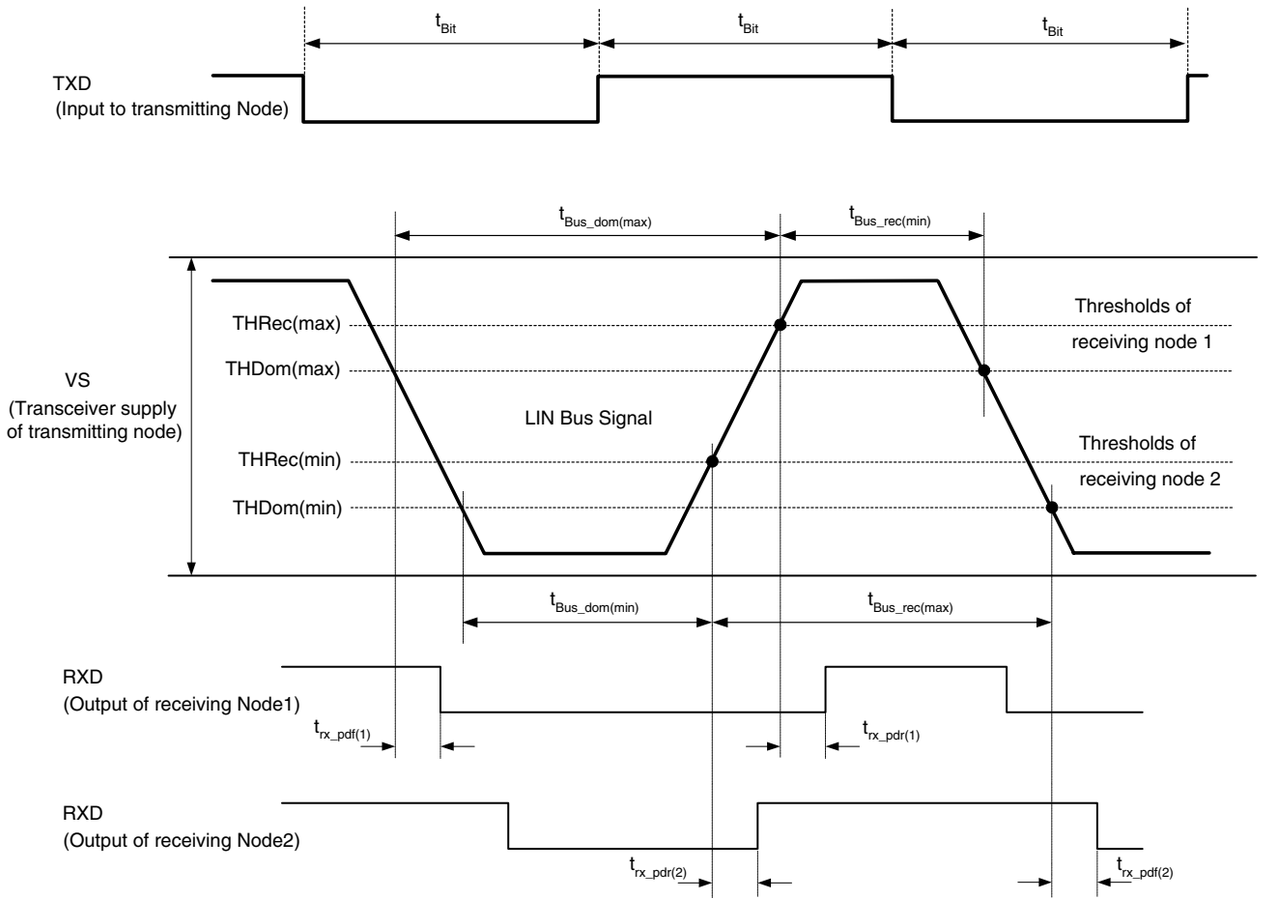
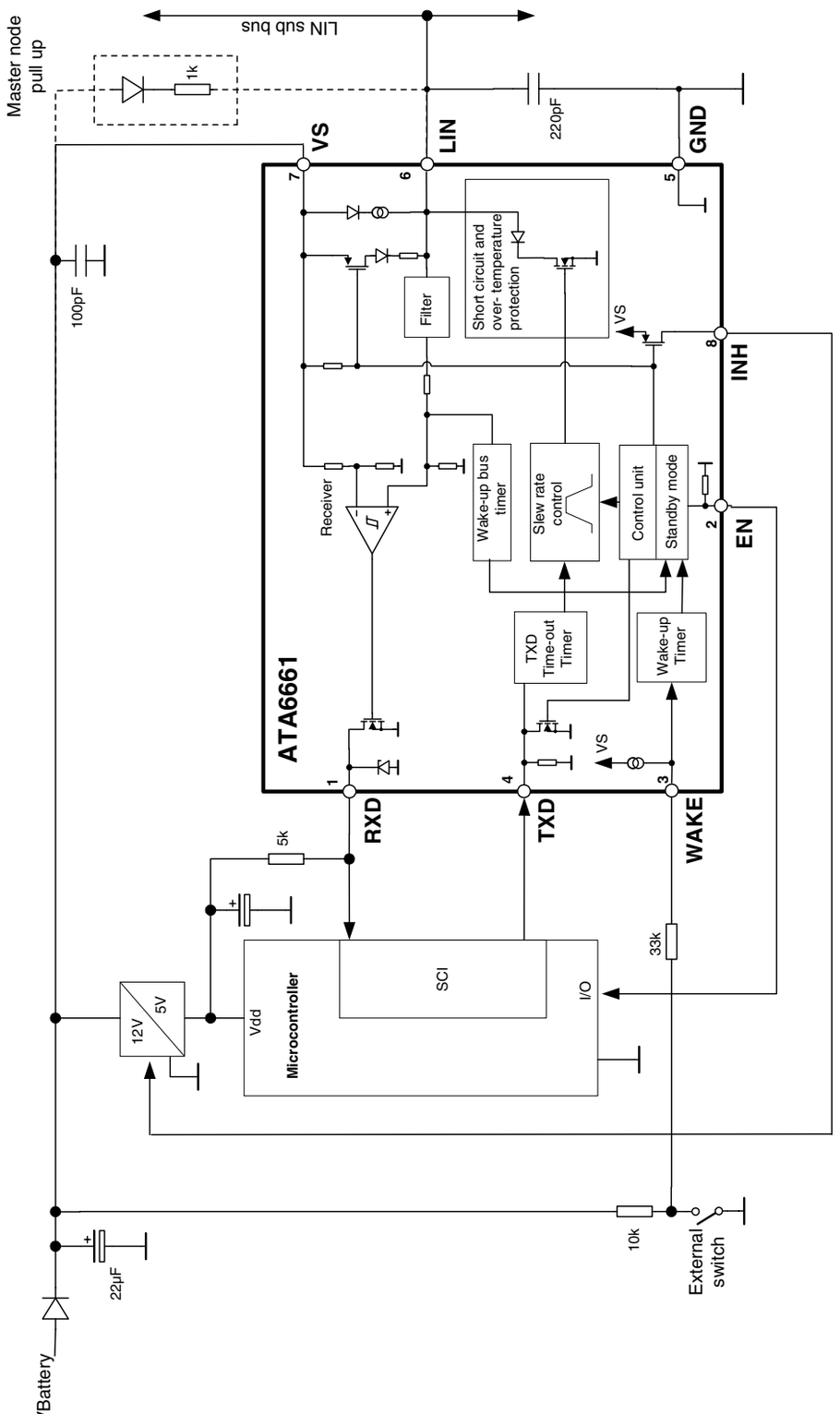


**Figure 7.** Application Circuit



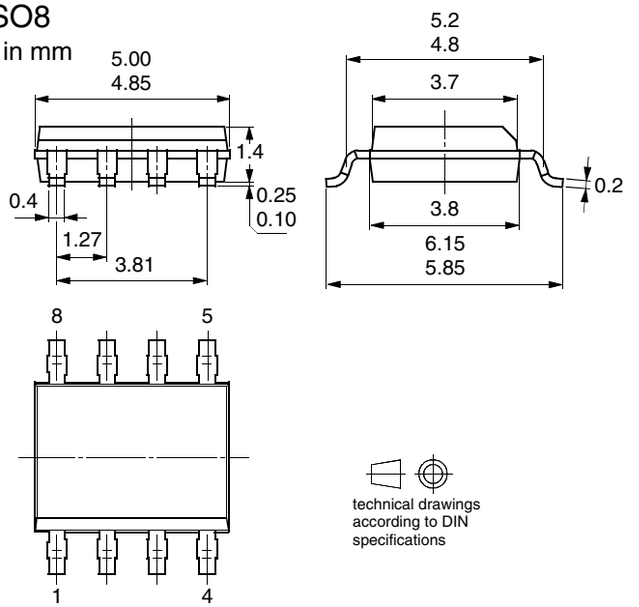
## Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| ATA6661-TAQJ | SO8 | LIN transceiver |

## Package Information

Package SO8

Dimensions in mm



## Revision History

Please note that the referring page numbers in this section are referred to the specific revision mentioned, not to this document.

### Changes from Rev. 4729B - 05/04 to Rev. 4729C - 06/04

1. Table “Ordering Information” on page 13 changed.

### Changes from Rev. 4729C - 06/04 to Rev. 4729D - 10/04

1. Put datasheet into new template (new last page)
2. Page 1: Features changed, Block diagram changed
3. Page 2: Bus Pin (LIN): Text changed
4. Page 3: TX Dominant Time-out Function: Text changed
5. Page 3: Output Pin (RXD): Text changed
6. Page 3: Inhibit Output Pin (INH): Text changed
7. Page 3: Wake-up Input Pin (WAKE): Text changed
8. Page 4: Remote Wake-up via Dominant Bus State: Text changed
9. Page 5: Section Fail-safe Features added
10. Page 7: Abs. Max. Ratings Tabelle: some changes
11. Pages 8-10: El. characteristics: changed rows: 1.3, 1.4, 1.5, 6.2, 7.9, 7.10, 7.11, 9.3
12. Pages 8-10: El. characteristics: changed rows: 2.4 (added), 8.5 (added), 8.6 (added), 8.7 (added)
13. Page 12: Application Circuit changed

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